Delay and Energy Efficient Low-Voltage Dual Tail Comparator

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***Abstract*—The necessity for ultra low-power, area efficient, and high speed analog-to-digital converters is forcing toward the use of dynamic regenerative comparators to boost up speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions calculated. From the analytical expressions, designers can achieve a perception about the main contributors to the comparator delay and completely given the tradeoffs in dynamic comparator design. Based on the analysis and by adopting sleep transistor approaches a new dynamic comparator is proposed, where the circuit of a conventional dual tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. The simulation results in 45nm technology shows that in the proposed dual tail dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153 μW, respectively. The standard deviation of the input-referred offset is 5 mV at 0.8 V supply.**

***Index Terms*—Dynamic clocked comparator, Dual-tail comparator, sleep approach, dynamic ,controlled dual tail,low power ,high speed ADCs design.**

1 INTRODUCTION

Comparator circuit compares two voltage or current signals and determines which one is greater. The result of this comparison is indicated by the output voltage. These are mostly used in ADCs. Dynamic latched comparators are useful for many applications such as high speed analog to digital converters (ADCs) due to high speed, low power consumption, high input impedance and full swing output. They use positive feedback mechanism with one pair of back to back cross coupled inverters (latch) in order to convert a small input voltage difference to a full scale digital level in a small time interval. The desire of many ADCs, are high-speed, low power comparators with small chip area. In high speed ultra deep sub micrometer (UDSM) CMOS comparators, the technology suffers from lower supply voltages. This is intense especially when considering the fact that threshold voltages of the devices have not been scaled at the same speed as the supply voltages of the modern CMOS processes.This low voltage leads to limited common-mode input vary, that is vital in several high-speed ADC architectures, like flash ADCs. Supply boosting technique (SBT) is suitable for sub-micron CMOS processes containing MOSFET transistors with threshold voltages comparable to the supply voltage, but these introduce some reliability issues.Techniques using body-driven transistors, current-mode design and dual-oxide processes, which may handle higher supply voltages, are developed to satisfy the low voltage design challenges The most well known technique is sleep approach, in this an additional sleep transistors such as an extra sleep PMOS or sleep NMOS transistor is placed between VDD and pull up network is placed to reduce the amount of power dissipation. In this paper the analytical expressions about the delay of dynamic comparator has been presented for different architectures Furthermore, depend on the double-tail structure a new controlled double tail comparator is presented, which does not require boosted voltage or connecting of too many transistors. Just by adding a few small size transistors to the conventional double tail dynamic comparator, maximize the latch speed and a new sleep approach, thus providing a new choice to low leakage power VLSI designers.

This paper is organized as follows. Section II describes the operation of the regenerative dynamic comparators and the problems and conclusions of each structure is discussed the analytical expressions for the delay of the comparators are presented the proposed comparator and its sleep transistor approach is presented in Section III. Simulation results are represented in Section IV and conclusions in Section V.

2. REGENERATIVE DYMANIC COMPARATORS

2.1 Conventional dynamic comparator

Conventional dynamic comparator widely used in ADCs, with high input impedance, full swing output and no static power consumption. The disadvantage is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time and this structure has only one current path, via tail transistor *M*tail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch and the tail transistor operates in triode region which is not acceptable for regeneration.

2.2 Conventional dual tail Dynamic Comparator

A conventional dual tail comparator is shown in Fig 1. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider mtail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low offset. The operation of this comparator is as follows (see Fig (c)). During reset phase (CLK = 0, *N*tail1, and *N*tail2 are off), transistors *P2-P1* pre-charge f2 and f1 nodes to *V*DD, which in turn causes transistors *N*R1 and *N*R2 to discharge the output nodes to ground. During decision-making phase (CLK = *V*DD, Mtail1 and Mtail2 turn on), *P2-P1* turn off and voltages at nodes f2 and f1 start to drop with the rate defined by *I*Mtail1*/C*f2*(1)* and on top of this, an input-dependent differential voltage Δ*V*f2*(1)* will build up. The intermediate stage formed by *N*R1 and *N*R2 passes Δ*V*f2*(1)* to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise. Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, *t*0 and *t*latch. The delay *t*0 represents the capacitive charging of the load capacitance *C*lout is given as

$$t_o = \frac{(C_{Lout}\, V_{Thn})}{I_{B1}} \approx \frac{2\,(C_{Lout}\, V_{Thn})}{I_{tail2}} \qquad (1)$$

After the first n-channel transistor of the latch turns on (for instance, N4), the corresponding output (e.g., Outn) will be discharged to the ground, leading front p-channel transistor (e.g., P3) to turn on, charging another output (Out1) to the supply voltage (VDD) , the regeneration time (tlatch) is obtained

$$t_{latch} = \frac{C_L}{g_{m,eff}} . ln\left(\frac{\Delta V_{out}}{\Delta V_o}\right) = \frac{C_L}{g_{m,eff}} . ln\left(\frac{\Delta V_{DD}/2}{\Delta V_o}\right) \qquad (2)$$

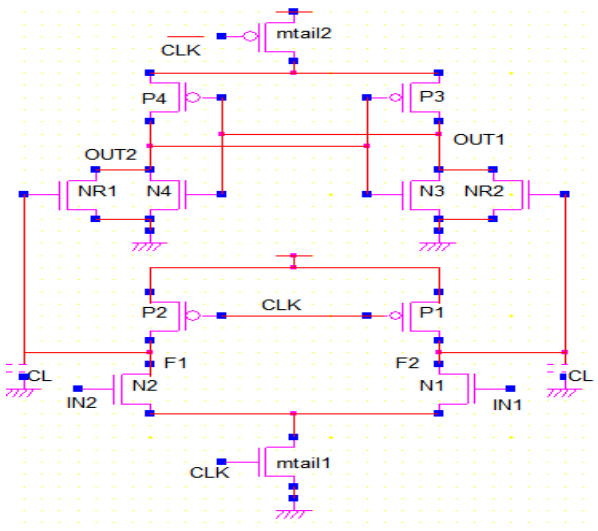


Fig 1. Schematic diagram of dual tail comparator

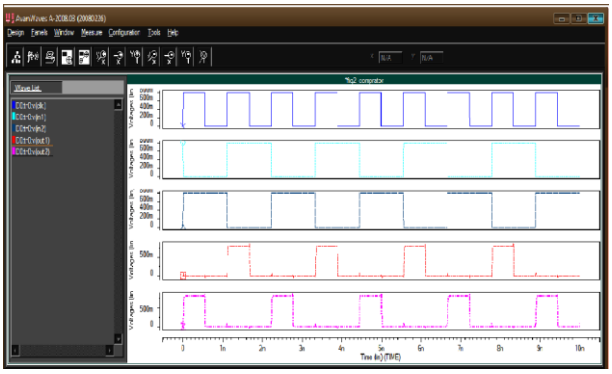


Fig 2. Transient simulations of the dynamic dual tail comparator for input voltage difference of Δ*V*in = 5 mV, *V*cm = 0.7 V, and V_{DD} = 0.8V

This equation shows that Δ*V*0 depends strongly on the transconductance of input and intermediate- stage transistors, input voltage difference (Δ*V*in), latch tail current, and the capacitive ratio of *CL*out to *CL,*f2*(1)*. Substituting Δ*V*0 in latch regeneration time, the total delay of this comparator is achieved as follows

$$t_{delay} = t_o + t_{latch}$$

$$= 2\frac{C_{Lout}V_{Thn}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot ln\left(\frac{\Delta V_{DD}/2}{\Delta V_o}\right)$$

$$= 2\frac{C_{Lout}V_{Thn}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot ln\left(\frac{V_{DD}\cdot I^2_{tail2}\cdot C_{L,f2(1)}}{8V_{Thn}{}^2\cdot C_{Lout} g_{mR1.2} g_{m1.2}\Delta V_{in}}\right) \qquad (3)$$

From the equations two important conclusions are developed on the dual tail dynamic comparator.

1) The voltage difference at the first stage outputs (Δ*V*f2/f1) at time *t*0 is increased then the amount of delay would profoundly reduce.

2) In this comparator during the reset phase both the transistors charged from ground to vdd due to this the amount of power dissipation increases.

2.3 Controlled DualTail Dynamic Comparator

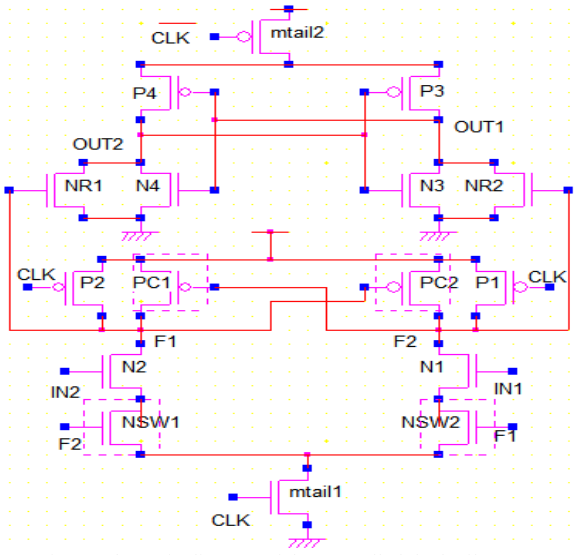


Fig 3. Schematic diagram of the controlled dual tail comparator

The operation of the controlled dual tail comparator is same as dual tail comparator. During reset phase (CLK = 0, m_{tail1} and m_{tail2} are off, avoiding static power), *P1* and *P2* pulls both f1 and f2 nodes to V_{DD}, hence transistor *P*c1 and *P*c2 are cut off. Intermediate stage transistors, *N*R1 and *N*R2, reset both latch outputs to ground. During decision-making phase (CLK = V_{DD}, *m*tail1, and*N*tail2 are on), transistors *P1* and *P2* turn off. In the proposed structure as soon as the comparator detects that for instance node f2 discharges faster, a pMOS transistor (*P*c1) turns on, pulling the other node fp back to the V_{DD}. Therefore by the time passing, the difference between f1 and f2 ($\Delta V_{f1/f2}$) increases in an exponential manner, leading to the reduction of latch regeneration time. The transient simulation results are shown below. The delay of controlled dual tail comparator comprised by two parameters .those are delay due to t_0 and delay due to t_{latch} Each of these factors will be discussed in detail.

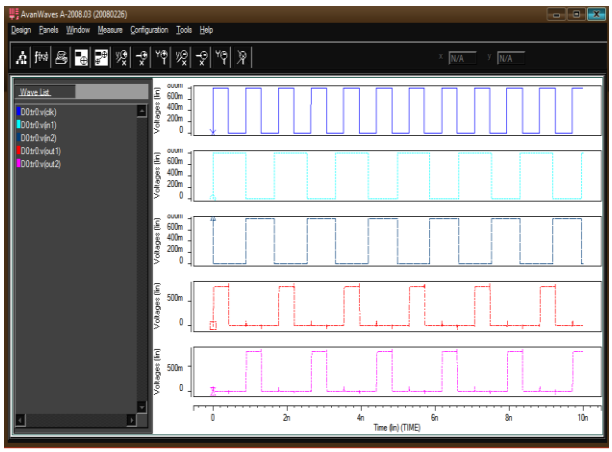


Fig 4. Transient simulations of the proposed dual tail comparator for input voltage difference of ΔVin = 5 mV, *V*cm = 0.7 V, and V_{DD} = 0.8V

2.3.1 Effect of enhancing ΔV0

The delay time *t*0, is define as time after which latch regeneration starts or *t*0 is considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the back-to-back inverters turns on, so that it will pull down one of the outputs and regeneration will starts in this comparator we have

$$\Delta V_O = 2V_{Thn}\frac{g_{mR1.2}}{I_{tail2}}\Delta V_{\frac{f2}{f1}}$$

$$= 4V_{Thn}|V_{Thp}|\frac{g_{mR1.2}}{I_{tail2}}\frac{g_{m1.2}\Delta V_{in}}{I_{tail1}}exp\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,f2(1)}}\right)\cdot \quad (4)$$

2.3.2 Effect of improving Effective Transconductance of latch

In the previous comparator design the nodes f1 and f2 discharged completely to ground but in our proposed comparator only one of the first stage output nodes (f1/f2) will charge up back to the *V*DD at the beginning of the decision making phase, will switch on one of the control transistors, thus the effective transconductance of the latch is increased. i.e the positive feedback is improved . Hence, *t*latch will be

$$t_{latch} = \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}}\cdot ln\left(\frac{\Delta V_{out}}{\Delta V_o}\right)$$

$$= \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}}\cdot ln\left(\frac{\Delta V_{DD}/2}{\Delta V_o}\right) \quad (5)$$

Therefore the total delay is given as

$$= t_o + t_{latch} \quad = 2\frac{C_{Lout}V_{Thn}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}+g_{mR1,2}}\times$$

$$ln\left(\frac{V_{DD}/2}{4V_{Thn}|V_{Thp}|\frac{g_{mR1.2}}{I_{tail2}}\frac{g_{m1.2}\Delta V_{in}}{I_{tail1}}exp\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,fn(p)}}\right)}\right) \quad (6)$$

By comparing the equations for the delay of the three mentioned structures, it can be observed that the proposed comparator takes advantage of an inner positive feedback in dual tail operation, which strengthens the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of *V*Th/*V*DD, the transconductance of the transistors decreases, thus the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator .These results are shown in Simulation analysis.

2.3.3 Reduction in Energy per Comparison

In conventional dual tail topology, both f2 and f1 nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the *V*DD. However, in our proposed comparator, only one of the mentioned nodes (f1/f2) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required. This can be seen when being compared with conventional topologies.

3. DYMANIC COMPARATORS DESIGN USING SLEEP TRANSISTOR APPROACH

An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal power gating is more suitable. CMOS switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

3.1 conventional sleep dynamic comparator

Here we are connencting sleep transistor i.e either PMOS or NMOS is connected at Vdd or at ground resepectively, by connecting these sleep transistor we can reduce the amount

of power dissipation and optimum delay ia achieved the schematic diagram of resepective comparator is shown below.

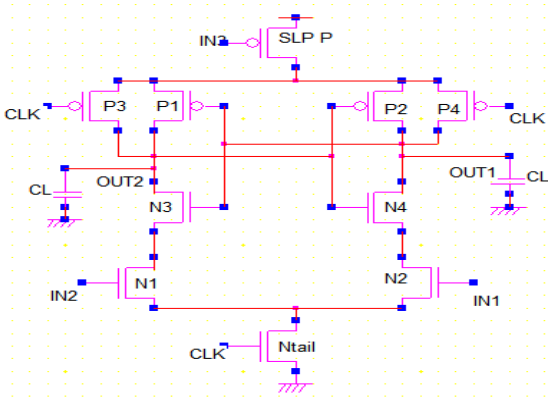


Fig 5. Schematic diagram of conventional sleep dynamic comparator

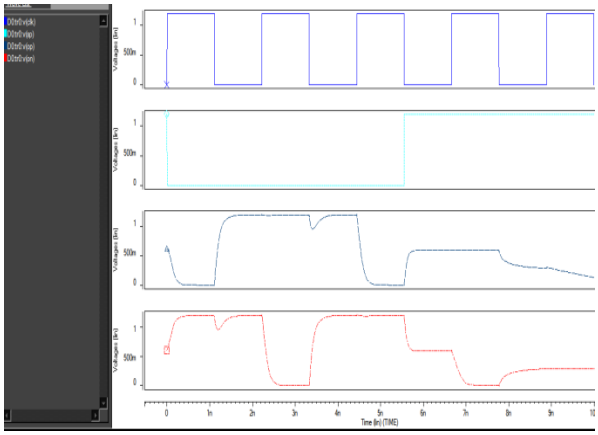


Fig 6. Transient simulations of conventional sleep dynamic comparator for input voltage difference of ΔVin = 5 mV, Vcm = 0.7 V, and V_{DD} = 0.8V

3.2 Proposed sleep controlled Dual-Tail comparator

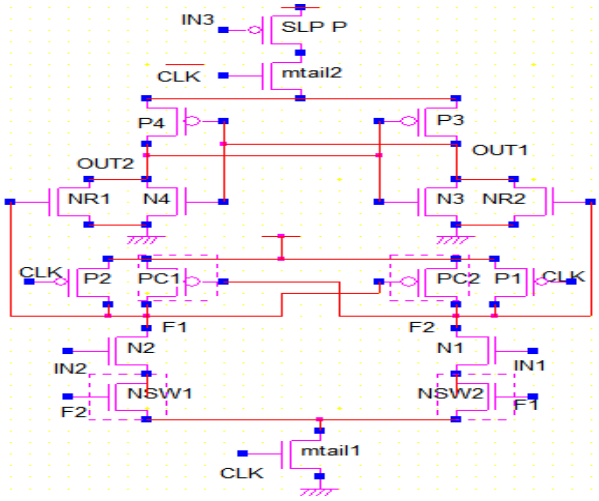


Fig 7. Schematic diagram of the proposed dual tail comparator

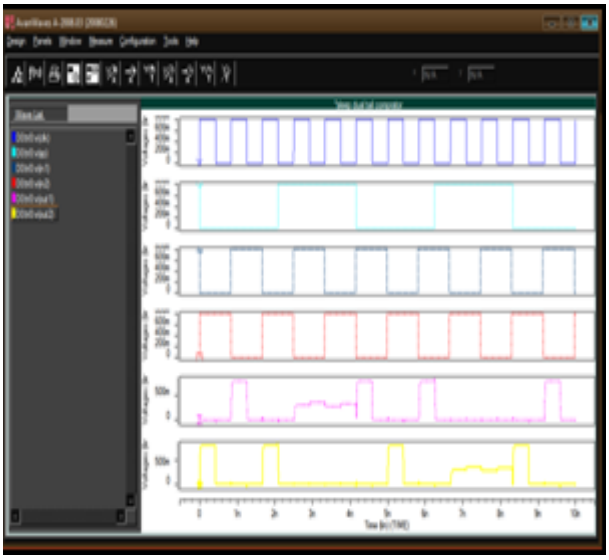
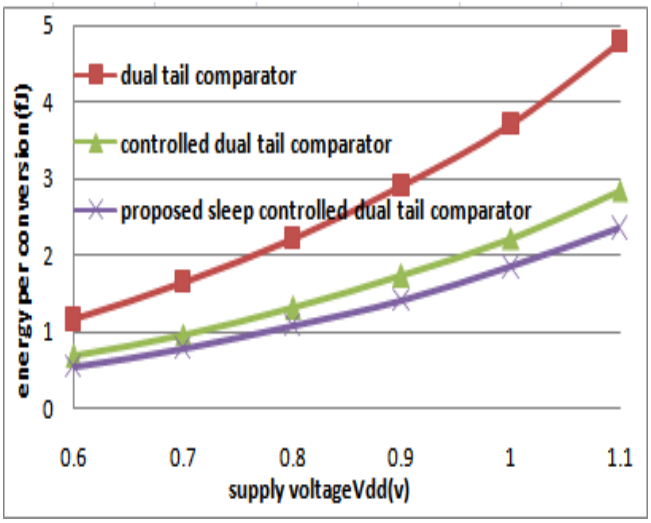


Fig 8. Transient simulations of the proposed sleep dual tail comparator for input voltage difference of ΔVin = 5 mV, Vcm = 0.7 V, and V_{DD} = 0.8V

The operation of the proposed sleep dual tail comparator, during reset phase (CLK =in3=0, N_{tail1} and N_{tail2} are off, avoiding static power), *P1* and *P2* pulls both f1 and f2 nodes to V_{DD}, hence transistor *P*c1 and *P*c2 are cut off. Intermediate stage transistors, *N*R1 and *N*R2, reset both latch outputs to ground. During decision-making phase (CLK =in3= V_{DD}, *N*tail1, and*N*tail2 are ON) .the sleep transistor doesn't allow vdd to latch circuit. The amount of leakage power reduces negligibly small compared to proposed comparator.

4. SIMULATION RESULTS

The comparison of proposed comparator and sleep comparator with existing design can be observed by simulated in 45nm CMOS technology with V_{DD}=0.8V and offset deviation of 5mv at the input common mode voltage of V_{cm}=0.7v



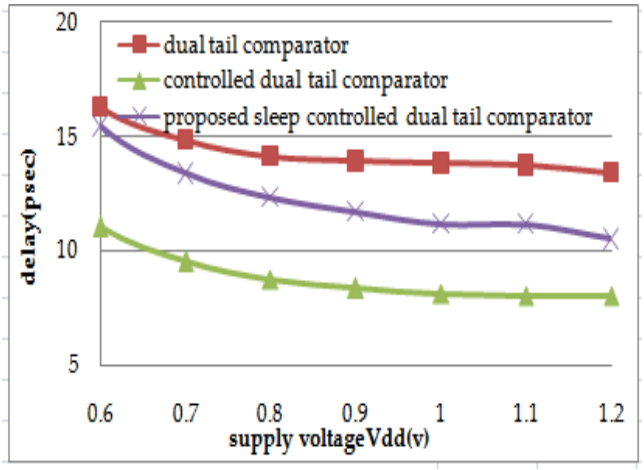


Fig 9. Post-layout simulated (i) energy per conversion and (ii) delay as a function of supply voltage (ΔVin = 5 mV, Vcm = VDD − 0.1)

Table I
Performance comparsion

Comparator structure (45nm Vdd=0.8v)	**Sampling frequency**	**Delay /log(ΔVin) (psec/dec)**	**Energy per conversion (p/fs) fJ**
Conventional dynamic comparator	900MHz	51.51	7.3
Convential dual tail comparator	1.8GHz	6.14	2.22
Controlled dual comparator	2.4GHz	3.82	1.3
Sleep controlled dual tail comparator	2.4GHz	5.37	1.07

5. CONCLUSION

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were represented. Based on theoretical analyses, a new dynamic comparator with sleep transistor and without sleep transistor with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in *45n*m CMOS technology confirmed that energy per conversion of the proposed comparator is reduced and delay was optimally reduced in comparison with the existing designs.

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Tirumalareddy anjireddby was born in Andhra pradesh in 1991. He received his b.tech degree In Electronics and Communication Engineering from jntu Kakinada, Kakinada A.P. in 2012, where he is pursuing his M.Tech in VLSI SysDesign. In Electronics and Communication Engineering dept. with research going on Energy efficient low voltage dual tail comparator

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