Data Stored Based Test Pattern Generation in Flash Memory

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***Abstract*-The Flash Memory built with floating gate transistor are easily affected by device noises that leads to Bit Error Rate(BER). These noises heavily depend on the stored data pattern. Data Pattern Aware(DPA) is proposed to manipulate the ratio of 0's and 1's in stored data to reduce the probability of Data Patterns which are easily affected by device noises. A test pattern is proposed to monitor the input vectors for concurrent testing of NAND flash memory. Only required test pattern are picked out from the entire sequence of generated test pattern. These sequences are selected based on the data stored in memory. A response vector provides a comparison and determines that the memory contains tested data for the given input.**

Keyword: NAND flash memory, Data pattern and Test pattern generation.

I. INTRODUCTIOIN

Flash memories are non-volatile memory that are built in with a floating gate transistor which does not require power to retain data. There are two types of flash memory. NAND flash memory is preferred due to its lowest cost per bit and has its maximum chip capacity so that they can compute with magnetic storage devices like hard disk. It is designed in such a way that they provide banked memory structure. There are several hierarchy of memory cells. Multilevel Cell (MLC) can represent two-bits per cell, this provides four sequences of data to store in single cell.

In reference to the previous work it is identified that MLC NAND flash memory are easily affected to device noises such as program disturb, read disturb, and retention time noise which are identified as Bit Error Rates (BER). Program disturb are caused due to cell to cell interference and Random Telegram Noise (RTN) [1]. At high electric field, the electrons tunnel through a barrier called field emission also called Fowler-Noedheim tunneling [2], which results in read disturb. This read disturb is also due to an increase in the gate leakage current called the Stress Induced Leakage Current (SILC) [3]. Retention time noise occurs during charge loss on the floating gate. These are the major cause of BER which highly depends on the pattern of the data stored in the memory. Storing data into a memory by containing the maximum number of 1's will provide a secured space from these noises. A process called Data Pattern Aware (DPA) will execute the process of making the given input data secured [1]. This work focus on the prevention of error that occurs on the memory. A test pattern is generated in need of concurrent testing of the given input data stored in the memory. The main idea of the is to provide,

- The given input data is modified and stored using DPA.
- A part of DPA function known DPA-PPU (Pattern Probability Unbalance) modifies the pattern of the given data from the lowest number 1's to its maximum. DPA-DRM (Data Redundancy Management) manages the redundancy caused by the process during the modification process.
- Test pattern generated for the data pattern to be stored in memory and verified each time after every reset.

The test pattern generation for the data stored would provide us a better error resistant data content in memory. It also provides us double assurance of the given input data that the user given to store it in the chip memory.

II. BASIC OF FLASH MEMORY USED

A NAND flash memory is a banked memory structure. It allows high data rate transformation since it can be addressed independently. They are designed to support multimedia files which implies high bandwidth. There are several memory hierarchy based on their capacity of the bits per cell. Multilevel Cell (MLC) has the capacity to store two bits of information per cell. Four sequences of information can be stored in a single cell. The information stored in the cell are represented by v_{th} level (L0~L3). As discussed earlier the information in the cell are easily affected to the program disturb, retention time noise and read disturb, these are together called bit errors. The Bit Error rate (BER) is increased due to program/erase cycle of the memory and heavily depends on the data pattern stored in the memory. The information stored as v_{th} level in the memory contains data pattern with both 0's and 1's. The data containing maximum number of 1's is not easily affected by these noises, automatically the v_{th} distortion is reduced.

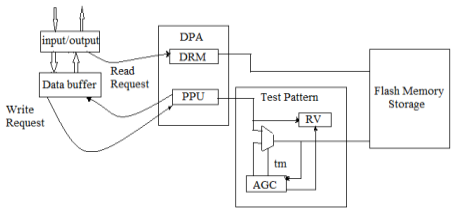

Fig. 1. Overview Data pattern and Test pattern generation

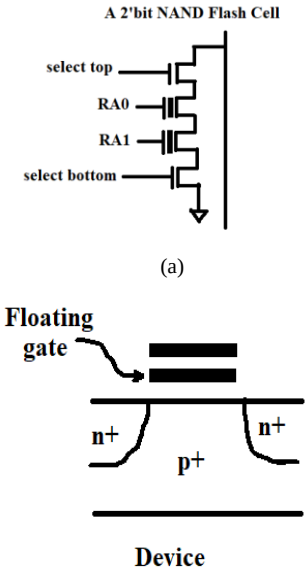

Fig. 2. Flash memory. (a). Flash Memory device. (b). MLC NAND Flash memory.

III.DATA PATTERN AWARE (DPA)

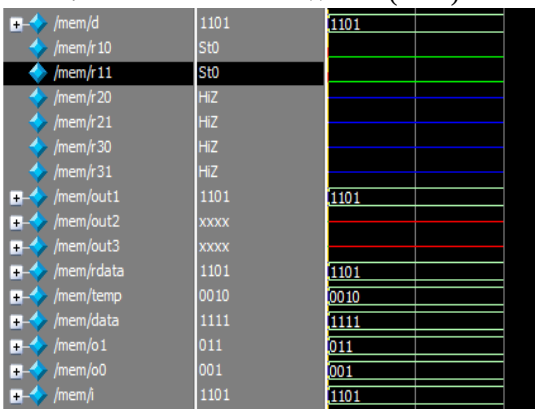

Fig. 3. DPA process for the given input data

DPA modifies or manipulates the given input data pattern to the highest ratio of ones. It implies two major parts namely DPA-PPU (Pattern Probability Unbalance) and DPA-DRM (Data Redundancy Management) [1]. DPA-PPU modifies the ratio of ones by scrambling and decorrelation process in which they are achieved using XORing process. The given input pattern is first inverted and then XORed with the original input pattern given and stored into the memory. This increases the ratio of the one's in the given data and makes data error resistant of the device noises. By storing the data in this way would also provide an efficient storage system of NAND flash memory. The retrieval of the actual input data can be obtained by descrambling and correlation process. Now inverted data is XORed with modified data pattern stored in the memory to obtain the actual input data pattern given. Repetition of this process will lead to data redundancy which is managed DPA-DRM. A redundancy page is available in every data pages. These pages are used in managing the data redundancy and plays an important work in descrambling process by storing the data that is used to scramble the actual input pattern given. Before every retrieval process checks its page to verify only required information is stored. Other than the required one this page will automatically erase the content in it. By this process it easily manages the data redundancy that occurs in memory. The main advantage of this technique is that it provides error resistant data even when the power is off. This technique provides data recurrence in an efficient way even if the system is on or off state. A test pattern is generated in this work to make dual assurance data. From this process, the data to be stored is known and test pattern only required is selected. Fig 4 represents the DPA generated for the given input data.

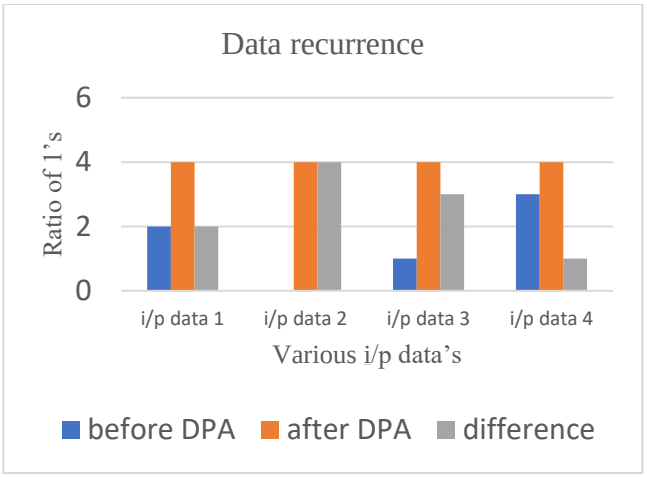

Fig. 4. Ratio of 1's increased in given input data

IV. RELATED WORK

The process of reducing the rate of error occurrence by the process of DPA increases the error resistance by increasing the ratio of 0's and then inverted to the maximum ratio of 1's [1]. To reduce the error rate BER nibble remapping code [9] was proposed by reducing the number of 1's in the data pattern given. Before this a scheme was introduced called refresh scheme to reduce the retention time noise that cause error in the system. Many codes such as LPDC code and reed-Solomon code [7] to improve the system reliability based on the performance of error correction done for the given input data were proposed. These codes come under soft-decision code [6] that is applied to improve the system storage. To extend the lifetime of the system error prediction [8] was introduced.

Multiple search patter technique was proposed to monitor the test sequence concurrently based on the concurrent scan monitoring provides a better test data with less latency and improved fault coverage in the memory system [12]. A combination uploaded test patterns of multiple binary sequences are searched by Concurrent Scan Test (CST) [14]. A total fault coverage in a memory is quite difficult, very small number of test pattern or a vector can detect the error that occurs [15]- [18]. It is found that previous works generates test pattern for the data that are directly stored to the memory. There are many possibility of error occurrence even test pattern is generated which would occur at the time of input data stored in memory are frequently gone through read or write process. This work would provide a better recurrence of data since it has double security of DPA and test pattern.

V. TEST PATTERN GENERATION

Test pattern for the data stored is generated based on the Built in Self Technique (BIST) technique unlike used in every testing process. This technique allows the system itself to check or test the data stored, which helps in increasing the controllability and observability of the chip or memory. It is designed for reducing the cost, caused by the duration of the test cycle taken or the probe setup that is cause complexity. The test cycle and the probe setup are reduced by minimizing the input and output signals that are driven under tester control. It includes the idea of pseudorandom generator and cyclic redundancy checker (CRC). This technique provides us less cost on testing at the time of manufacture. A pseudorandom generator will provide 2^n-1 non-zero sequences of output for n sequences of input. Test pattern generated are send to the circuit under test to verify and its response is obtained at the response verifier.

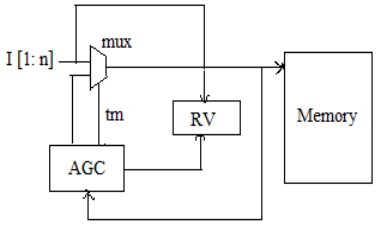

Fig. 5. Test Pattern Generation.

The given data after the DPA process is given to the testing part. Sequence of pattern are generated at the pattern generation part and send to the check the data received. Automatic Gain Control (AGC) is used to control the generated test pattern. It allows only the required test pattern and quits the remaining pattern.

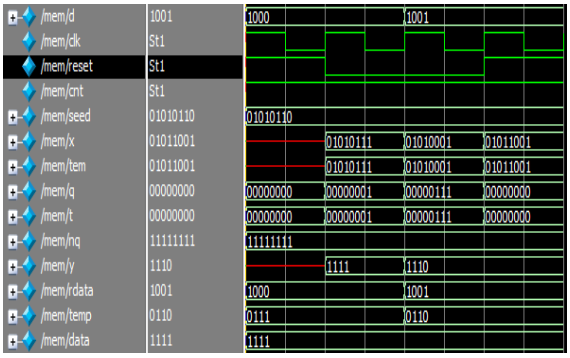

Fig. 6. Simulation of test pattern generated after DPA

A mux is used to send only the pattern that matches with the actual data and the pattern generated. The output of the tested data is verified with response at the response verifier. Then the data is stored to the memory and retrieved as the original data at the output section.

VI. CONCLUSION

The presented idea includes the concept of DPA along with the test pattern generation. Input data given are stored with maximum ratios of 1's to make the data secured from the noises that occurs at memory. Along with this test pattern are generated from the pseudorandom generator to make the stored data pattern more secured. It provides us a best way of protecting the data given, from the device noises and fault that occurs in the memory or chip. This experimental result states that this technique provides an improved data assurance that is stored in memory.

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