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Data Compression and Decompression Method and System for Communication System

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Abstract:- **With the rapid development of mobile communication technology, the demand for signal transmission bandwidth is increasing. Technologies such as carrier aggregation will also increase the amount of data transmitted between the baseband processing unit and the remote radio unit. This puts forward higher requirements for optical fiber transmission capabilities. In the current communication system based on optical fiber transmission, the application of optical modules with a transmission rate of 10Gb/s has become popular. In 5G applications, 40G or 100G optical modules are even required to meet the ever-increasing application requirements. In order to reduce and control the consumption of optical fiber resources, it is necessary to develop a data compression method to reduce data transmission pressure and reduce costs. This paper proposes an IQ data compression and decompression algorithm based onFPGA hardware and according to the characteristics of programmable logic devices. As a result, the antenna system improves the efficiency of radio frequency power amplifiers, and reduces operation and maintenance costs.**

Keywords*: *Digital communication, Data compression, IQ data compression

I. INTRODUCTION

With the release of 5G licenses and commercial applications, the demand for radio access will increase explosively. Operators can continuously deploy new cellular stations to cope with the surge in data traffic. But it will lead to an increase in network operation costs and installation complexity. As the number of antennas or signal bandwidth increases, link capacity becomes a bottleneck. One solution is to use multiple modules or high-speed modules, which are expensive.

Recently, IQ data compression/decompression methods [1-6] have been proposed to solve the problems of low cost and high capacity. In Hu's work [7], the energy of the data needs to be counted. Then the mark bit is determined according to the threshold range for truncation processing. The mark bit is transmitted with the control word of the CPRI frame. After the shift factor is determined, the grouped data is shifted and then quantized [8]. The system requires additional transmission of the compression factor and the flag bit of each compressed data [9].

This paper proposes a simple and easy-to-implement baseband signal compression and decompression algorithm. This data compression algorithm eliminates redundant information in IQ data to reduce the cost of useless information transmission. The data compression and decompression algorithms described in this paper are implemented based on FPGA hardware. According to the characteristics of programmable logic devices, a structure system of IQ compression and decompression is proposed.

After the data received by the antenna undergoes analog- to-digital conversion, it is down-converted to baseband. Then according to the bandwidth occupied by valid data, the antenna will perform filtering and extraction operations. The system will reduce the data transfer rate. The data compression module further compresses the transmission bit of IQ data. After framing according to the CPRI protocol, it is transmitted to the remote end through optical fiber. The receiver first receives the data transmitted by the optical fiber, then CRPI deframes the data, and finally decompresses the data. Then the data is interpolated, up-converted, and digital-to-analog converted, and then sent out through the antenna for signal coverage.

II. DATA COMPRESSION PRINCIPLE

The block diagram of the data compression and decompression principle of this system is shown in Figure 1

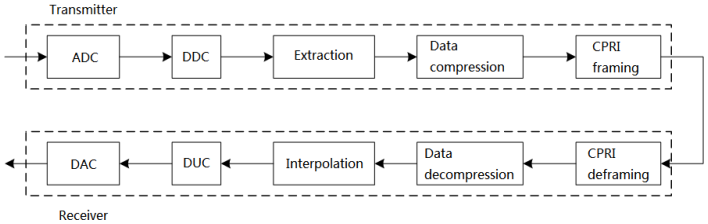

Figure 1: Schematic diagram of data compression and decompression system.

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In order to increase the efficiency of signal transmission, the system compresses the signal before transmission. Fixed-point IQ data is grouped. The grouped IQ data is respectively determined the maximum absolute value of the group of data. Then the maximum value is compared with the maximum power at full scale calibration to determine the shift factor *k* of the group. According to the shift factor *k* corresponding to each group, the I data and Q data of each IQ data in the group are respectively shifted and truncated to obtain compressed data. The shift factor *k* of each group and the compressed data of each group are sent to the receiver. The receiver performs decompression according to the packet length *N*, the shift factor *k* of each group, and the compressed data of each group.

Taking the actual situation of this paper as an example, the data bit width is 14 bits, and it becomes 10 bits after compression.

The group length is 4, the steps are as follows:

1) Confirm the input bit width $M = 14$.

2) Determine the compression ratio $k = 14{:}10$.

3) Determine the packet length $N = 4$.

4) Each grouped data is divided into two IQ channels. Shift and truncation are performed in units of groups, which are compressed data.

5) The equation that produces the shift information:

$$W_I = \frac{[\ln(2^{m-1})]}{\text{Max}(\text{abs}(\text{data}_{i}))} \quad (1)$$

where *i* is the serial number of the current group, *M* is the original data bit width, and $data_i$ is the data in the current group.

6) Determine the cut bit width bit_{cut} according to the compression ratio $k = 14/10$, the input bit width *M* of the data to be compressed, and the shift information bit width *N* (which is an integer, and the value of *N* is 1 in this paper).

$$_{\text{bitcut}} = M — \frac{M}{K} + N \quad (2)$$

Remark: The compression ratio k can be determined according to the requirements of compression processing, suchas 2:1, 3:2, etc. The highest bit in the compressed data is still the sign bit. The data bit portion of the compressed data follows it. The tail is overhead bit, such as shift information. After receiving the compressed data, the decompression transmitter can decompress it correctly. Assuming that the input bit width of the data to be compressed is $M = 12$ and thecompression ratio $k = 14{:}10$, the compressed data bit width is

10. If the overhead bit is 1 bit, the highest bit of the compressed data is the sign bit. The next 8 bits are the compressed data bits, and the lowest 1 bit is the overhead bit.

The compression module is designed to compress the effective data by truncating, which is lossy compression. When the data effective bit width is smaller than the compressed bit width, the high sign bit is truncated. When the effective bit width of the data is more than the compressed bit width, in order to ensure the linearity of the data, only one sign bit in the data is reserved. Then the system truncates the excess low data bits through rounding. The system will keep the lowest bit in the output data. A schematic diagram of data compression from 14 bits to 10 bits is shown as Figure 2.

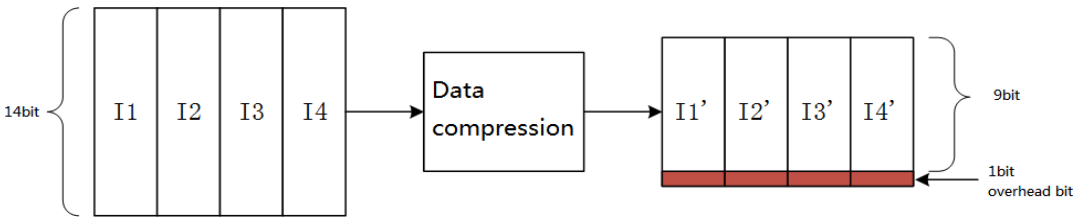

Figure 2: A schematic diagram of data compression from 14 to 10 bits.

The key to this paper is to group data. Then the system finds the maximum value of the absolute value of each group of data, and determines the maximum bit width required to represent the maximum value. Then the data is truncated. Finally, the truncation code is scattered and stored on the overhead bits of the reorganized data.

In order to facilitate data recovery at the decompression transmitter, the truncation code is encoded. It is shown in Table 1.

Table 1: The correspondence table of data compression control bits.

Code	Description
4'b0000	Code No. 1, truncates the high sign bit of the input data, and retains the low data bit.
4'b0010	Code No. 2, truncating the input data bit0 and the extra high sign bit.
4'b0100	Code No. 3, truncating the input data bit0~bit1 and the extra high sign bit.
4'b0110	Code No. 4, truncating the input data bit0~bit2 and the extra high sign bit.
4'b1000	Code No. 5, truncating the input data bit0~bit3 and the extra high sign bit.

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4'b1010	Code No. 6, truncating the input data bit0~bit4 and the extra high sign bit.
4'b1100	Code No. 7, truncating the input data bit0~bit5 and the extra high sign bit.
4'b1110	Code No. 8, truncating the input data bit0~bit6 and the extra high sign bit.
4'b1111	Synchronization encoding, used to synchronize data when recovering data on the decompression side.

Remark: The synchronization code here is a special code. If there are codes with the same consecutive number in the link, every other code will generate a synchronization code.

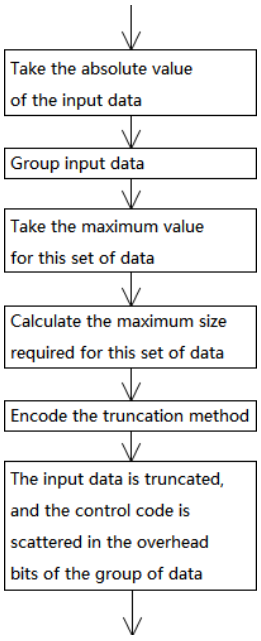

Figure 4: Data compression processing flow.

The decompression module separately extracts bit0 in the input data as a control bit.The remaining bit widths are signal bits.

After the data synchronization is completed, the lowest bit is extracted as a group of every four data to form a control bit code. The data is filled and outputted according to Table 2.

III. Result analysis

In the present invention, the baseband signal is processed by decimation to reduce the data rate of the effective bandwidth of the transmitted signal. Thus the system reduces the amount of data transmitted.

When performing data compression, the sender and receiver unify the packet length *N*. The shift factor of each group is decomposed into the overhead bits of the group of compressed signals for transmission. Therefore, the system does not require additional transmission.

In order to facilitate data recovery at the decompression transmitter, if consecutively numbered shift information codes appear in the link, a synchronization code is generated every other code. In this way, the receiver can identify the synchronization position based on the synchronization code.

Table 2: Correspondence table of data decompression control bits.

Code	Description
4'b0000	Code No. 1, fill the high sign bit of the input data.
4'b0010	Code No. 2, fill 0 in input data bit0, fill other high sign bit.
4'b0100	Code No. 3, fill 0 in input data bit0~bit1, fill other high sign bit.
4'b0110	Code No. 4, fill 0 in input data bit0~bit2, fill other high sign bit.
4'b1000	Code No. 5, fill 0 in input data bit0~bit3, fill other high sign bit.
4'b1010	Code No. 6, fill 0 in input data bit0~bit4, fill other high sign bit.
4'b1100	Code No. 7, fill 0 in input data bit0~bit5, fill other high sign bit.
4'b1110	Code No. 8, fill 0 in input data bit0~bit6, fill other high sign bit.
4'b1111	Synchronous coding, restore the last set of data control bits.

IV. The advantages and effects of this invention

In this paper, the baseband signal is processed through filtering and extraction. The data rate of the effective bandwidth of the transmitted signal is reduced. Thus the system reduces the amount of data transmitted. For signals with an effective bandwidth of 80M, the data processing rate can be reduced to 92.16Mps for processing.

The data compression method proposed in this paper intercepts the signal according to the transmission power of the data. When the power is low, the lower data is intercepted to avoid data damage. When the power is high, the damage to the signal linearity is also very small. This method can keep the characteristics of small signals as much as possible in the case of grouping. Moreover, this method is very simple and convenient for FPGA implementation. Furthermore, this method can control the synchronous coding to be transmitted with the compressed signal without additional overhead bits.

In this paper, the receiver adopts cyclic detection synchronization, which has strong reliability. Even if the transmission is abnormal due to external interference, it can be restored in a short time. The digital optical fiber remote system realized by this algorithm has been tested. It can be

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compressed to 8bit at most when meeting the requirements of system indicators. The compression ratio is 7:4, which effectively reduces the amount of data transmitted.

V. Conclusions

This paper proposed a new data compression and decompression algorithm. This algorithm eliminates the redundant information in IQ data and reduces the cost of useless information transmission. It is based on FPGA hardware implementation, the idea of the system comes from programmable logic devices. Simulation results showed that our method reduced the amount of data transmitted. For the signal with effective bandwidth of 80M, the data processing rate can be reduced to 92.16mps. It can be compressed to 8 bits at most when it meets the requirements of system indicators. Simulation results also showed that the compression ratio is 7:4, which effectively reduces the amount of data transmitted. Therefore, the antenna system improves the efficiency of RF power amplifier and reduces the operation and maintenance costs.

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