DA-Based DCT with Error-Compensated Adder Tree

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Abstract- **In this paper, by operating the shifting and addition in parallel, an error-compensated adder-tree (ECAT) is proposed to deal with the truncation errors and to achieve low-error and high-throughput discrete cosine transform (DCT) design. Instead of the 12 bits used in previous works, 9-bit distributed arithmetic-precision is chosen for this work so as to meet peak-signal-to-noise-ratio (PSNR) requirements. Thus, an area-efficientDCT core is implemented to achieve 1 Gpels/s throughput rate with gate counts of 22.2 K for the PSNR requirements outlined in the previous works.**

***Index Terms*-Distributed arithmetic (DA)-based, error-error-compensated adder-tree (ECAT), 2-D discrete cosine transform (DCT).**

I. INTRODUCTION

Discrete cosine transform (DCT) is a widely used tool in image and video compression applications [1]. Recently, the high throughput DCT designs have been adopted to fit the requirements of real-time applications. The high-throughput shift-adder-tree (SAT) and adder-tree (AT), those unroll the number of shifting and addition words in parallel for DA-based computation, were introduced in [3] and [4], respectively. However, a large truncation error occurred. In order to reduce the truncation error effect, several error compensation bias methods have been presented [5]–[7] based on statistical analysis of the relationship between partial products and multiplier-multiplicand. However, the elements of the truncation part outlined in this work are independent so that the previously described compensation methods cannot be applied. This brief addresses a DA-based DCT core with an error-compensated adder-tree (ECAT).The proposed ECAT operates shifting and addition in parallel by unrolling all the words required to be computed. Furthermore, the error-compensated circuit alleviates the truncation error for high accuracy design.

II.MATHEMATICAL DERIVATION OF DISTRIBUTED ARITHMETIC

The inner product is an important tool in digital signal processing applications. It can be written as follows:

$$Y= A^T X = \sum_{i=1}^{L} A_i X_i \quad \ldots\ldots (1)$$

where A_i, X_i, and L are *i*th fixed coefficient, *i*th input data, and number of inputs, respectively. Assume that coefficient A_i is Q-bit two’s complement binary fraction number. The inner product computation in (1) can be implemented by using shifting and adders instead of multipliers. Therefore, low hardware cost can be achieved by using DA-based architecture.

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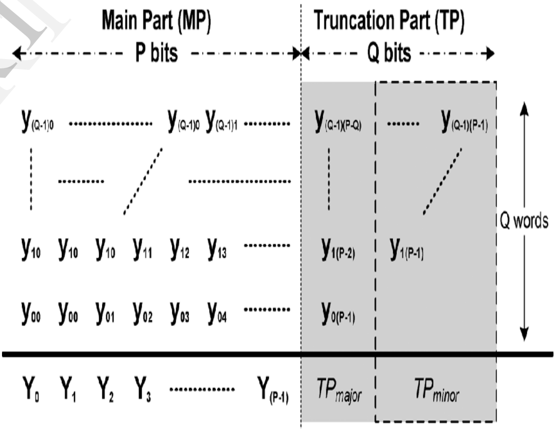
Main Part (MP)
P bits
Truncation Part (TP)
Q bits
$y_{(Q-1)0}$ $y_{(Q-1)0}$ $y_{(Q-1)1}$ $y_{(Q-1)(P-Q)}$ $y_{(Q-1)(P-1)}$
y_{10} y_{10} y_{10} y_{11} y_{12} y_{13} $y_{1(P-2)}$ $y_{1(P-1)}$
y_{00} y_{00} y_{01} y_{02} y_{03} y_{04} $y_{0(P-1)}$
Q words
Y_0 Y_1 Y_2 Y_3 $Y_{(P-1)}$
TP_{major}
TP_{minor}

Fig. 1. Q P-bit words shifting and addition operations in parallel.

III. ECAT ARCHITECTURE

The shifting and addition computation can be written as follows:

$$Y= \sum_{j=0}^{Q-1} y_j \,.\, 2^{-j} \,.\, \ldots\ldots (2)$$

In Fig. 1, the Q P-bit words operate the shifting and addition in parallel by unrolling all computations. Furthermore, the operation in Fig.1 can be divided into two parts: the main part (MP) that includes P most significant bits (MSBs) and the truncation part (TP) that has Q least significant bits (LSBs). Then, the shifting and addition output can be expressed as follows:

$Y= MP + TP .2^{-(P-2)}$. …… (3)

The proposed ECAT is explained as follows.

A. Proposed Error-Compensated Scheme

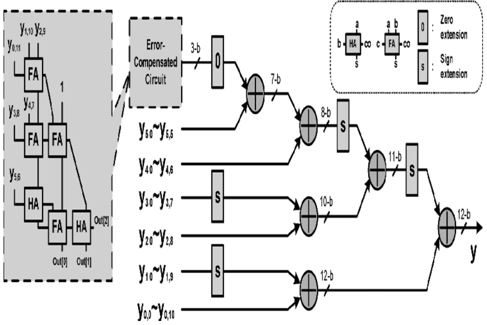

Fig. 2. Proposed ECAT architecture of shifting and addition operators for the (P,Q)=(12,6) example.

From Fig. 1, (3) can be approximated as

$Y \approx MP + \sigma . 2^{-(P-2)}$ …… (4)

where σ is the compensated bias from the TP to the MP

	Shift-add-add	SAT	Proposed ECAT
Area (gares)	236	406	463
Delay (ns)	10.8	3.72	3.89
Area×delay	100%	59.3%	70.7%
ϵ_{mse}	0.326	6.761	0.218

$\sigma = \text{Round}(TP_{major} + TP_{minor})$ …… (5)

where Round() is rounded to the nearest integer. The TP_{major} has more weight than TP_{minor} when contributing towards the σ. Therefore, the compensated bias σ can be calculated by obtaining Tp_{major} and estimating $TP_{minor.}$

B. *Performance Simulation for an Error-Compensated Circuit*

The ε, ε_{max}, and ε_{mse} are defined as follows:

$\varepsilon = \text{Avg} \{|TP - \sigma|\}$ …… (6)

$\varepsilon_{max} = \max \{|TP - \sigma|\}$ ……(7)

$\varepsilon_{mse} = \text{Avg} \{ (TP-\sigma)^2 \}$ …… (8)

where Avg is the average operator.

TABLE I
COMPARISONS OF ABSOLUTE AVERAGE ERROR ε, MAXIMUM ABSOLUTE ε_{max} ,ERROR , AND MEAN SQUARE ERROR ε_{mse}

Error	**(P,Q)**	**(12,3)** Case 1	**(12,6)** Case 3	**(12,9)** Case 2	**(12,12)** Case 2
ε	Direct-T	1.0625	2.5078	4.0010	5.5001
	Proposed	**0.2656**	**0.3789**	**0.3804**	**0.4738**
	Post-T	0.2500	0.2500	0.2500	0.2500
ε_{max}	Direct-T	2.1250	5.0156	8.0020	11.000
	Proposed	**0.6250**	**1.5000**	**2.0020**	**3.0000**
	Post-T	0.5000	0.5000	0.5000	0.5000
ε_{mse}	Direct-T	1.3516	6.7614	16.730	31.224
	Proposed	**0.1016**	**0.2184**	**0.2222**	**0.3472**
	Post-T	0.0859	0.0834	0.0833	0.0833

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TABLE II

COMPARISONS OF THE PROPOSED ECAT WITH OTHER ARCHITECTURES FOR A SIX 8-BIT WORDS EXAMPLE

C. Proposed ECAT Architecture

The proposed ECAT has the highest accuracy with a moderate area-delay product. The shift-and-add [2] method has the smallest area, but the overall computation time is equal to 10.8(=1.8×6) ns that is the longest. Similarly, the SAT[10], which truncates the TP and computes in parallel, takes 3.72 ns to complete the computation and uses 406 gates, which is the best area-delay product performance. However, for system accuracy, the SAT is the worst option shown in Table II. Therefore, the ECAT is suitable for high-speed and low-error applications.

IV. PROPOSED 8 × 8 2-D DCT CORE DESIGN

The 1-D DCT employs the DA-based architecture and the proposed ECAT to achieve a high-speed, small area, and low-error design. The 1-D 8-point DCT can be expressed as follows:

$$Z_n=(½)k_n \sum_{m=0}^{7} x_m\times\cos(((2m+1)n\pi)/16) \quad ……….(9)$$

Where x_m denotes the input data;Z_n denotes the transform output; the proposed 2-D DCT is designed using two 1-D DCT cores and one transpose buffer. For accuracy, the DA-precision and transpose buffer word lengths are chosen to be 9 bits and 12 bits, respectively, meaning that the system can meet the PSNR requirements outlined in previous works.Moreover, the 2-D DCT core accepts 9-bit image input and 12-bit output precision.

V. DISCUSSION AND COMPARISONS

Table IV compares the proposed 8 × 8 2-D DCT core with previous 2-D DCT cores. In [3] and [4], the SAT and AT architectures for DA-based DCTs improve the throughput rate of the NEDA method. However, DA-precision must be chosen as 13 bits to meet the system accuracy with more area overhead. The proposed DCT core uses low-error ECAT to achieve a high-speed design, and the DA-precision can be chosen as 9 bits to meet the PSNR requirements for reducing hardware costs. The proposed DCT core has the highest hardware efficiency, defined as follows (based on the accuracy required by the presented standards)

$$\text{Hardware Efficiency}(10^3 \text{ pels/s}) = \frac{\text{Throughput Rate}}{\text{GateCounts}} \quad ...... (10)$$

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TABLE III
COMPARISONS OF DIFFERENT 2-D DCT ARCHITECTURES WITH THE PROPOSED ARCHITECTURE

	Shams et al.[2]	Huang et al.[4]	**Proposed**
Architecture	NEDA	DA-based	DA-based
Technology	0.18µm	0.18µm	0.18µm
Multipliers/ROMs	0/0	0/0	0/0
Adders	92	50+16AT	46+16 ECAT
DA-precision	12 bits	13 bits	9 bits
Throughput Rate(pels/sec)	77M†	400 M	1G
Hardware Efficiency	3.42	10.05	45

†77MHz=1GHz/13

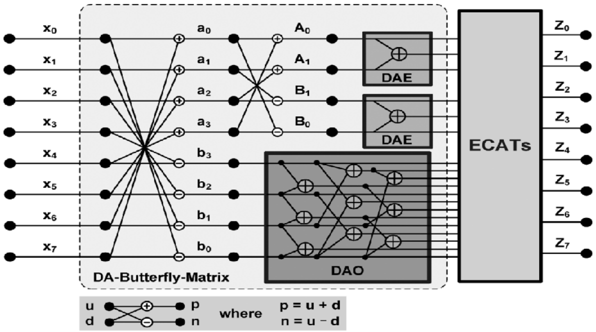
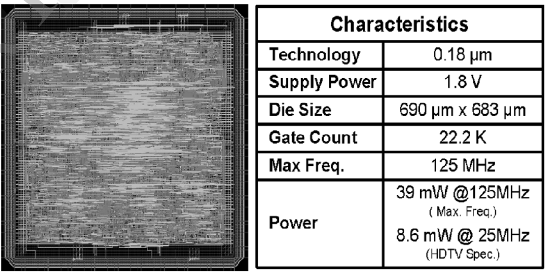


Fig. 3. Architecture of the proposed 1-D 8-point DCT



Characteristics	
Technology	0.18 µm
Supply Power	1.8 V
Die Size	690 µm x 683 µm
Gate Count	22.2 K
Max Freq.	125 MHz
Power	39 mW @125MHz (Max. Freq.) 8.6 mW @ 25MHz (HDTV Spec.)

Fig. 4. Core layout and characteristics

VI. CONCLUSION

In this brief, a high-speed and low-error 8 × 8 2-D DCT design with ECAT is proposed to improve the throughput rate significantly up to about 13 folds at high compression rates by operating the shifting and addition in parallel. Furthermore, the proposed error-compensated circuit alleviates the truncation error in ECAT. In this way, the DA-precision can be chosen as 9 bits instead of 12 bits so as to meet the PSNR requirements. Thus, the proposed DCT core has the highest hardware efficiency than those in previous works for the same PSNR requirements. Finally, an area-efficient 2-D DCT core is implemented using a TSMC 0.18-_m process, and the maximum throughput rate is 1 Gpels/s. In summary, the proposed architecture is suitable for high compression rate applications in VLSI designs.

ACKNOWLEDGEMENT

p. chinababu would like to thank Mr. p. Mahesh kumar Assistant professor of ECE department. Who had been guiding throughout the project and supporting me in giving technical ideas about the paper and motivating me to complete the work effectively and successfully.

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