Crosstalk Effects on Global Interconnects in Multi core Processors

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Abstract

One of the most harmful effects of noise on circuit operation is the degradation of signal integrity causing uncertainty in the signal delay. The uncertainty of the propagation delay of a signal can cause a catastrophic violation of the timing constraints within a system. For capacitively coupled interconnect lines, In this paper the effect of signal degradation for different interconnects lengths have been observed and simulations are done at 32nm and 45nm technology nodes.

1. Introduction

Due to continuous advances in technology scaling, modern integrated circuits consist of billions of transistors [1]. Traditionally, the operating speed of an integrated circuit had been assumed proportional to the speed of a logic gate. The interconnects between the gates were considered as ideal conductors that propagated signals instantaneously and had little effect on circuit operation. Such approximations are however no longer adequate, since the physical dimensions of interconnects have been greatly reduced while the operating speeds have increased. For example, in a modern 32 nm technology [2] the width and thickness of local wires are measured in only tens of nanometers, while the clock frequency is in the range of several GHz. Due to this scaling, the performance of interconnects is increasingly affected by their electrical parasitics, i.e. resistance, capacitance and inductance. These parasitics may result in long propagation delays for a signal travelling on interconnects or in signals that have been distorted by noise. The transmission of such a signal requires charging or discharging the wire capacitances which in turn consumes energy. This energy dissipated in the interconnect structure is projected to grow dramatically due to higher frequencies and increases in the number of metal layers [3]. For example, in [4] over 50% of the dynamic power consumption of a microprocessor was determined to be consumed by interconnects. In addition to transmitting data signals, on-chip wires are also used to distribute an operating voltage and the clock signal. The wires need to provide a constant operating voltage across the chip despite the increasing switching speeds and device count. The design of digital systems is further complicated by the fact that both wires and devices also suffer from process variations, i.e. their manufactured properties differ from the ideal designed values. Overall, due to these growing delay, signal integrity and energy issues in interconnects, there has been a shift of focus from devices to wires, or from computation to communication. This has resulted in a need for novel design tools and models that can be used to analyze and optimize on-chip interconnects

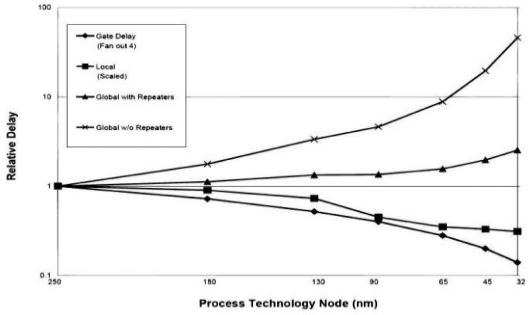

Figure 1. Delay for local (Metal 1) and global wiring versus feature size [3].

2. On-Chip Global Communication

The interconnects in an integrated circuit can be loosely divided into local, intermediate and global interconnects depending on their length, size and metal layer. An integrated circuit today often contains several large intellectual property (IP) blocks, such as memory, processing elements and interfaces. These IP blocks need to communicate with each other over long distances and they are linked by wide global interconnects that span at least one block or at most the length of the chip edge. While these global interconnects are routed in the top metal layers, the lower metal layers in turn are used by local narrow interconnects that connect

neighboring gates. The aforementioned scaling issues do not affect all interconnect types in an equal manner, as illustrated in Fig. 1. Unlike gate delays which are reduced as their dimensions become smaller, the delay of a fixed-length wire increases when its dimensions are scaled [5]. For local wires this delay increase is alleviated by the fact that their length is reduced with scaling since they need to connect nearby gates whose sizes diminish with scaling. However, the length of global wires is not scaled with technology since they may need to run across the chip. This has resulted in a growing delay gap between gates and global interconnects. Despite such efforts as increased aspect ratios, low-resistivity wire materials like copper, and low-k (permittivity) dielectric, global signaling often remains a major bottleneck in modern integrated circuits. In order to provide a high bandwidth, on-chip communication links are normally constructed of multiple wires. Among common communication architectures are point-to-point links, buses and a network-on-chip (NoC) [6, 7, and 8].

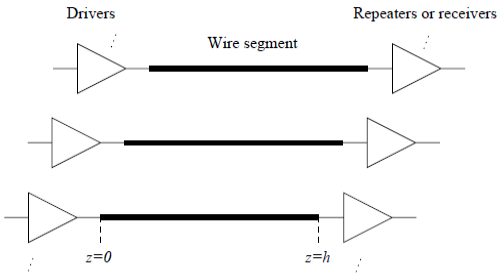

Figure .2: An on-chip communication link consisting of multiple parallel wires.

In practice, buses are often implemented using techniques such as bus splitting [9] to reduce the total wire load. NoC links on the other hand are typically modular and structured interconnects running between routers. In addition, because of delay and signal integrity issues interconnects are commonly broken with repeaters [10] into segments. Therefore, in the physical level the communication often reduces to multiple wires running in parallel. In this paper, the focus is on long, multiple parallel wires that typically form a part of a communication link as depicted in Fig. 2. A common way to implement a long on-chip communication link is by using voltage-mode signaling with buffering. The delay of an RC interconnects increases quadratically with length since both resistance and capacitance increase linearly with wire length. The basic principle behind buffering is to reduce this delay increase to linear by inserting repeaters along the wire. The total delay then becomes equal to the number of wire segments multiplied by the individual segment delay. In addition to delay reduction, buffering can be used to reduce noise. In order to achieve the desired objective, the repeaters need to be both spaced and sized appropriately. In addition to the common voltage mode signaling, other signaling techniques for global on-chip communication have also been proposed. These include e.g. encoded, current-mode, and differential signaling. The objective is typically to enhance signaling speed, power dissipation, signal integrity or a combination of these. Bus encoding uses additional bus wires and encoding and decoding logic to alter the signals to be transmitted on a bus. The encoding is used to avoid certain bit patterns that would result in high noise, delay or power. On the other hand, in differential signaling, a signal is transmitted over a pair of wires where the second wire is carrying the complement of the original signal. A differential signal acts as its own receiver reference and offers improved noise immunity by rejecting common mode noise. The signal swing is also effectively doubled, thus increasing noise margins and improving speed as the rise and fall times at the receiver are reduced [11]. In voltage-mode signaling, the interconnects need to be fully charged to propagate a signal. This is avoided in current modesignaling, where the interconnects are terminated with a resistor. Because of the resistive termination, there is a current flow that the receiver detects to determine the transmitted logic value. It has been shown that for high data rates current sensing can be very speed and power efficient in comparison to voltage sensing [12]. there are also emerging on-chip interconnect paradigms such as carbon nanotubes [13, 14], optical [15] and RF communications [16]. These interconnects however have several issues that need to be resolved before they can be used in on-chip communication,

3. Interconnect Delay

Interconnect delay is a primary design criterion due to the close relationship to the speed of a circuit. Early interconnect design methodologies [19, 20] focused primarily on delay optimization. A typical data path in a synchronous digital circuit is shown in Fig. 3. In the case of zero clock skew, the minimum allowable clock period is [21]

$$T_{p\_min} = T_{C\text{-}Q} + T_{int} + T_{logic\_max} + T_{setup} \qquad (1)$$

where $T_{C\text{-}Q}$ is the time required for the data to leave the initial register after the clock signal arrives, T_{int} is the interconnect delay, T_{logic_max} is the maximum logic gate delay, and T_{setup} is the required setup time of the receiving register. From (1), by reducing Tint, the clock period can be decreased,

increasing the overall clock frequency of the circuit (assuming the data path is a critical path).

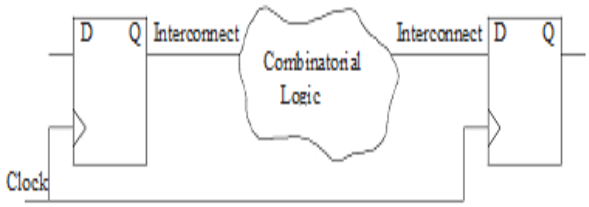

Figure .3. A data path in a synchronous digital system.

In advanced microprocessors, multiple computational cores can be fabricated on the same die [5]. Communication among these cores and on-chip memories generally requires multiple clock cycles. Sometimes the computational core enters an idle state waiting for the required data or control signals from other regions of the IC. The computational resource of these cores, therefore, cannot be efficiently utilized due to the large amount of multi-cycle communication. By reducing the interconnect delay, the speed of the system, i.e., the computational efficiency of the cores, can be improved at the architecture level.

4. Results

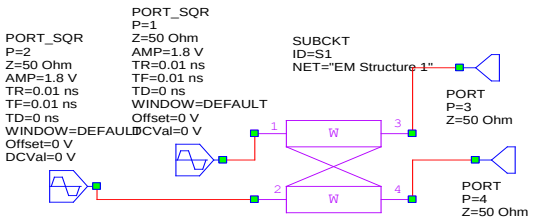

Fig.4.Experimental setup

Figure.4.describes circuit simulation setup for the interconnects in AWR software.Figure.5.reprents the top model of interconnect.

Fig.5. Top model of Interconnect lines

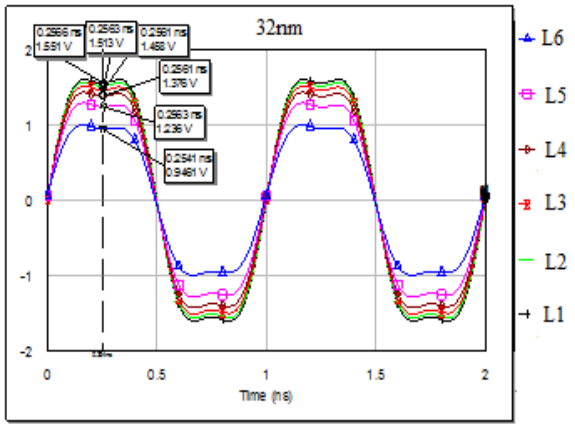

Fig.6. Output voltage waveforms for 32nm Technology

Figure.6. describes output signal degradation with increase in interconnect lengths of 1mm,2mm,3mm,4mm,5mm and 6mm at 32nm Technology

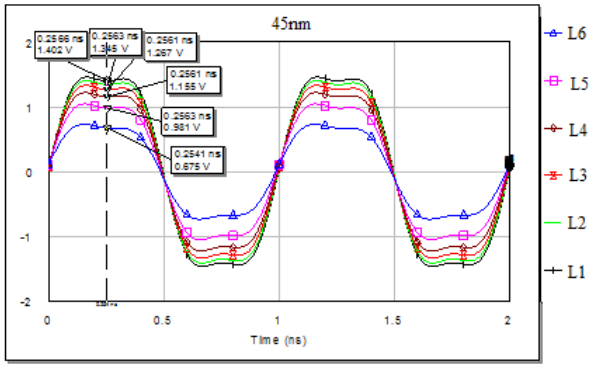

Fig.7. Output voltage waveforms for 45nm Technology

Figure.7. describes output signal degradation with increase in interconnect lengths of 1mm,2mm,3mm,4mm,5mm and 6mm at 45nm Technology

5. Conclusion

Crosstalk, caused by EM coupling between multiple transmission lines running parallel. It can cause noise pick up on the adjacent quiet signal lines that may lead to false logic switching. Crosstalk will also impact the timing on the active lines if multiple lines are switching simultaneously. Depending on the switching direction on each line the extra delay introduced may significantly increase/decrease the sampling window. The amount of crosstalk is related to the signal rise time, to the spacing between the lines, and to how long these multiple lines run parallel to each other.

6. References

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