

# Cross layer Optimization of Optical Node in High Speed Network

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**Abstract**— Optical switching system based on packet switching referred as Optical Packet Switching is considered as next generation high speed data transfer technology. In OPS, the design of an efficient optical node is a complex problem. Performance evaluation of the switches (Optical nodes) is done both at physical as well as network layer. Parameter like packet loss probability is used to measure performance of the switch in network layer. For efficient switching high throughput is desired therefore low packet loss probability is to be achieved. In the physical layer, effects of system impairments on bit-error rate (BER) are studied. Physical layer impairments are dominated by amplified spontaneous emission (ASE) noise and crosstalk, which also leads to packet drop. In this paper, cross-layer optimization of an AWG based optical packets switch is done. The detailed analysis shows that the architecture presented here can be operated in the sub-micro watts with very good quality of service in terms of packet loss rate (PLR).

**Keywords**—BER; OPS; PLR; ASE; Optical Node

## I. INTRODUCTION

OPS is a transmission technology which utilizes the huge transmission bandwidth of optical fiber very efficiently using WDM technology. In OPS, data is transmitted in forms of packets which are transmitted optically [1]. Each packet is composed of header and payload. Header is processed electronically after O/E conversion at each node while payload remains in optical domain [2]. As header is processed at each intermediate node, it is send at lower data rates. Header contains meaningful information like: source address, destination address etc.

Currently, in optical transport networks, first light-path paths are set, then data travels over it[1-4]. These all-optical switches are transparent to information carried over the light path. At the same time, optical circuit switching technology has made it feasible to have virtual topologies over an actual physical fiber topology (layout). It allows us to rapidly deliver the enormous bandwidth of WDM networks to customer, while remaining inefficient at the physical layer. One requires packet for efficient use of the physical layer. The possibility of packet switching using photonic technologies allows all-optical packet switched networks where packets remain in optical form without undergoing optoelectronic conversion at intermediate nodes [5-8]. The design of the OPS network is shown in Fig. 1.

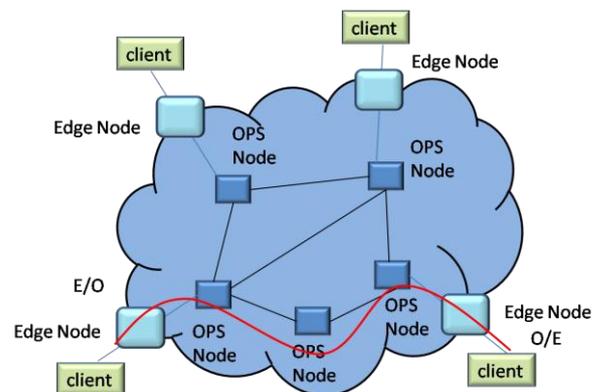


Fig. 1. Optical Packet Switching Network Full layout

The all-optical packet switches placed in the core network as shown in figure 2, processes the packets and converts the header of the packet to electrical form and maintains the payload in optical form. The header information is used for routing of the packet. Once the packet reaches the egress node, the aggregated optical packets can be separated optically (if required) and directed towards the client network. We can call them as aggregate core transport networks.

## II. SWITCH DESIGN AND POWER BUDGET ANALYSIS

The design of optical node is shown in Fig. 2. Switch size is assumed to be  $N \times N$ , with ' $m$ ' buffer modules [9]. Here, TWC placed at the input of the switch plays major role as it tunes the wavelength of the incoming packets such that either they can be placed in any buffer ( $1, \dots, m$ ) depending on the required amount of delay, or can be send to the output of the scheduling AWG, from here packets can be transferred to actual output by tuning their wavelengths using the TWC placed at the input of the switching AWG. The detailed description and advantages of the architecture can be found in [9-10]. The switch design very efficiently uses the wavelength domain routing pattern of the AWG. In the paper design proposed in [9] is modified by placing SOA just after scheduling AWG so that the loss of both buffered as well as direct packets can be compensated.

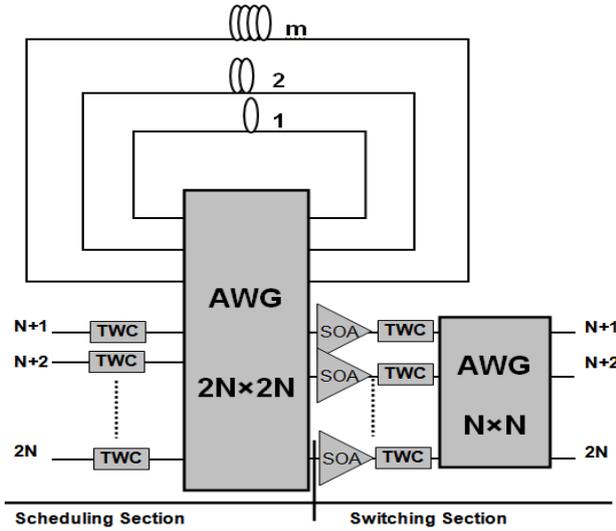


Fig. 2. WDM based AWG Optical Router

### A. Loss Analysis

The loss of input unit is

$$A_m = L_{TWC} \quad (1)$$

The loss of buffer is

$$A_b = L_{AWG}^{2N \times 2N} L_{FDL} \quad (2)$$

Here,  $L_{AWG}^{2N \times 2N}$  is loss due to scheduling AWG.  $L_{FDL}$  is the loss due to the fiber delay lines.

Similarly the loss of output unit is

$$A_{out} = L_{AWG}^{2N \times 2N} L_{TWC} L_{AWG}^{N \times N} \quad (3)$$

By combing all the above losses, total loss of the switch is

$$A_T = A_m A_b A_{out} \quad (4)$$

To fully compensate the loss, the gain of the SOA placed at the input of the switching AWG must satisfy  $A_m A_b A_{out} G = 1$ .

### B. Power Analysis

In the sub-section power analysis is presented. Power entering the switch for bit  $b$  is

$$P_s = bP_{in} \quad b \in [0, 1] \quad (5)$$

The extinction ratio ( $\epsilon = P_0/P_1$ ) is assumed to be zero.

Power at the output of the switch is

$$P_{out} = P_{in} + n_{sp} (G_3 - 1) h\nu B_0 \frac{A_{out}}{L_{AWG}^{2N \times 2N}} \quad (6)$$

### C. Noise Analysis

The information in optical domain suffers from various noise sources. These noises terms beat with each other to produce shot noise, ASE-ASE beat noise, sig-ASE beat noise, shot-ASE beat noise and thermal noise variances are denoted by  $\sigma_s^2$ ,  $\sigma_{sp-sp}^2$ ,  $\sigma_{sig-sp}^2$ ,  $\sigma_{s-sp}^2$ , and  $\sigma_{th}^2$  respectively [11]. Various noise components are defined as

Shot noise

$$\sigma_s^2 = 2qRPB_e \quad (7)$$

ASE-ASE beat noise

$$\sigma_{sp-sp}^2 = 2R^2 P_{sp} (2B_o - B_e) \frac{B_e}{B_0^2} \quad (8)$$

Sig-ASE beat noise

$$\sigma_{sig-sp}^2 = 4R^2 P \frac{P_{sp} B_e}{B_0} \quad (9)$$

Shot-ASE beat noise

$$\sigma_{s-sp}^2 = 2qRP_{sp} B_e \quad (10)$$

Thermal noise

$$\sigma_{th}^2 = \frac{4K_B T B_e}{R_L} \quad (11)$$

The expression for  $P$  and  $P_{sp}$  will be given by

$$P = bP_{in},$$

$$P_{sp} = n_{sp} (G_3 - 1) h\nu B_0 \frac{A_{out}}{L_{AWG}^{2N \times 2N}} \quad (12)$$

The total noise variance for bit  $b$  is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sp-sig}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2 \quad (13)$$

$$BER = Q\left(\frac{I(1) - I(0)}{\sigma(1) + \sigma(0)}\right) = Q\left(\frac{RP(1) - RP(0)}{\sigma(1) + \sigma(0)}\right) \quad (14)$$

$$Q(z) = \frac{1}{\sqrt{2\pi}} \int_z^\infty e^{-\frac{z^2}{2}} dz \quad (15)$$

The equation 14 will provide the BER at different power levels, which is an important parameter in physical layer analysis. In the next subsection- network layer parameter packet loss probability will be obtained using the computer simulation.

TABLE I. LIST OF PARAMETRES USED IN CALCULATION

Symbol	Parameter	Value
$N$	Size of the switch	16
$n_{sp}$	Population inversion factor	1.2
$c$	Speed of light	$3 \times 10^8 \text{ m/s}$
$N$	Refractive index of fiber	1.55
$R$	Responsively	1.28 A/W
$e$	Electronic charge	$1.6 \times 10^{-19} \text{ C}$
$B_e$	Electrical bandwidth	20GHz
$B_0$	Optical bandwidth	40GHz
$L_{TWC}$	TWC insertion loss	2.0 dB
$L_{AWG}^{2N \times 2N}$ $L_{AWG}^{N \times N}$	Loss of Scheduling and Switching AWG (32 channels)	3.0 dB
$L_{FDL}$	Loss of the fiber loop	0.2 dB/km

#### D. Simulation Analysis

The simulation is done in MATLAB. In the simulation, for traffic generation and destination assignment random traffic model is considered. In the random traffic model, it is assumed:

1. Packet can arrive to any of the input of switch with equal probability  $p$ .
2. Each packet has equal probability ( $1/N$ ) to go to any of the output, where  $N$  is the number of output of the switch.

The probability of arrival of that  $K$  packets for a particular tagged output is given by

$$P[K] = {}^N C_K \left(\frac{p}{N}\right)^K \left(1 - \frac{p}{N}\right)^{N-K} \quad (16)$$

It must be remembered that module  $m$  provides a delay of  $m$  slots.

### III. RESULTS AND CROSS LAYER OPTIMIZATION

In this section physical layer results are presented. The length of the fiber loop is taken equal to the packet duration equivalent of slot duration and is given by

$$L = cb / nB_r \quad (17)$$

Here,  $c$  ( $=3 \times 10^8 \text{ m/s}$ ) is the speed of light,  $b$  is the total number of bits stored in fiber delay lines,  $n$  ( $=1.55$ ) is the refractive index and  $B_r$  is the bit rate.

#### A. Power Budget Analysis Results

TABLE II. BER ANALYSIS AT VARIOUS POWER LEVELS FOR SWITCH SIZE  $N=16$ , BUFFER=16 AND PACKET SIZE OF 1000 BITS

Power $\mu\text{W}$	BER		
	$B_r=10 \text{ Gbps}$	$B_r=20 \text{ Gbps}$	$B_r=40 \text{ Gbps}$
0.6	$9.6175 \times 10^{-4}$	$9.2421 \times 10^{-4}$	$9.0591 \times 10^{-4}$
1	$1.7166 \times 10^{-5}$	$1.6066 \times 10^{-5}$	$1.5540 \times 10^{-5}$
2	$8.4966 \times 10^{-10}$	$7.4348 \times 10^{-10}$	$6.9524 \times 10^{-10}$
3	$4.4044 \times 10^{-14}$	$3.6002 \times 10^{-14}$	$3.2534 \times 10^{-14}$
4	$2.2980 \times 10^{-18}$	$1.7540 \times 10^{-18}$	$1.5314 \times 10^{-18}$
5	$1.1969 \times 10^{-22}$	$8.5287 \times 10^{-23}$	$7.1930 \times 10^{-23}$
6	$6.2099 \times 10^{-27}$	$4.1298 \times 10^{-27}$	$3.3643 \times 10^{-27}$
7	$3.2074 \times 10^{-31}$	$1.9906 \times 10^{-31}$	$1.5662 \times 10^{-31}$
8	$1.6493 \times 10^{-36}$	$9.5510 \times 10^{-36}$	$7.2579 \times 10^{-36}$
9	$8.4454 \times 10^{-40}$	$4.5630 \times 10^{-40}$	$3.3487 \times 10^{-40}$
10	$4.3076 \times 10^{-44}$	$2.1713 \times 10^{-44}$	$1.5388 \times 10^{-44}$

In above table II results are tabulated for buffer size 16 and for different lengths of packets or time slots. Bit rate 10 Gbps, 20 Gbps, 40 Gbps correspond to length of 19.3 m, 9.67 m, 4.83 m respectively. Considering loss of fiber to be 0.2 dB/Km, the amount of loss will be very less. Hence, with above table II, it can be concluded that power level of  $2 \mu\text{W}$  will be sufficient for the proper operation of the switch ( $\text{BER} \leq 10^{-9}$ ). Considering power of  $2 \mu\text{W}$  if the data rate is increased from 10 Gbps to 20 Gbps and 40 Gbps there is reduction in BER. Thus as slot length decreases BER improves.

TABLE III. BER ANALYSIS AT VARIOUS POWER LEVELS FOR SWITCH SIZE  $N=16$ , BUFFER=16 AND PACKET SIZE OF 10000 BITS

Power $\mu\text{W}$	BER		
	$B_r=10 \text{ Gbps}$	$B_r=20 \text{ Gbps}$	$B_r=40 \text{ Gbps}$
0.6	0.0019	0.0013	0.0011
1	$5.2698 \times 10^{-5}$	$2.8719 \times 10^{-5}$	$2.0885 \times 10^{-5}$
2	$8.1129 \times 10^{-9}$	$2.3953 \times 10^{-9}$	$1.2614 \times 10^{-9}$
3	$1.3260 \times 10^{-12}$	$2.1056 \times 10^{-13}$	$7.9986 \times 10^{-14}$
4	$2.1970 \times 10^{-16}$	$1.8691 \times 10^{-17}$	$5.1113 \times 10^{-18}$
5	$3.6505 \times 10^{-20}$	$1.6598 \times 10^{-21}$	$3.2633 \times 10^{-22}$
6	$6.0613 \times 10^{-24}$	$1.4703 \times 10^{-25}$	$2.0764 \times 10^{-26}$
7	$1.0044 \times 10^{-27}$	$1.2982 \times 10^{-29}$	$1.3159 \times 10^{-30}$
8	$1.6602 \times 10^{-31}$	$1.1421 \times 10^{-33}$	$8.3053 \times 10^{-35}$
9	$2.7370 \times 10^{-35}$	$1.0013 \times 10^{-37}$	$5.2213 \times 10^{-39}$
10	$4.5005 \times 10^{-39}$	$8.7502 \times 10^{-42}$	$3.2704 \times 10^{-43}$

In table III results are again reproduced using packet size of 10000 bits rest of parameters are same as in table II. The slot length is increased due to increase in the number of bits and correspondingly buffer length increases, thus more power is required to maintain  $\text{BER} \leq 10^{-9}$ . In above table the results are plotted for Bit rate 10 Gbps, 20 Gbps, 40 Gbps correspond to length of fiber as 193 m, 96.7 m, 48.3 m respectively and again a power level of  $3 \mu\text{W}$  will be required for the switch to operate properly. Thus increasing slot length by a factor of 10 the power required to achieve acceptable signal quality increases by  $1 \mu\text{W}$ .

**B. Simulation Results**

In this section, network layer results in terms of packet loss probability are presented. Simulation is done on MATLAB and to obtain steady state results simulation is repeated for  $10^6$  runs.

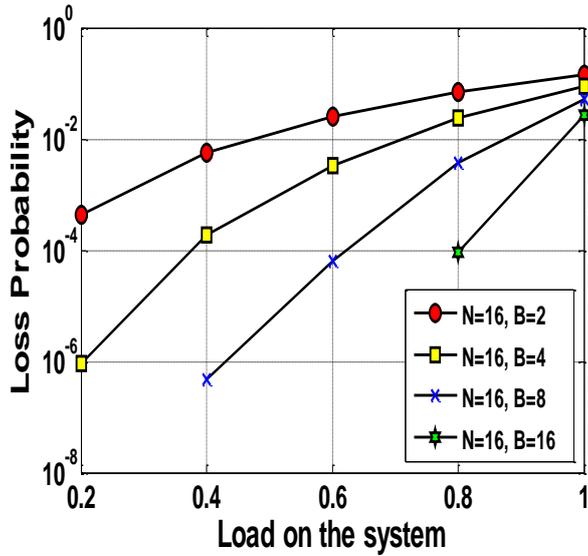


Fig. 3: Packet loss probability vs. load (Random Traffic) with varying number of buffer module

In figure 3, switch of size  $N = 16$  and buffer is varying from 2 to 16 is considered. It is clear from the figure that if no of inputs are 16 then to achieve very low packet loss probability of order  $10^{-4}$  at higher load (0.6) buffer modules required are at least 8 or above. If number of modules are decreased to 4 or 2 packets loss increases. At load of 0.6 with  $B=4$ , loss probability is approximately  $10^{-3}$ . If traffic load on switch is further increased to 0.8 then required buffer size is at least 16 to achieve low packet loss. The switch performs well in terms of the packet loss probability as we are able to achieve low packet loss probability. It is also observable form the figure as the number of buffer modules increases, the packet loss probability also improves.

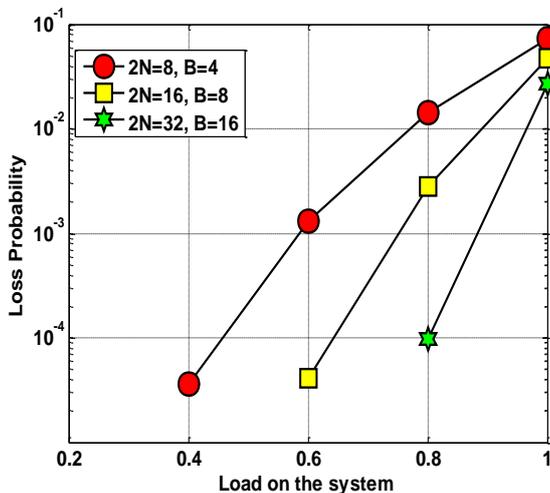


Fig. 4: Packet loss probability vs. load (Random Traffic) for  $N=B$

In figure 4 plots are obtained for various cases of scaled switch architecture with  $N=B$ . If total number of inputs of scheduling AWG is  $2N= 32$  then for the case of  $N=B$  half of the ports used as input and rest half as buffer. Considering the case of  $N=B=4$  and  $N=B=16$ , even at the load of 0.8, the packet loss improvement is more than 100. Thus it is evident from figure that as switch size and buffer is increased while keeping their ratio constant, packet loss probability decreases.

**C. Cross Layer Optimization**

The schema of cross layer optimization is shown below in figure 5; here it is shown that for desired packet loss, how switch buffer and power will be fixed for a particular switch size.

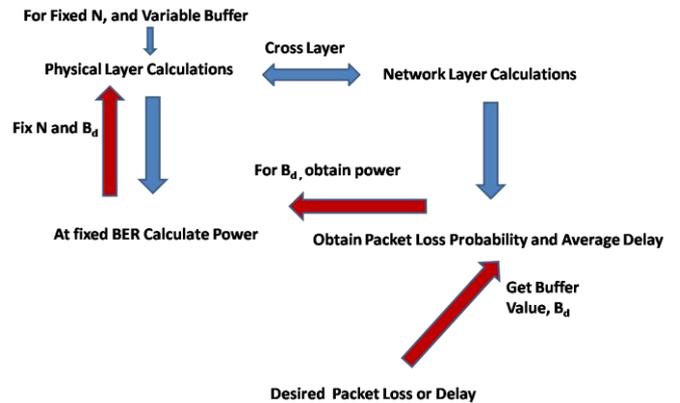


Fig. 5: Flow diagram for Cross layer optimization

Let for a particular application the desired packet loss for switch of size  $N=16$  is  $10^{-4}$  at the load of 0.8. First of all consider figure 4, where packet loss for  $N=16$  for different buffer space is shown. Thus as per the requirement the minimum buffer to be considered is 16. Now we have fixed our design parameters for the switch which are  $N=16$  and  $B=16$ . Referring Table II, the desired power would be  $2\mu W$ . The length of the packet will of 1000 bits and maximum data transmission speed is 40 Gbps. Similarly if packet of 10,000 is to be used than required power is  $3\mu W$ .

**IV. CONCLUSIONS**

This paper presents the cross layer optimization of an AWG based switch. The cross layer optimization is performed between the physical and network layers. This analysis is very important when switches are cascaded or placed in the network. It is shown that to get desired quality of service, a particular switch design is needed with some minimum amount of power. In general switch size is fixed thus this analysis fix the buffer size, packet size at different bit rates and required amount of power for the correct reception of the signal at the output.

## REFERENCES

- [1] D. K. Hunter and I. Andonovic, "Approaches to Optical Internet Packet Switching," *IEEE Communications Magazine*, vol. 38(9), pp. 116-122, September 2000.
- [2] S. Yao, B. Mukherjee, and S. Dixit, "Advances in Photonic Packet Switching: an Overview," *IEEE Communications Magazine*, vol. 38(2), pp. 84-94, February 2000.
- [3] F. Callegati, G. Corazza, and C. Raffaelli, "Design of a WDM Optical Packet Switch for IP Traffic," in Global Telecommunications Conference, 2000. *GLOBECOM '00*, 2000, vol. 2, pp. 1283-1287.
- [4] R. S. Tucker and W.D. Zhong., "Photonic packet switching: an overview," *IEICE Trans. Commun.*, vol. E82 B, pp. 254-264, Feb. 1999.
- [5] M. Chia et al., "Packet loss and delay performance of feedback and feed-forward arrayed-waveguide gratings-based optical packet switch with WDM inputs-outputs," *J. Lightw. Technol.*, vol. 19, no. 9, pp. 1241-1254, Sep. 2001.
- [6] R. K. Singh, R. Srivastava and Y. N. Singh, "Wavelength division multiplexed loop buffer memory based optical packet switch," *Optical and Quantum Electronics*, vol. 39, no. 1 pp. 15-34, Jan. 2007.
- [7] A. Pattavina, "Multi-wavelength switching in IP optical nodes adopting different buffering strategies," *Optical Switching and Networking*, vol. 1, no. 1 pp. 65-75, Jan. 2005.
- [8] D. K. Hunter, et.al., "WASPNET: A wavelength switched packet network," *IEEE Commun. Magazine*, vol. 37, no. 3, pp. 120-129, Mar. 1999.
- [9] Rajiv Srivastava and Yatindra Nath Singh, "Feedback Fiber Delay Lines and AWG Based Optical Packet Switch Architecture," *Journal of Optical Switching and Networking*, volume 7, Issue 2, April 2010, Pages 75-84.
- [10] R. Srivastava, R. K. Singh and Y. N. Singh, "All optical reflectors based WDM Optical Packet Switch," Indian Patent office, patent application no. 2707/DEL/2007 (patent granted).
- [11] R. Srivastava, R. K. Singh and Y. N. Singh, "Design Analysis of Optical Loop Memory," *J. Lightw. Technol.* vol.27, no. 21, pp.4821-4831, Nov.2009.