Critical Load Protection by using DSTATCOM with Stiff Source

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***Abstract*—A novel control design algorithm based DSTATCOM control has been proposed in this paper. DSTATCOM can't be used to protect the loads that are connected to the stiff source from voltage disturbances. This algorithm based DSTATCOM operated in voltage control mode. In voltage control mode the voltage regulation will be quite faster, it protects the critical loads and mitigates voltage and current related power quality issues. Thus with these factors, this scheme allows the compensator to tackle quality issues, THD, UPF and voltage regulation. SIMULINK/MATLAB results are presented.**

Keywords*—Voltage control mode, stiff source, DSTATCOM, Power Quality, voltage regulation, Current control mode, Voltage source Inverter.

I. INTRODUCTION

Now-a-days the distribution system suffers from both voltage and current related power quality (PQ) problems. They are low power factor, disturbed source current, voltage distortions and harmonics [1], [2]. The custom power devices are used to mitigate these PQ problems. Depending on the mode of operation A DSTATCOM can mitigate the several power quality problems. A DSTATCOM is connected to the system at Point of common coupling (PCC) is used to mitigate both current and voltage related PQ problems [2]-[5]. In current control mode, the compensator injects harmonic and reactive components of load currents to form balanced and sinusoidal source currents and these currents should be in phase with PCC voltages [3]-[5]. While operating in voltage control mode (VCM), the compensator regulates the voltages to reference value to save the load from voltage disturbances as sag and swell. However both advantages cannot be achieved with one device, as both of them are independent of each other.

A source is termed as stiff or non-stiff is based on the distance between the source and the load. The source is termed as stiff source when the distance between the source and the load is very small and has negligible feeder impedance, and the source is termed as non-stiff source when the distance between the source and the load is long and has higher feeder impedance.

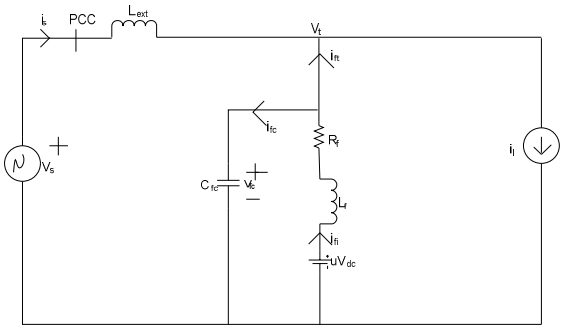

Fig (1): Single-phase equivalent circuit of DSTATCOM.

In current control mode, the compensator cannot compensate for the disturbances caused by voltage. Therefore CCM cannot be used for voltage disturbances, which is a main drawback of this CCM operation [13]. By indirectly regulating the voltage across the external inductor DSTATCOM provides voltage regulation. During normal operation, the control algorithm makes source currents balanced, sinusoidal and in phase with respective source voltages. During voltage disturbances, a constant voltage is maintained at the load terminal

This paper considers the DSTATCOM to operate in VCM and uses a novel algorithm to obtain variable reference load voltage as a function of the desired source current. This novel algorithm achieves both the advantages of VCM and CCM with only working in one mode of operation. The performance of this scheme is compared with the conventional method. At nominal load operation, UPF is obtained. Fast voltage regulation is obtained during voltage unbalances. The effectiveness of this novel algorithm is validated by simulation results.

II. DESCRIPTION OF THE EQUIVALENT CIRCUIT

The source Vs and the load i_l are connected through the external inductor L_{ext} at point of common coupling. i_s is the source current. Through the LC filter VSI (voltage source converter) which is represented as uV_{dc} is connected to the load. Where

V_{dc} is the voltage maintained across each capacitor And u is the control variable.

Depending upon the switching state the control variable can be +1 or -1

The currents through the VSI, DSTATCOM AND C_{fc} are $i_{fi}, i_{ft} and i_{fc}$ and the source and the load voltages are $v_s and v_t$ respectively.

There will be no importance of external impedance under normal operation where as under disturbances by the amount of the sag to be mitigated and the rating of the DSTATCOM the value of the external impedance is decided and the source current is

$$\bar{I}_s = \frac{V_S \angle 0 - V_t \angle -\delta}{R_{ext} + jX_{ext}}$$

For a practical case $X_{ext} \succ\succ R_{ext}$ .when δ is minimum then the reactive source current is maximum, for this the source current will supply only losses so the δ will be minimum.

$$I_m\left[\bar{I}_s\right] = \frac{V_t - V_S}{X_{ext}}$$

The aim is to protect the critical loads during voltage disturbances by improving the DSTATCOM capability to mitigate the sag. To protect the load, the voltage during the voltage sag is 0.9pu is sufficient. Assuming the reactive current is 20A and the sag is 40% then the value of external inductor will be

$$X_{ext} = \frac{0.9 - 0.6}{20} \times 230 = 3.45\Omega$$

III. CONTROL SCHEME

DSTATCOM -compensated circuit diagram is shown in Fig.1.shows the equivalent single phase representation of DSTATCOM in a distribution network. Variable u is either +1 or -1 depending upon switching state is a switching function. High switching frequency components are eliminated by shunt capacitance C_{fc} .

Initially, discrete system modeling is carried out to determine discrete voltage control law. With properly chosen VSI parameters the voltage is regulated so the procedure to design the VSI parameters is described. By using complex Fourier transformations and theory of instantaneous symmetrical component, a magnitude of reference voltage is generated which makes the advantages of CCM at nominal load. The controller block diagram is shown in Fig.2.

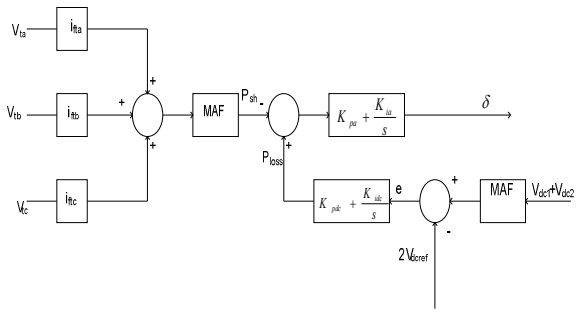

Fig (2) controller circuit

A. COMPUTATION OF REFERENCE VOLTAGE MAGNITUDE(V^*_t):

The advantages provided by the CCM operation are:

Source currents are balanced and
Sinusoidal
Unity power factor at PCC
Source supplies load average power
and VSI losses

Load voltage must be regulated to achieve the above advantages during the normal operation.

Load voltages are balanced and sinusoidal by using DSTATCOM but contains some switching harmonics which gives unwanted reference source currents when directly used. To compute the reference source currents, the +ve sequence components of load voltages are extracted they are:

$$i_{sa}{}^* = \frac{v^+_{ta1}}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)$$

$$i_{sb}{}^* = \frac{v^+_{tb1}}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)$$

$$i_{sc}{}^* = \frac{v^+_{tc1}}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)$$

Where $\Delta^+_1 = \sum_{j=a,b,c}\left(v^+_{tj1}\right)^2$ and P_{lavg} is the average load power which can be calculated by using the moving average filter(MAF) and P_{loss} is the total power loss which can be calculated by passing the error that is developed by comparing the average dc link voltage (Vdc1+Vdc2) and predefined reference value (2Vdcref) through a PI controller.

$$P_{loss} = K_{pdc}e + K_{idc}\int edt$$

Where K_{pdc} proportional gain

K_{idc} integral gain

e is the error of the PI controller i.e

$$e = 2V_{dcref} - \left(V_{dc1} + V_{dc2}\right)$$

Once the reference currents are drawn from the source then the reference voltages at the load terminal can be derived.

By applying the kirchhoffs law to fig (1)

$$\bar{V}_s = \bar{I}_s Z_{ext} + V_t$$

For the UPF operation, the source voltage and source current will be in phase

$$V_s = I_s\left(R_{ext} + jX_{ext}\right) + V_t$$

The load voltage is:

$$\left(V_s - I_s R_{ext}\right) - jI_s X_{ext} = V_t$$

$$V_t^2 = \left(V_s - I_s R_{ext}\right)^2 + \left(I_s X_{ext}\right)^2$$

$$V_t = \sqrt{\left(V_s - I_s R_{ext}\right)^2 + \left(I_s X_{ext}\right)^2}$$

The value of V_t lies between 0.9pu and 1.1pu based on standards and the advantages of CCM operation are achieved. V_t is controlled by source current. The load voltage magnitude lies between 0.9pu and 1.1pu during sag and 1.1pu and 1.8pu

during swell. For satisfactory operation maximize the DSTATCOM disturbance with standard ability while keeping the load voltage at safe limits i.e.

$V_t = 0.9\,pu$ when there is a sag

$V_t = 1.1\,pu$ when there is a swell

B. Computation of load angle:

From the block diagram of controller circuit P_{sh} is calculated by using MAF and P_{loss} is calculated by using PI controller. By comparing shunt power and power loss an error is developed which is passed through the PI controller to compute δ

$$\delta = K_{pa}\left(P_{loss} - P_{sh}\right) + K_{ia}\int\left(P_{loss} - P_{sh}\right)dt$$ where

$$P_{sh} = \frac{1}{T}\int_{t_1}^{t_1+T}\left(V_{ta}i_{fta} + V_{tb}i_{ftb} + V_{tc}i_{ftc}\right)dt$$

Power flows from DSTATCOM to load when P_{sh} is positive and power flows from load to DSTATCOM when P_{sh} is negative. By taking power from source the VSI losses are compensated in steady state so P_{sh} will be negative in steady state.

In steady state the capacitor voltage decreases from reference value it represents losses in VSI so P_{loss} will be negative in steady state.

The difference of P_{sh} and P_{loss} be minimized when P_{sh} and P_{loss} are equal.

C. INSTANTANEOUS REFERENCE VOLTAGE:

The three phase reference voltages are taken by selecting the suitable reference load voltage magnitude and computing load angle

$$V_{trefa} = \sqrt{2}V_t^* \sin(\omega t - \delta)$$

$$V_{trefb} = \sqrt{2}V_t^* \sin\left(\omega t - \frac{2\pi}{3} - \delta\right)$$

$$V_{trefc} = \sqrt{2}V_t^* \sin\left(\omega t + \frac{2\pi}{3} - \delta\right)$$

Where ω is the system frequency

D.GENERATION OF SWITCHING PULSES:

The state-space representations of the single-phase equivalent circuit shown in Fig 1 are given by:

$$\dot{x} = Ax + Bz \quad \ldots\ldots\ldots\ldots\ldots\ldots(1)$$

Where,

$$A = \begin{bmatrix} 0 & \frac{1}{C_{fc}} \\ \frac{-1}{L_f} & \frac{-R_f}{L_f} \end{bmatrix}$$

$$B = \begin{bmatrix} 0 & \frac{-1}{C_{fc}} \\ \frac{V_{dc}}{L_f} & 0 \end{bmatrix}$$

$$x = \begin{bmatrix} v_{fc} & i_{fi} \end{bmatrix}^t \qquad z = \begin{bmatrix} u & i_{ft} \end{bmatrix}^t$$

To compute the state vector $x(t)$ with known initial value $x(t_0)$, the general time domain solution of (1) is given by:

$$x(t) = e^{A(t-t_0)}x(t_0) + \int_{t_0}^{t} e^{A(t-T)}Bz(T)\,dT \qquad \ldots(2)$$

The continuous discrete solution is acquired by replacing $t_0 = kT_d$ and $t = (k+1)T_d$ as follows:

$$x(k+1) = e^{ATd}x(k) + \int_{kT_d}^{T_d+kT_d} e^{A(T_d+kT_d-T)}Bz(T)\,dT \quad \ldots\ldots(3)$$

where, k represents the sample and

T_d represents the sampling period

By changing the integration variable, (3) is written as

$$x(k+1) = e^{ATd}x(k) + \int_0^{Td} e^{A\lambda}Bd\,\lambda z(k) \quad \ldots\ldots\ldots (4)$$

(4)is rewritten as:

$$x(k+1) = Gx(k) + Hz(k) \quad \ldots\ldots(5)$$

G and H are sampled matrices of sampling time T_d .Matrices G and H are calculated for small sampling time as follows:

$$G = \begin{bmatrix} G11 & G12 \\ G21 & G22 \end{bmatrix}$$

$$G \cong e^{ATd} = I + ATd + \frac{A^2Td^2}{2} \quad \ldots\ldots(6)$$

$$H = \begin{bmatrix} H11 & H12 \\ H21 & H22 \end{bmatrix}$$

$$H = \int_0^{Td} e^{A\lambda}Bd\,\lambda \cong \int_0^{Td}(I + A\lambda)Bd\,\lambda \quad \ldots\ldots(7)$$

From (6) and (7), $G_{11} = 1 - \frac{T_d^2}{2L_fC_{fc}}$ $G_{12} = \frac{T_d}{C_{fc}} - \frac{T_d^2R_f}{2L_fC_{fc}}$

$$H_{11} = \frac{T_d^2V_{dc}}{2L_fC_{fc}} \quad , \quad H_{12} = -\frac{T_d}{C_{fc}}$$

Hence the capacitor voltage from (5) is given as:

$$v_{fc}(k+1) = G_{11}v_{fc}(k) + G_{12}i_{fi}(k) + H_{11}u(k) + H_{12}i_{fi}(k) \quad ..(8)$$

From the equation (8), the terminal voltage should be maintained at reference value and it depends upon the inverter parameters V_{dc}, C_{fc}, R_f, L_f and T_d

Therefore, inverter parameters must be chosen very carefully.

Let v_t^* be the reference load terminal voltage.

A minimization of cost function is chosen as follows:

$$J = \left[v_{fc}(k+1) - v_t^*(k+1)\right]^2 \quad ...(9)$$

The minimum value of cost function is acquired by differentiating with respect to $u(k)$. The voltage control-law, from (8) and (10), is given as:

$$v_{fc}(k+1) = v_t^*(k+1) \quad ....(10)$$

In (11) $V_t^*(k+1)$ is the unknown future reference voltage. Using a second-order

$$u^*(k) = \frac{v_t^*(k+1) - G_{11}v_{fc}(k) - G_{12}i_{fi}(k) - H_{12}i_{fi}(k)}{H} \quad (11)$$

Then $u^*(k)$ is converted into the ON/OFF switching command to corresponding VSI switches using hysteresis controller.

IV. SIMULATION RESULTS

By using the proposed control algorithm and multifunctional DSTATCOM which makes the 3-ϕ source currents balanced and sinusoidal. To protect the sensitive loads during voltage disturbances, a fast voltage regulation is provided at the load terminal.

System quantities	values
Stiff source V_s	230v
Filter inductance L_f	20mH
Filter capacitance C_f	10 μ F
External inductance L_{ext}	11mH
V_{dc}	600v
C_{dc}	3000 μ F

In the initial, a unbalanced linear and non-linear load of 6.9kw is connected. At t=0.2sec, the load current in phase-a increases by increasing the load to 9.6kw which is shown below figure

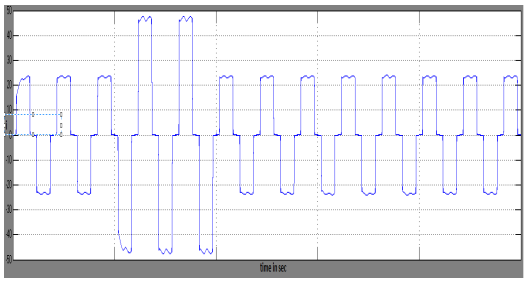

Fig (3) load current waveforms of phase-a before, during and after load change

The source voltage and current waveforms are in phase with each other after the load change

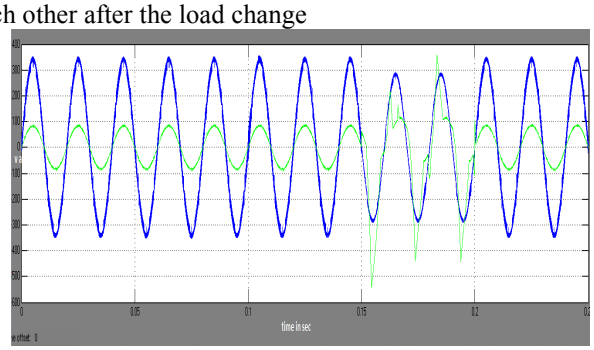

Fig (4) source voltage and current waveforms of phase-a before, during and after load change

At t=0.8sec a sag is created by reducing the source voltage by 30% to show the voltage regulation capability of DSTATCOM. During this sag period the source current increases.

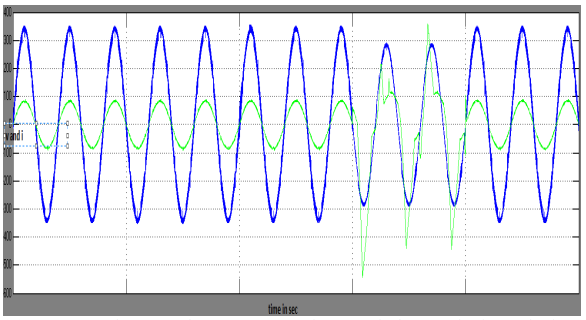

Fig (5) source voltage and current waveforms of phase-a before, during and after sag

Maintaining the voltage of 0.9pu, a fast voltage regulation is provided at the load terminals

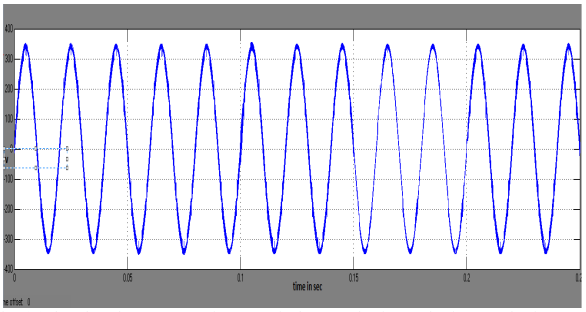

Fig (6) load voltage waveforms of phase-a before, during and after sag

During normal operation, load change and voltage disturbances a controller regulates the load angle. Voltage at DC bus is regulated around 1200 during the whole process.

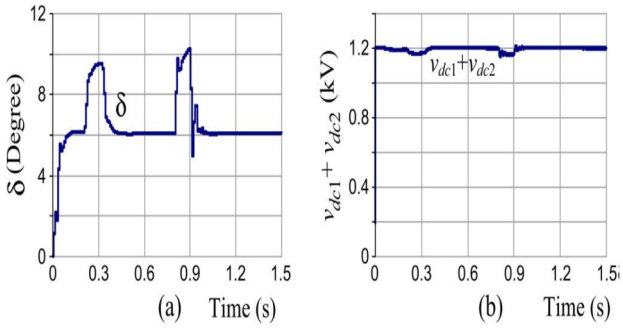

Fig (7) a)load angle b)voltage across dc bus

V. CONCLUSION

Through this paper a new algorithm is used to generate reference voltage for DSTATCOM in voltage control mode. It meets the objectives protecting the load from voltage disturbances under stiff source, fast load voltage regulation, advantages of the ccm operation are achieved while operating in vcm, attaining unity power factor (UPF), harmonics reduction, nearly UPF is attained during load change, losses are decreased so as saving the rating of VSI. Thus, by considering the above one can say PQ is improved. The simulation results have been presented.

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