Converter Topologies in VSC-HVDC Systems-an overview

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Abstract— **The converter topologies in VSC-HVDC system have an important role in the performance of the system. In this paper, an overview of converter topologies such as, Two level, Three level and Multi Modular Converter (MMC) topologies that are applicable for VSC-HVDC systems is presented. A comparative study of these topologies is carried out. Also a summary of the converter topologies implemented in VSC-HVDC systems by different pioneer power industries is presented.**

Keywords— Two level converter, Neutral Point Clamped converter, Flying Capacitor converter, Modular Multilevel converter, VSC-HVDC.

I. INTRODUCTION

The basic VSC-HVDC topology consists of a converter at each end of a pair of extruded DC transmission cables or DC transmission lines. The station feeding energy into the DC circuit is called the rectifier, the converter taking energy from the DC circuit and feeding it into the receiving AC network is called the inverter. In VSCs, the roles of the inverter and rectifier can be interchanged between the stations at any time without delay, without breaker switching and without polarity reversal. Both stations can independently generate or consume reactive power as suitable at connection point [1]. The classical bulk-power HVDC transmission system converters that are usually referred to as Current Sourced Converter (CSC) are realized by line-commutated Thyristors at the sending and receiving end stations. Motivated by the availability of high power rating GTOs, a conventional two-level PWM based Voltage Sourced Converters based HVDC (or VSC-HVDC) system was proposed [2] for the first time in 1990. Nowadays, VSC-HVDC systems generally utilize IGBTs for the converters. For increasing the power rating of such simple topology, stacking of several power semiconductor devices in series is required [3], [4]. Even though this arrangement reduces the voltage stress on each device and increases the power rating, it adds more control complications to ensure dynamic voltage balancing between the series connected devices. An alternative approach to achieve high power rating of the converter stations is to use multilevel converter topologies. More commonly used multilevel topologies in VSC-HVDC systems are: Neutral Point Clamped converter topology, Flying Capacitor topology and their modified versions such as Multi-Level Voltage reinjection (MLVR) schemes [5, 6] with simpler switching

structures. But those topologies have inherent problems that restrict the number of their practical voltage levels. Another promising topology named the Modular Multilevel topology that uses Modular Multilevel Converter (MMC) is gaining popularity in VSC-HVDC systems due to simple structure and control [7], [8]. It has no restrictions on its practical voltage levels and overcomes most of the problems of Two level and Three level converters.

In this paper, simulation models for these converter topologies and the switching techniques are developed in SimPowerSystems environment. The paper is organized as follows: In section II, simulation models for Two level, Three level Neutral Point Clamped converter, Three level Flying Capacitor Converter, Seven level and Thirteen level MMC topologies are developed. The simulation results and FFT analysis of Line to Line voltage are presented. A comparison of these converter topologies with respect to Total Harmonic Distortion (THD), number of switching devices required per leg of the converter and also requirement of DC link capacitor is carried out. In section III, a consolidated information about the converter topologies implemented by different pioneer power industries for VSC-HVDC transmission is presented.

II.   CONVERTER TOPOLOGIES

In this section, a detailed description of Two level, Three level and MMC topologies is presented. Simulation models and the switching techniques for each topology are developed. The harmonic level in the output voltage is determined and compared.

For all the VSC topologies considered here, the output voltage rating and the load current (phase peak) are chosen as ±150 kV and 2.5 kA respectively.

A. *Two level converter*

The Two level topology has been widely used in many applications at a wide range of power levels. Fig. 1 shows one phase of a Two level converter and the corresponding output voltage. As seen from the figure, the output is a square waveform, which can be improved using Pulse Width Modulation (PWM) technique. Such an improved output is found to have a dominant fundamental component and significant high order harmonics [9].
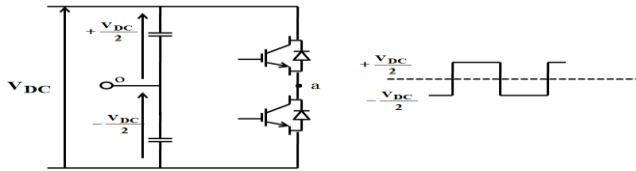
Fig. 1. One phase of a Two level converter

In order to illustrate this, a detailed scheme of one converter of VSC-HVDC system, chosen to be operating in inverter mode with a star configured RL load is shown in Fig. 2.Here, a virtual zero point at the DC voltage source side (o) is considered, in order to determine the output voltages of the inverter. Therefore, the output voltages v_{a0}, v_{b0} and v_{c0} can take only two values: $+V_{dc}/2$ and $-V_{dc}/2$.

In the PWM technique used for the Two level converter, three phase reference control voltages (modulating voltages) v_{aref}, v_{bref} and v_{cref} of 50 Hz that are phase displaced by 120^0 with respect to each other are compared with the triangular wave, v_{tr} and gate pulses are generated as shown in Fig. 3.

In order to avoid dominant higher harmonics, the frequency of the triangular voltage (f_s) must be odd. Further, zero crossover of each control voltage should coincide with zero crossover of the triangular voltage.

According to the Fourier analysis, this condition is fulfilled if the frequency relation $k_f = \dfrac{f_s}{50}$ is a whole multiple of three, where k_f is given by Equation (1)

$$k_f = (2n+1)*3 \text{ with } n=0,1,2,3\ldots \qquad (1)$$

In this method of PWM technique, the per phase output voltage provides half and quarter wave symmetry, which eliminates even harmonics from the carrier spectrum and allows symmetrical three phase voltages to be generated from a three phase sine wave set and one saw tooth waveform [10,11].

Here, k_f is chosen as 27 for which, n=4, that results in a value of 1350Hz for f_s.

The relation between the amplitudes of the control voltages and triangle voltage is amplitude modulation factor 'm', which decides the amplitude of the output voltage and is given by Equation (2)

$$m = \dfrac{\hat{v}_{ref}}{\hat{v}_{tr}} \qquad (2)$$

The pole voltage (v_{ao}), pole to pole voltage (line to line voltage) v_{ab} and phase A load current waveforms are shown in Figure 4(a), (b) and (c) respectively. As seen in the figure, the pole voltage switches between two levels of voltage: +150 kV and -150 kV. The FFT analysis of the line to line voltage (L-L) is shown in Fig. 5 and is observed that, only odd harmonics are present with predominant harmonics of order 25th and 27th. The THD is found to be 119.35%.

The quality of the basic ac waveform can be improved by using multi level inverters. The basic multilevel inverter is a Three level inverter, which is explained in the following section.
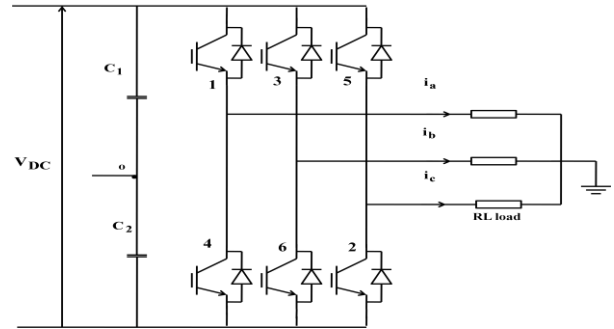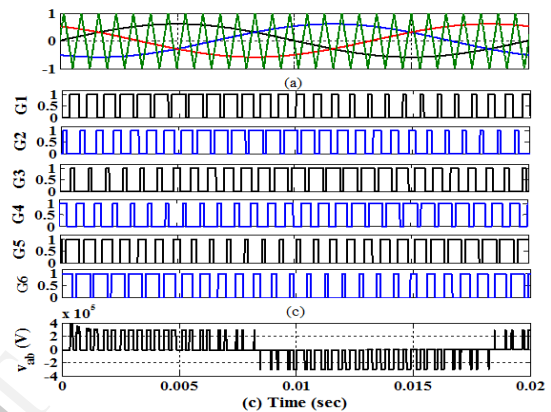

Fig. 2. Simplified two level inverter

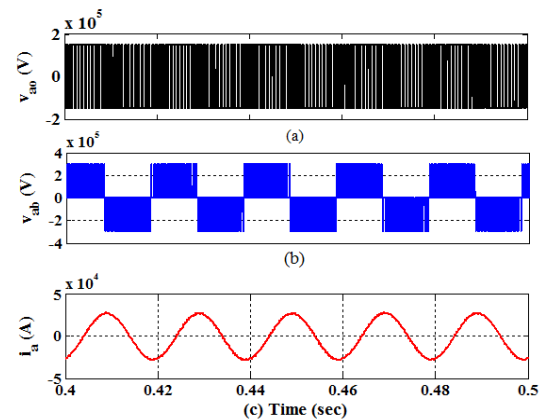Fig. 3. Principal operation of PWM
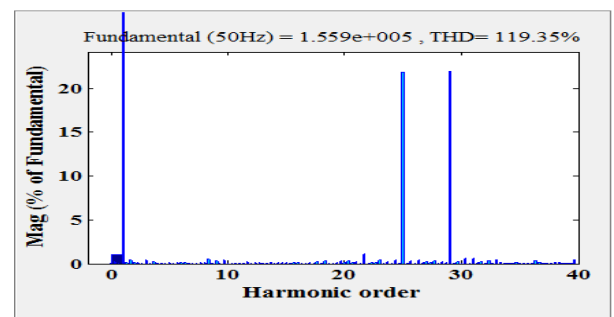

Fig. 4. AC voltages and load current

Fig. 5. FFT analysis of L-L voltage

B. Three level converters

The main objective of multi level conversion is to generate a good high voltage waveform by stepping through several intermediate voltage levels. Generally, for an m-level converter, the phase voltage has m steps and the line voltage has (2m-1) steps [10]. In this paper, the following multilevel VSC concepts that are commonly implemented / proposed in VSC-HVDC systems are described.

1. Neutral Point Clamped (NPC) converters
2. Flying capacitor converters

Here, for both types, the number of levels chosen is three. The switching frequency is 1350Hz and the modulation index is 0.8. A detailed description is provided in the following sections:

1) Neutral Point Clamped converters

The three level NPC-VSC is a multi level converter that offers an alternative to reduce (or even to avoid) the number of series connected switches for high power applications [12].The circuit for a Three level Neutral Point Clamped converters is shown in Fig. 6. In this topology, the converter unit ac terminals are switched between three dynamic voltage levels. As seen from Fig. 6, the three phase unit has as extra terminal on the DC side connected to the centre point of the equally split DC source (o). The switching configuration has two sets of valves in series, with their intermediate point connected to the DC supply centre tap via extra diodes (D11, D21, D31, D12, D22 and D32).

The gate signals for such a converter are generated by comparing a reference wave with two triangular signals, which have the same amplitude and frequency, but they are level shifted as shown in Fig. 7(a).The gating commands for switches S11 and S12 must be complementary and similarly for switches S13 and S14 must also be complementary as shown in Fig. 7(b).

The v_{ao}, v_{ab} and i_a waveforms are shown in Fig. 8. As seen from Fig. 8(a), v_{ao} consists of three levels, i.e. positive (+150 kV), negative (-150 kV) and zero for a chosen V_{DC} of 300 kV at the input terminals of the inverter. The positive level is produced by switching on the two series connected upper valves of the phase unit (switches S11, S12). Similarly, the negative level is produced by switching on the two series connected lower valves of the phase unit (switches S13,S14).The zero level is produced by switching the upper and lower middle valves, thus connecting the centre tap of the DC supply to the output via the two extra diodes (switches S12,S13). In the zero voltage output region, the current continues to flow via the upper middle IGBT device and upper centre tap diode (when positive), or the lower middle IGBT device and the lower centre tap diode (when negative).The FFT analysis of the L-L voltage is shown in Fig. 9 and is observed that, only odd harmonics are present and the THD is found to be 41.07%, which is drastically reduced, when compared to Two level circuit topology.
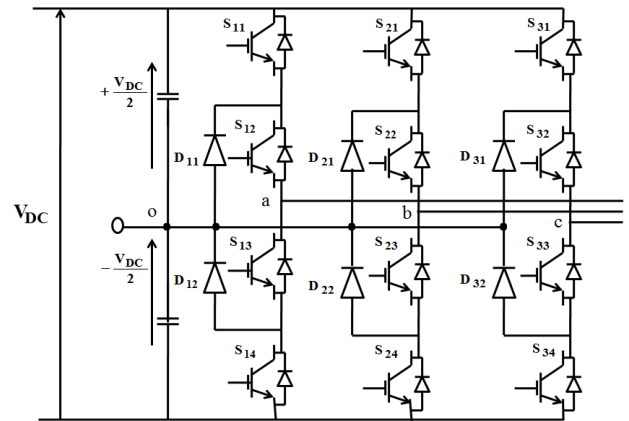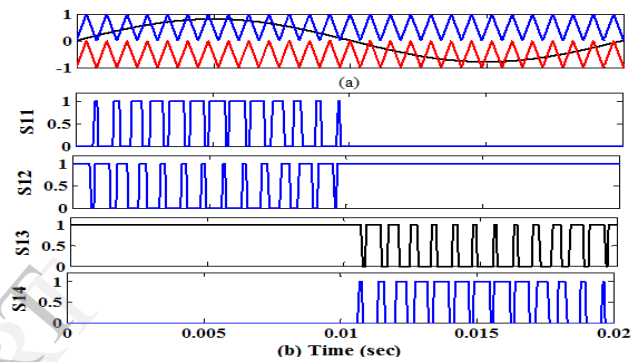

Fig. 6. Three level NPC converter topology

Fig.7. Gate pulse generation for phase A switches with m=0.8, f_s=1350Hz
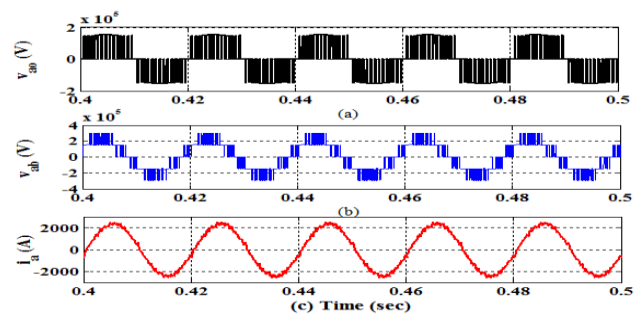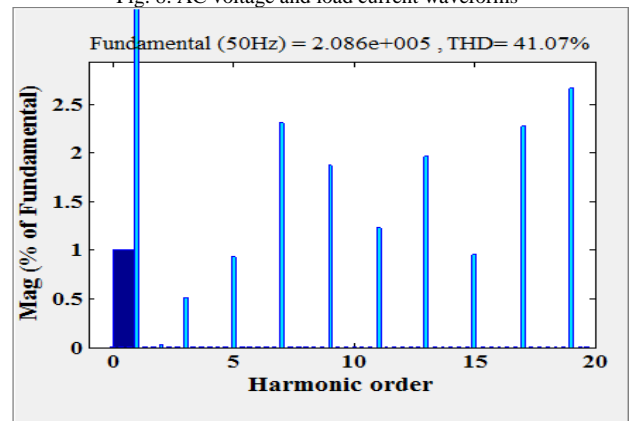

Fig. 8. AC voltage and load current waveforms

Fig. 9. FFT analysis of L-L voltage

2) Flying capacitor converters

The Flying capacitor conversion is also known as Floating capacitor or Imbricated cell conversion and the circuit for the converter is shown in Fig. 6[10],[13-15]. In this type of converter, the additional voltage step is obtained by the use of a separate DC capacitor in each phase. This capacitor is pre charged to one half of the total DC voltage across the converter bridge.

The switches in each phase arm are arranged in two pairs (A1, B1) and (A2, B2). Within each pair, the switches need always to be in complementary states. Thus, to create the $-V_{dc}$ level of the phase output waveform, switches A1 and B2 must be turned on. Similarly, switches A2 and B1 need to be turned on to produce the $+V_{dc}$ level. The intermediate DC capacitor is bypassed for part of the fundamental frequency cycle.

From Fig. 11 and Fig. 12, it is seen that, the PWM switched waveform and the Fourier analysis are identical to the NPC circuit results.

3) Modular Multilevel Converter

MMC is realized by series connection of submodules. The submodule is mainly composed of two IGBT switches and a
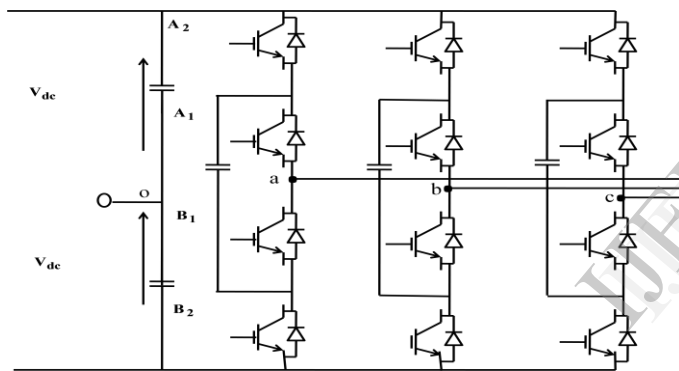

Figure 10 Three level Flying Capacitor converter

local dc-storage capacitor, as shown in Fig. 13.Each submodule can be switched between a state with full module voltage (when IGBT 1 = ON, IGBT 2 = OFF) and a state with zero module voltage (when IGBT 1 = OFF, IGBT 2 = ON) in both current directions.
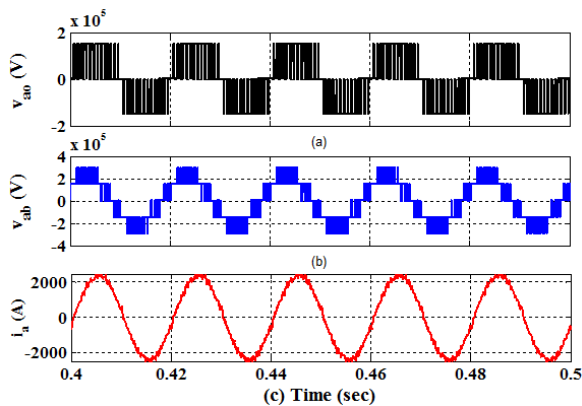

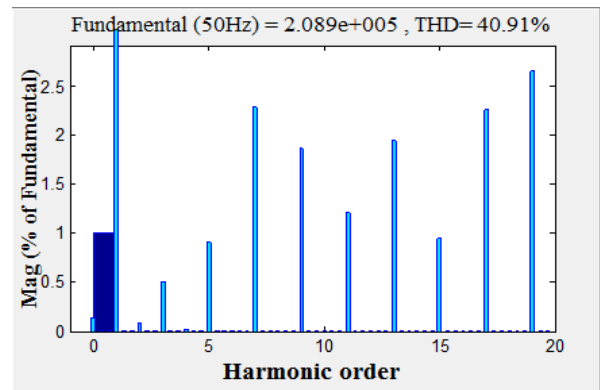Fig. 11. AC voltage and load current waveforms

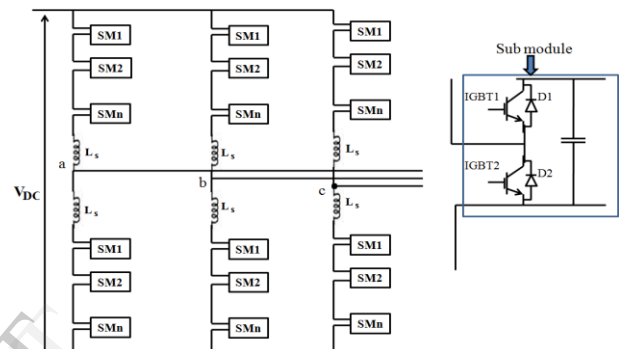Fig. 12. FFT analysis of L-L voltage

Fig. 13. MMC circuit with details of a submodule:

Depending on the current direction, the capacitor can be charged or discharged, if IGBT 1 is turned on.

During steady-state operation, the voltages are controlled in order to achieve one third of the total DC current in each phase unit and to achieve an equal sharing of the AC current in the upper and lower part of each phase unit [8].It is found that, a very smooth and nearly ideal sinusoidal waveform can be generated with MMC converters, since each submodule is switched individually. Owing to this, the requirements to filter circuits are much less severe. Additionally, the submodules can be switched at a significantly lower frequency which, in its turn, leads to lower operational losses of the converter. The MMC converter has a modular design resulting in its high flexibility.

The converter reactor(Ls)shown in Fig. 13 substantially reduces the effects of faults arising inside or outside the converter and also damp the balancing currents to a very low level and make them controllable by means of appropriate methods.

The gate pulse generation for MMC topology is a challenging issue. The multicarrier PWM techniques are used for generation of gate pulses. In this technique, a single modulating or reference signal, which in most cases is sinusoidal, is compared and sampled through a number of triangular waveforms. The multicarrier PWM techniques can be categorized as follows [16]:

a) Carrier disposition methods:

Here, N-1carrier signals with the same peak-to-peak amplitude and same frequency are disposed in such a way so that the bands they occupy are contiguous and form an N-level line-to-neutral output waveform. These methods are further classified to phase disposition (PD), phase-opposition-disposition (POD), and alternative-phase-opposition-disposition (APOD).

In this paper, gate pulse generation using PD technique is implemented for a seven level MMC, where in, all triangular carriers are in phase as shown in Fig. 14(a). The chosen values for f_s and 'm' are 2.5kHz and 0.9 respectively. The phase voltage, L_L voltage and load current waveforms obtained with this technique without any filter equipment are shown in Fig 15. Here, H+1 modulation technique (H is the number of sub modules) is used to obtain seven level output [17]. The simulation model does not include any voltage balancing algorithm to maintain equal voltage across the submodules. The switching frequency can be further reduced if this is taken care and also the voltage levels can be clearly distinguished in the output voltage waveform. It is also observed from the FFT analysis of the L-L voltage shown in Fig. 16 that, the THD is reduced to 13.15%, which is much less when compared to two level and three level inverter voltage THD levels.

a) Sub-harmonic method

Here, a number of carriers are phase shifted with respect to each other. The phase shifted angle is determined by the number of levels of the output waveform and is usually defined as = 360/ (N -1) , where N is the number of line-to-neutral levels. Gate pulse generation using phase shifted technique is implemented for a 13 level MMC, wherein, the triangular carriers are phase shifted by 30^0, as per the above equation. The chosen values for f_s and 'm' are 250Hz and 0.9 respectively. Here, 2H+1 modulation technique is implemented, where in 2H+1 levels of output can be obtained by modulating an MMC with H SMs per arm [17].

The sub module voltage balancing is not taken care in this simulation model. The phase voltage, L_L voltage and load current waveforms obtained with this technique without any filter equipment are shown in Fig. 17. It is also observed from the FFT analysis of the L-L voltage shown in Fig. 18 that, the THD is reduced to 10.69%, which is much less when compared to Two level and Three level THD levels.
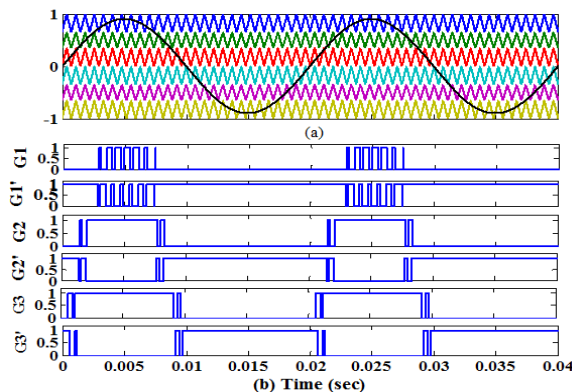

Fig.14. PD PWM technique of gate pulse generation (shown for 3 sub modules of phase 'a')
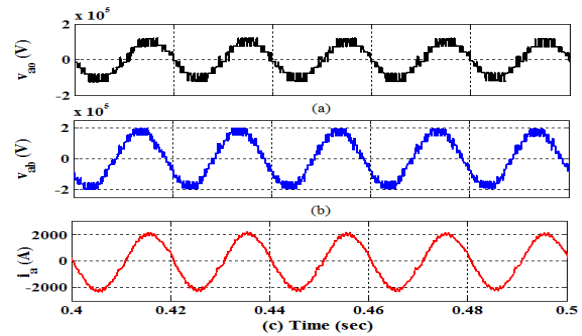

Fig. 15. AC phase voltage, L-L voltage, load current
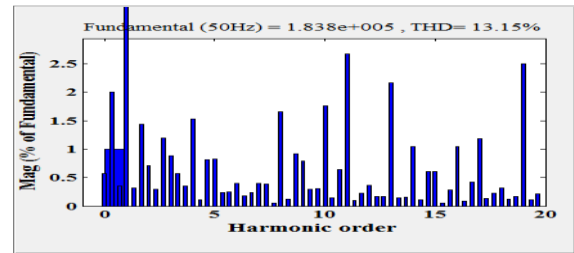
Fig. 16. FFT analysis of AC L-L converter voltage
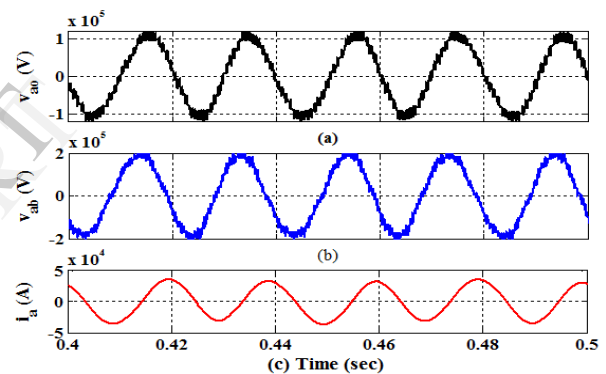
Fig. 17. AC phase voltage, L-L voltage, load current

Fig. 18. FFT analysis of AC L-L converter voltage

A comparison of the topologies described in the previous paragraphs is presented in Table I. It is observed from the simulation models developed that, for a constant DC link voltage of 300 kV at the input terminals of the inverters, the DC link capacitor value has to be increased to get the same level of output AC voltage in all these converters.

TABLE I. SUMMARY OF COMPARISON OF THREE TOPOLOGIES

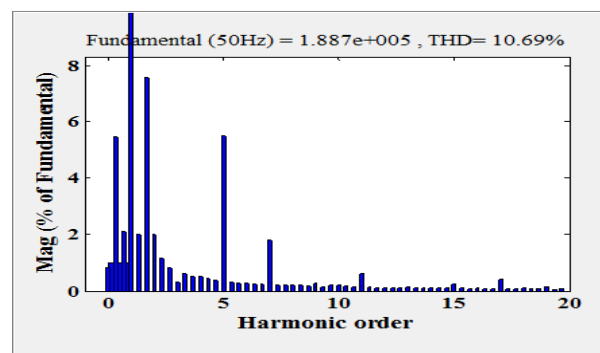| Comparison of VSC topologies	THD %	Modulation technique	No. of IGBTs per leg of the converter	DC link capacitor
Two level	119.35	Simple	2	35 μF
Three level	41.07	Complex	4	1500 μF
MMC			12 SMs in half bridge configuration	
(a)Seven level	13.15	Complex	24	2500 μF
(b)Thirteen level	10.69	Complex	24	2500 μF

III. CONVERTER TOPOLOGIES IN THE EXISTING VSC-HVDC PROJECTS

In the following paragraph, a brief information about the converter topologies used by some of the major companies dominating the global VSC-HVDC market is provided. ABB (Switzerland), Siemens (Germany), and Alstom (France) are found to be the key companies that have involved in the installation and successful operation of VSC-HVDC systems in different parts of the world.

The development of HVDC Light® converter (VSC developed by ABB) technology has been going over three generations. Generation 1 topology was a two-level converter switching the full voltage in a PWM pattern. Generation 2 was a three-level converter where the losses were reduced, but at a cost of more IGBTs. Generation 3 was a two-level converter with reduced number of IGBTs, but keeping the losses down by using optimized switching pattern and more optimized IGBT design [18]. Generation 4 topology is Cascaded two-level (CTL) converter, which is realized by connecting several smaller two-level building blocks (cells) in series. This configuration of converter is found to significantly reduce station losses.

HVDC PLUS (VSC developed by Siemens) with two level, three level and multi level topologies has also been successfully implemented in some of the HVDC projects undertaken by Siemens company.

HVDC MaxSine®, the VSC HVDC technology being developed by Alstom Grid [19], combines the advantages of the two kinds of existing circuit topologies. In the first, low-pulse-number converters are used, using large numbers of IGBTs in series, with pulse width modulation (PWM).The second category uses a multi-level approach to achieve very high pulse numbers for independently controlling a large number of bridges in each phase. In the new topology, the multi level converter cells are used to provide a voltage wave shaping function which is directed to the appropriate AC or DC network using the semiconductor switches. It is also found that, these new VSC topologies are to be tested in a demonstrator facility in Stafford, UK, consisting of a complete 25 MWHVDC scheme, configured in a back–to–back arrangement.

Some of the VSC-HVDC projects implemented by these companies are listed in Table II [20- 25].

TABLE II. EXAMPLES OF A FEW VSC-HVDC PROJECTS AND CORRESPONDING CONVERTER TOPOLOGIES

Project Name	Commis--sioning year	Power/ voltage rating	Company	Converter topology
Hällsjön, Sweden	1997	3 MW ±10 kV	ABB	Two level
Eagle Pass, USA	2000	36MW ± 15.9 kV	ABB	Neutral Point Clamped
Tjaereborg, Denmark	2000	7.2 MW +/- 9 kV	ABB	Two level
DirectLink, Australia	2000	180 MW ± 84 kV	ABB	Two level
MurrayLink, Australia	2002	220 MW ± 150 kV	ABB	Three level
CrossSound, USA	2002	330 MW ± 150 kV	Siemens	Two level (initially) Three level (presently)
Estlink, Estonia Finland	2006	350 MW ± 150 kV	ABB	six-valve converter bridge
Trans Bay Cable Link, San Francisco, USA	2010	400 MW ± 200 kV	Siemens	MMC
EirGrid East-West Interconnector between Ireland and Wales	2013	500MW ±200 kV	ABB	Two level converter topology

CONCLUSION

In this chapter, Two level, Three level and Modular Multi level converter topologies that are utilized in the VSC-HVDC system are described. The simulation models are developed for all the three topologies and some of the PWM techniques commonly used are addressed. The AC output voltage, current waveforms and the harmonic analysis of L-L voltage are presented. From the comparison of different topologies, it is found that, THD of L-L voltage of MMC is very less when compared to that of Two level and Three level converters. A brief information about the converter topologies utilized in the VSC-HVDC systems that are installed and operating successfully across the world is presented.

It is also seen from the simulations that, Two level converters are simple in structure and the complexity in gate pulse generation is found to be less when compared to Three level and MMC topologies.

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