International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 11, November - 2017

Comprehensive Study of Popular VLSI Test Scan Architecture

Madhura.R
AsstProfessor,ECEdept
DSCE, Bangalore

Ravi Shankar J
Co-Guide & Advisor
Govt.of Karnataka
Bengaluru,karnataka

Dr. Shanthi Prasad .M.J
Professor, ECE Dept.
KSIT, Bangalore

Abstract- **As a part of my ongoing Research on VLSI Design test architecture, I undertook an exhaustive & comprehensive technical survey spanning several technical papers, books, websites & data sheets to cover various & popular VLSI TEST SCAN ARCHITECTURES that are contemporary & widely used. In this paper, I am able to arrive at the TREE DIAGRAM covering various types of VLSI TEST SCAN ARCHITECTURE.**

Keywords- Design for testability, full scan, partial scan, Random access scan, Multiple scan, RT level scan, Generic scan, Boundary scan, Special purpose scan.

INTRODUCTION

Integration of design and test referred as **Design for** Testability (DFT) proposed in 1970s.

- To test circuits, need to control and observe logic values of internal lines.
- It helps to find difficult part of the circuit to test and assist in test pattern generation for fault detection.
- The three most important factors that determine the complexity of deriving a test for a circuit:
  - Controllability,
  - Observability
  - Predictability

Testability: It influences various costs associated with testing. It allows for status of device to determined and isolation of faults in a device to perform quickly to reduce both test time and cost.

Cost effective development of the tests to determine the status

Controllability: Ability to establish a specific signal value at each node a circuit by setting value on the circuit's input.

Observability: It is the ability to determine the signal value at any node in a circuit by controlling the circuit's inputs and observing its outputs.

Impact of accessibility on testing leads to following general observation.

- Sequential logic is much more difficult to test than combinational logic.
- Control logic is much more difficult to test than data-path logic
- Random logic is more difficult to test than structured, bus-oriented designs.

Ad-hoc approach

Ad-hoc approach involves a set of design practice and modification guidelines for testing improvement. Typical ad hoc techniques are:

- Insert test points
- Avoid asynchronous set/reset for storage elements
- Avoid combinational feedback loops
- Avoid redundant logic
- Avoid asynchronous logic
- Partition a large circuit into small blocks.

LSSD or Scan Design

1. Full scan design

In full scan design, all storage components are replaced by scan cells, which are then configured as shift registers (scan chains) during shift operation. Here, all the inputs and outputs of the circuit can be controlled and observed.

1.1 Muxed-D full scan design

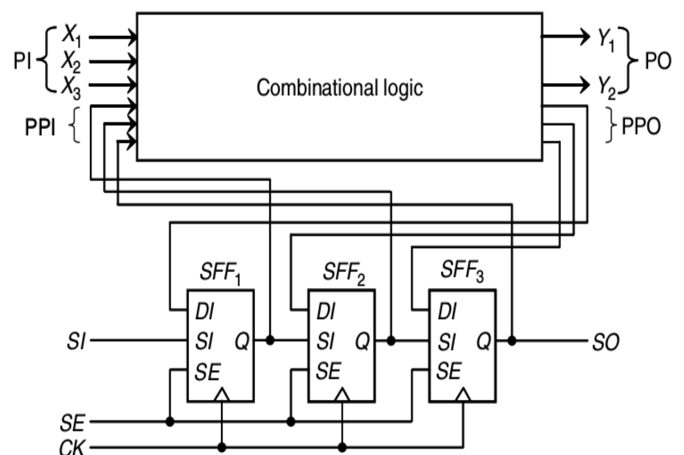

Fig.1 Muxed-D full scan design

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The circuit consists of three scan cells SFF1, SFF2 and SFF3. The data input DI of each scan cell is connected to the output of the combinational logic. In order to form a scan chain, the scan inputs SI of SFF2 and SFF3 are connected to the output of the previous scan cells, SFF1 and SFF2, and the scan input SI of the first scan cell SFF1 is connected to the primary input SI, and the output Q of the last scan cell SFF3 is connected to the primary output SO. In shift mode, SE=1, and the scan cells operate as a single scan chain. In capture mode, SE=0, and the scan cells capture the test response from the combinational block when a clock is applied.

1.2 Clocked full-scan design

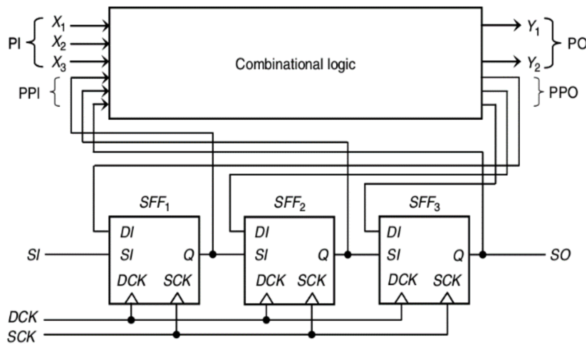

Fig.2 Clocked full scan design

The above figure shows the implementation of clocked full-scan circuit. The circuit is tested using shift and capture operations, similar to muxed-D full scan circuit but the difference is that two independent clocks SCK and DCK are used for shift and capture mode.

Advantage:

- It provides total controllability and observability of internal nodes by providing external access to all storage element
- It converts the difficult problem of sequential ATPG into the simpler problem of combinational ATPG.
- The test generation time is very small for the full-scan design.

Disadvantages:

- It consists of long chain of flip-flops that test data have to be shifted into that reflects on the test time.
- Individual scan cell cannot be controlled or observed without affecting the other scan cells.
- High switching activity at scan cells cause excessive test power dissipation and resulting in circuit damage.
- The presence of multiple clock domains is the challenge in full scan

1.3 LSSD full-scan design

LSSD full scan design can be implemented by using either single-latch design or double-latch design.

In single latch design, the output port +L1 of the master latch L1 drives the combinational logic block and slave latch L2 is used for scan testing. LSSD design use latches instead of flip-flops. Two system clocks C1 and C2 are used to prevent combinational feedback loops from occurring.

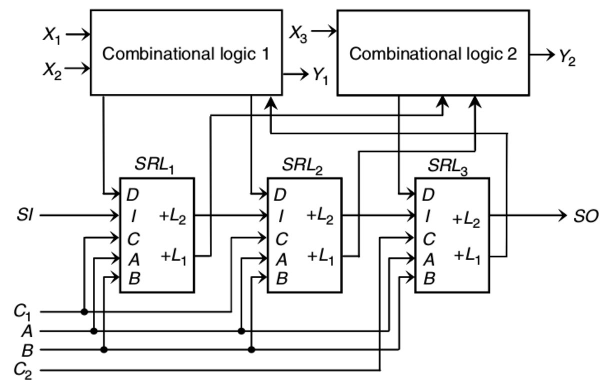

Fig.3 LSSD full scan design

In LSSD double-latch design, clocks C1 and C2 are applied in a nonoverlapping fashion. The testing of an LSSD full-scan circuit is done using shift and capture operations, similar to that of muxed-D full-scan circuit but these operations are distinguished by applying clock pulses C1, C2, A, and B. During the shift operation, clocks A and B are applied and the scan cells SRL1~SRL3 form a scan chain from SI to SO. During the capture operation, clocks C1 and C2 are applied and the test response is loaded from the combinational block into the scan cells.

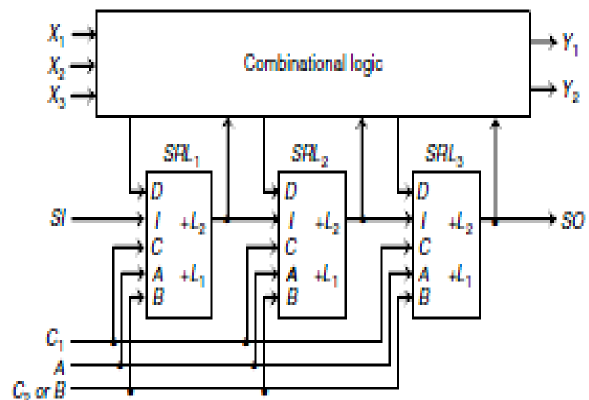

Fig.4 LSSD Double scan design

Advantages

It allows us to insert scan into a latch-based design.

- LSSD is guaranteed to be race free, which not case for the Muxed-D and Clocked-scan design.

Disadvantages

- It requires routing for the additional clocks, which increases routing complexity.

2. Partial scan Design

In partial scan design, a subset of storage element is replaced with scan cells to form a scan chain. A scan chain is constructed by using two scan cells SFF1 and SFF3, while flip-flop FF2 is left out. Sequential ATPG is used to control and observe the value of non-scan flip-flop FF2 and to detect faults in FF2. In this architecture, single clock is split into two

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separate clocks, one for controlling the scan cells, the other for controlling the non-scan cells.

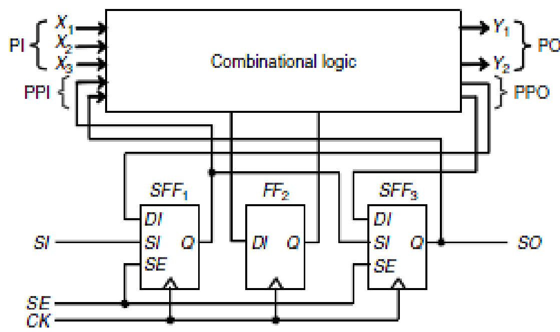

Fig.5 Partial scan design

I-Mode

There are two I-modes associated with mux represented by [IM (MUX: A->C); x=0; t=10ns] and [IM (MUX: B->C); x=1; t=10ns]. There are many I-modes associated with ALU denoted by [IM (ALU: A->C); x_1x_2=00; t=20ns] where x_1x_2=00is the condition for ALU to transfer the data from A to C. Another I-mode path is [IM (ALU: A->C); x_1x_2=01; B=0; C_{in}=0] where x_1x_2=01 is the condition for ALU to operate as adder. The I-mode for register is given by [IM (register: A->B); t=1 clock cycle]

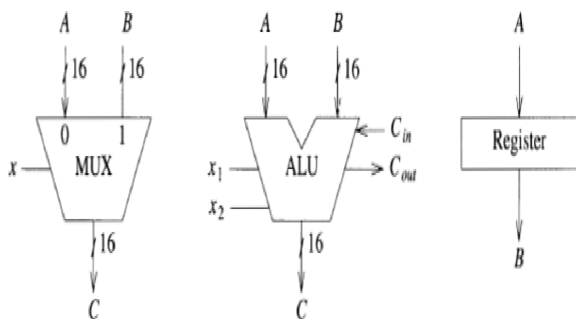

Fig.6 I-Mode Design

I-Path

I-Path refers to an identity transfer path that exists between output port X of module S1 to input port Y of module S2 represented by IP (S1:X->S2:Y).Every I-path consists of time tag and activation plan. Time tag denotes the time delay to transfer the data from X to Y. Activation plan represents the action performed to establish the I-path. I-path consists of chain of modules, each having an I-mode.

Advantages

- Partial-scan is a generalized scan method; scan can vary from 0 to 100%.
- Elimination of long cycles can improve testability via sequential ATPG.
- Elimination of all cycles and self-loops allows combinational ATPG. Partial-scan has lower overheads (area and delay) and reduced test length.
- Partial-scan allows limited violations of scan design rules, e.g., a flip-flop on a critical path may not be scanned.
- Reduced test time by having fewer bits to shift in.

Disadvantages

- Scan based architectures are very expensive as each scan test pattern contributes to a shift operation with high power consumption.
- Increase in test application time
- All the scan cells in the scan chain are switching at the same time causes excessive test power dissipation resulting in circuit damage.
- Low reliability or even test induced yield loss

3. Random– Access scan design

Scan cells are organized as two-dimensional array, where the cells can be accessed for observing (reading) or updating (writing) in any order. This full-random access capability is achieved by decoding a full address with a row (X) decoder and a column (Y) decoder. A $\log_2 n$bit address shift register is used that specifies which scan cell to access.

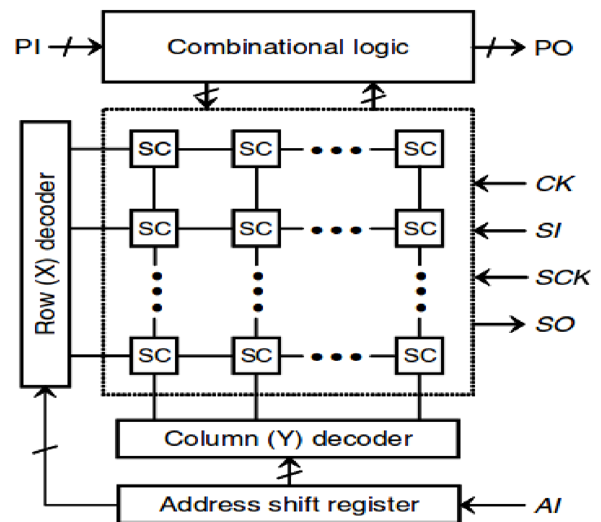

Fig.7 Random-Access scan design

Advantage:

- Reduces test power dissipation.
- Two independent test vectors applied consecutively simplifies process of performing delay.
- RAS may be suitable for certain architecture, e.g., where memory is implemented as a RAM block.

Disadvantages:

- Not suitable for random logic architecture
- High overhead – gates added to SFF, address decoder, address register, extra pins and routing
- Increase in test application time if a large no. Of scan cells have to be updated

4. MULTIPLE SCAN CHAIN

The problem of long scan chain can be solved by using multiple independent or parallel scan chain. In multiple independent scan chains, each scan register has its shift, load and clock control whereas in multiple parallel scan chains, all scan registers are controlled by the same set of signals.

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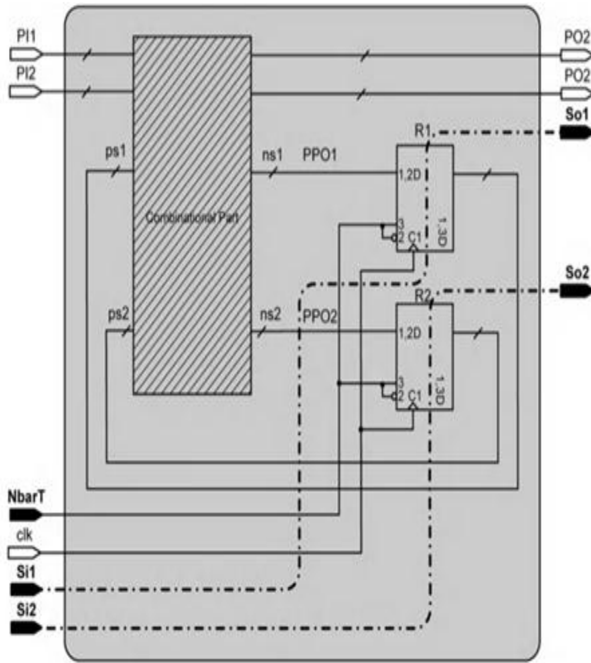

Fig.8 Multiple scan design

Advantages

- Reduces test time
- No overhead on test generation procedure

Disadvantages

- Overhead on extra test pins and in case of independent scans, on test clock and normal mode controls.

5. RT LEVEL SCAN DESIGN

5.1 RT level full-scan design

The adding machine includes two registers AC and IR, 6-bit program counter and 24 flip-flops including two control flip-flops. SI (serial input) is the left most bit of AC and SO (serial output) is taken from the least significant control bit. In RTL scan, the actual scan is inserted in the net list of the circuit obtained by synthesizing the behavioral description of the adding machine. Data_bus_in is the primary input, data_bus_out and ad_bus form the primary output.

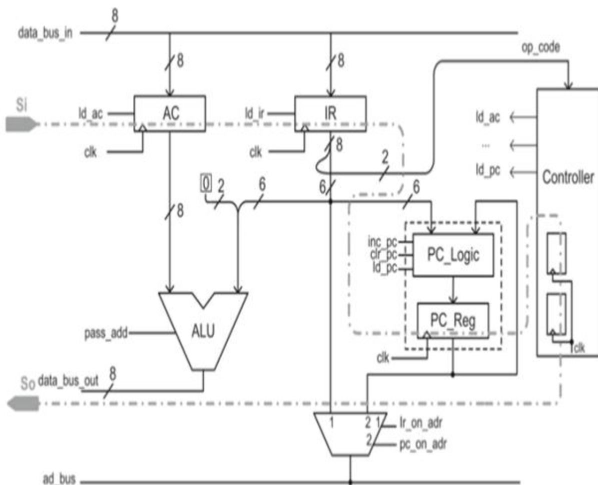

Fig.9 RT Level full scan design

5.2 RTL Design Multiple Scan

RTL design multiple scan architecture consists of three scan chains for AC, IR and for PC and two control flip-flops. The scan chains are inserted manually in the net list which is the result of synthesizing the Verilog code of the adding machine.

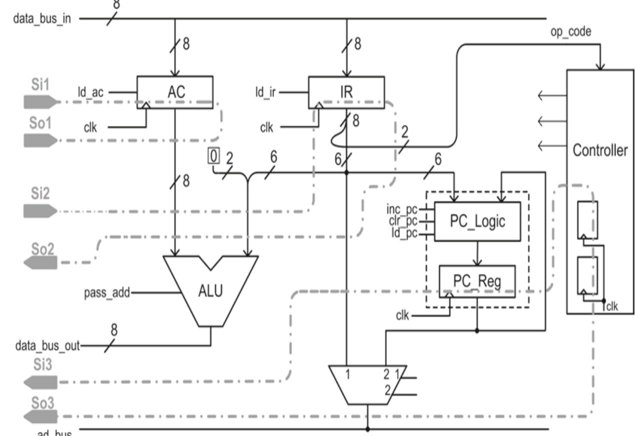

Fig.10 RTL multiple scan design

6. GENERIC SCAN BASED DESIGN

6.1 Full serial integrated scan

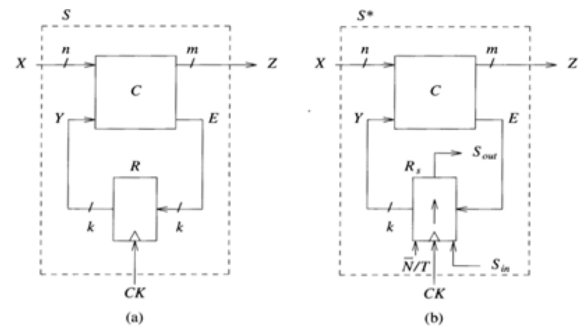

Fig.11 Full serial integrated scan

The full serial integrated scan circuit consists of a scan register R_s which operates in the parallel-latch mode when $\overline{N}/T=0$. The test generation is done using the algorithm such as PODEM or FAN. The result is a series of test vectors (x_1, y_1), (x_2, y_2), and responses (z_1, e_1), (z_2, e_2), .To test S^*, set $\overline{N}/T=1$ and scan y_1 into R_s. During the k-th clock period, $x_1$is applied to X and the first test pattern $t_1=(x_1, y_1)$ is applied to C. During the (k+1) th clock period, $\overline{N}/T=0$ and the state of E i.e., e_1 is loaded into R_s and the response on Z, i.e., is $z_1$is observed. The process is repeated and y_2 is scanned into R_s, e_1 is scanned out and hence becomes observable.

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6.2 Isolated Serial Scan

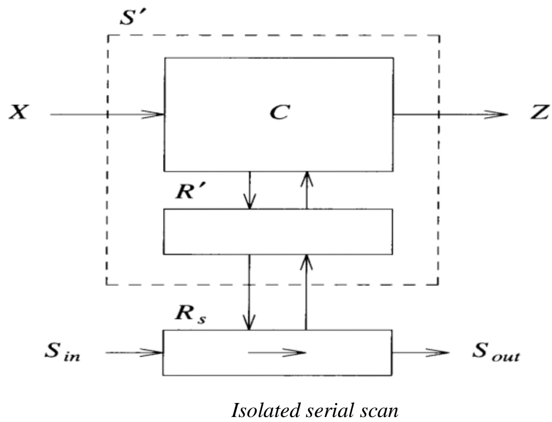

Fig.12

Isolated serial scan

In the above circuit S` consists of circuit C and register R`. The circuit can be tested by applying the test vector y_1 into R_s, which is then loaded into R` and circuit C. The response $e_1$ is loaded into R`, then transferred to R_s and scanned out. This type of architecture can be used in real time and on-line testing.

Advantages

- It supports real-time and on-line testing.
- On-line infers that, circuit can be tested while in normal operation.
- Data can be scanned out while circuit performs normal operation.
- This architecture supports latch based design i.e. Register consist of just latches rather than flip-flops.

6.3 Non-serial Scan

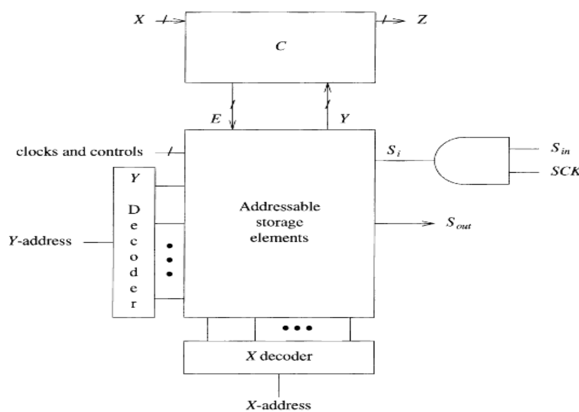

Fig.13 Non-serial scan architecture

In Non-serial scan architecture, storage elements are arranged in a random-access bit-addressable memory. During normal operation, the storage cells operate in the parallel-load mode. To scan a bit, the particular cell is addressed, the data is applied to S_{in} and the scan clock SCK is applied and the output of the cells are wired-ORed together. To scan out the cell contents, the cell is addressed and the control is broadcast to all cells and the output is obtained at S_{out}.

Advantages:

- To scan-in new vector only bits in R need to change
- It saves scanning data through entire register.

Disadvantage

- Overhead is high.

7. STANDARD IEEE TEST ACCESS METHOD

7.1 Boundary scan architecture

Test access port

TAP controller consists of three control pins TMS, TRST and TCLK. TMS (Test Mode Select) is used to put the test protocol in a given state for data or instruction. TCLK (Test clock) is the clock input that runs all the test hardware. TRST (Test Reset) pin resets the test hardware. It includes two data pins TDI and TDO. TDI (Test Data In) is used for shifting serial test data and instruction into the chip and TDO (Test Data Out) is the serial data pin.

BS-1149.1 Registers

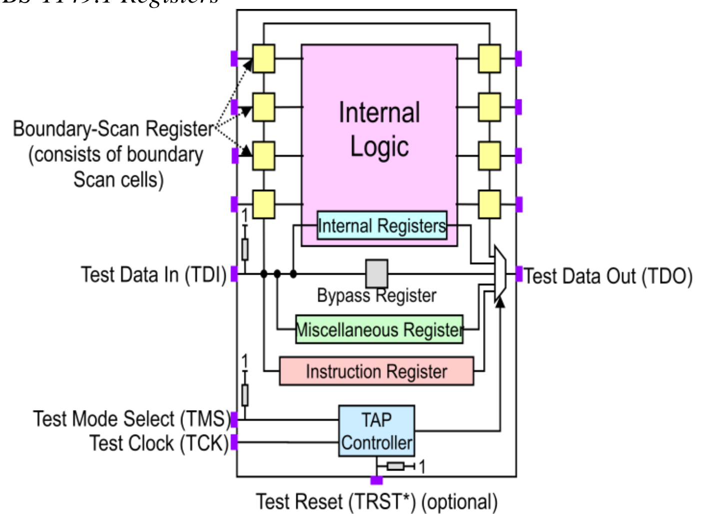

Fig.14 Boundary scan architecture

Registers are classified as instruction and data registers.

Instruction register

The instruction register cell consists of shift flip-flop which takes the serial instruction bits through S_{in} (TDI) input. When shiftIR=1, serial instruction bits from the previous cells are shifted into the flip-flop. The flip-flop is clocked by clockIR signal generated by the standard controller. At the end of shift or capture operation, the rising edge of updateIR data is obtained at the output of the first flip-flop which is then loaded into the instruction register. In the figure two flip-flops are active low asynchronous reset that resets the flip-flops when RstBar=0.

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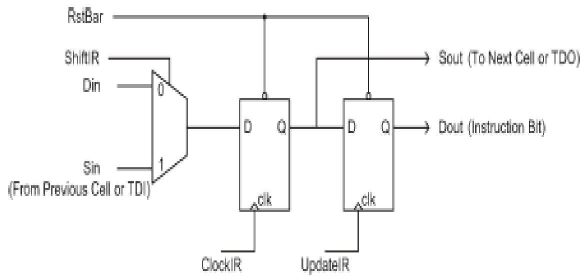

Fig.15 Instruction Register

Bypass register: The bypass register is a data register used to bypass a core from scan chain. It is a single-bit register which has either shift or capture flip-flop. In the bypass mode (Shift BY= 1), TDI is clocked into the bypass register on the rising edge of ClockBY.

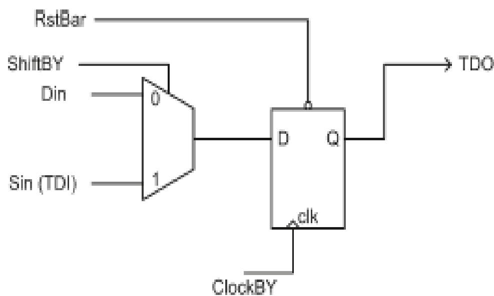

Fig.16 Bypass register

Device identification register
Device identification register (DIR) is an optional register in the 1149.1 standard. It is a 32-bit register that contains an identification code for the core logic.

Boundary scan register
Signals Sin and Sout are used for shifting serial data that enter the boundary scan register. It consists of shift or capture flip-flop and an update flip-flop. The update flip-flop holds the contents of the boundary scan register. Two multiplexers are used for routing the data. During the normal mode, the ModeControl of the output mux is 0, and Din is connected to Dout.

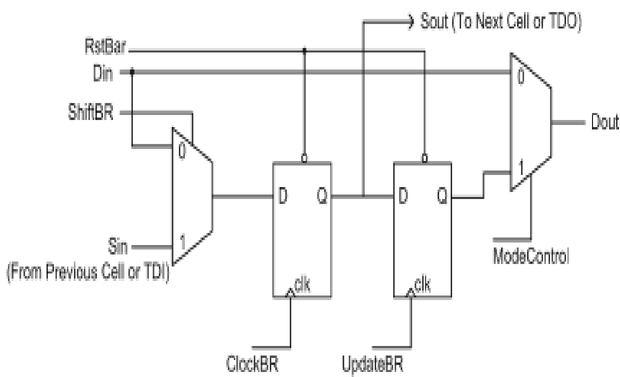

Fig.17 Boundary scan register

7.2 Boundary Scan Test Instructions
Boundary scan test instructions include 5 instructions:

Bypass instruction
This instruction is used for shortening the scan path and bypassing the units which are not involved in testing.

Sample instruction
Sample instruction captures the snap shot of input interconnect and outputs of the logic block.

Preload instruction
Preload instruction initializes the scan cells.

Extest instruction
Extest instruction tests the interconnection between two chips.

Intest instruction
Intest instruction tests the functionality of core logic which is performed in pin-permission mode.

7.3 RT level Boundary Scan
In the above circuit the adding machine is inserted in the hardware for CUT. It includes instruction register, decoder unit and boundary scan register. The decoder unit uses the output of instruction register along with the control signal to issue register control and select inputs. The adding machine 8 bit input bus, reset pin and a clock input.

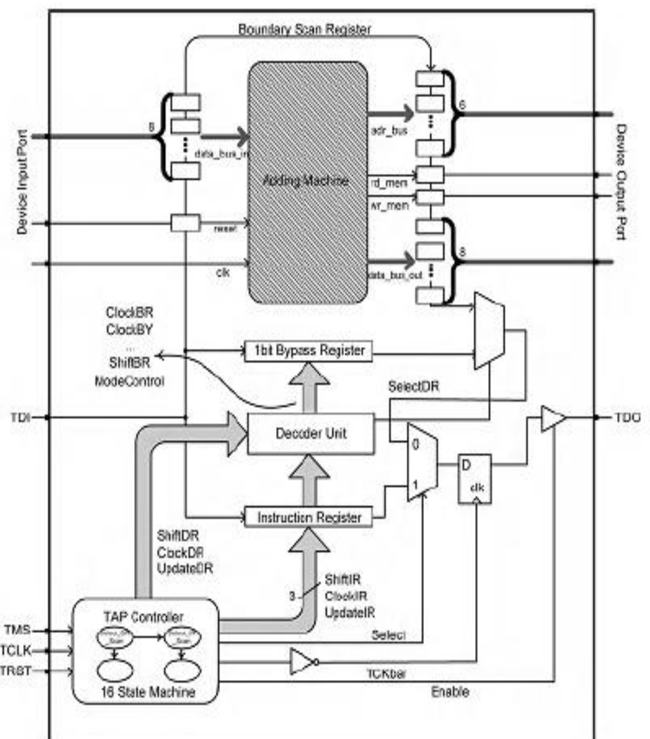

Fig.18 RTL Boundary scan architecture

Advantages

- It's a standard (IEEE 1149.1)
  - allows mixing components from different vendors
  - provides excellent interface to internal circuitry
- Supported by CAD tool vendors, IC & FPGA manufacturers

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- Allows testing of board & system interconnect
  - Back-plane interconnect test w/o using PCB functionality
  - Very high fault coverage for interconnect
- Useful in diagnosis & FMA
  - provides component-level fault isolation
  - allows real-time sampling of devices on board
  - Useful at wafer test (fewer probes needed)
- BS path reconfigured to bypass ICs for faster access

Disadvantages
- Overhead:
  - Logic: about 300 gates/chip for TAP + about 15 gates/pin
- Overall overhead typically small (1-3%)
- but significant for only testing external interconnect
  - especially tri-state (2 cells) & bi-directional buffers
- (3 cells)
  - I/O Pins: 4
- 5 if optional TRST (Test Reset) pin is included
  - Must be included in SoC cores to meet P1500 standards
  - I/O delay penalty
- 1 MUX delay on all input & output pins
  - this can be reduced by design
- Internal scan design cannot have multiple chains
- Cannot test at system clock speed

8 SPECIAL PURPOSE SCAN DESIGN

8.1 Enhanced Scan

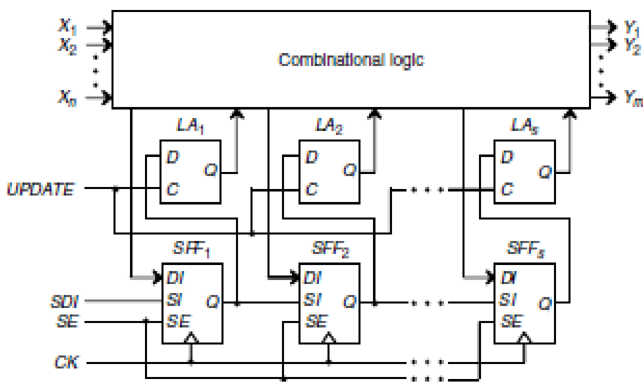

Fig.19 Enhanced scan design

The above figure is the enhanced scan architecture designed using muxed-D scan cells. Initially test vector V_1 is shifted into scan cell (SFF_1 ~ SFF_s) and when the UPDATE =1 it is stored into the latch (LA_1 ~ LA_s). Then the second test vector V_2 is shifted to scan cell when the UPDATE signal is 0. When the test vector V_2 is shifted in, UPDATE signal is shifted in, the UPDATE signal is applied to change V_1 to V_2 and the output response is obtained by applying clock CK.

Advantages:
- Allow to achieve high delay faults coverage using arbitrary pair of test vectors.

Disadvantages:
- Each enhanced scan cell requires an additional scan-hold D-latch.
- Maintaining timing relation is difficult between UPDATE and CK signal.
- Due to many false paths causes over-test problem.

8.2 Snapshot Scan

Snapshot scan design captures the snapshot of the internal states of storage elements used in the design without disrupting the functional operation of the design.

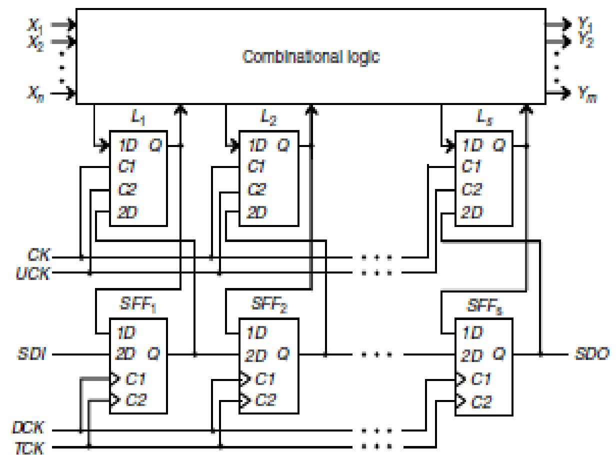

Fig.20 Snapshot scan design

The snapshot scan design architecture performs 4 operations: 1) Test data is shifted in and out of scan cells through SDI and SDO pins using TCK. 2) Test data can be transferred to the system using UCK. 3) Contents of latch can be loaded into the scan flip-flop using DCK. 4) In the normal mode, it uses CK to capture values from the combinational circuit to the system latch. During normal operation, contents of the latch are captured into scan flip-flop by applying DCK.

Advantages
- Observability improved at nonstorage circuit nodes.
- It can improve the circuit diagnostic resolution and silicon debug capability.

Disadvantage
- Increased area overhead.

8.3 Error- Resilient Scan

O_1	O_2	Q
0	0	1
1	1	0
0	1	Previous value retained
1	0	Previous value retained

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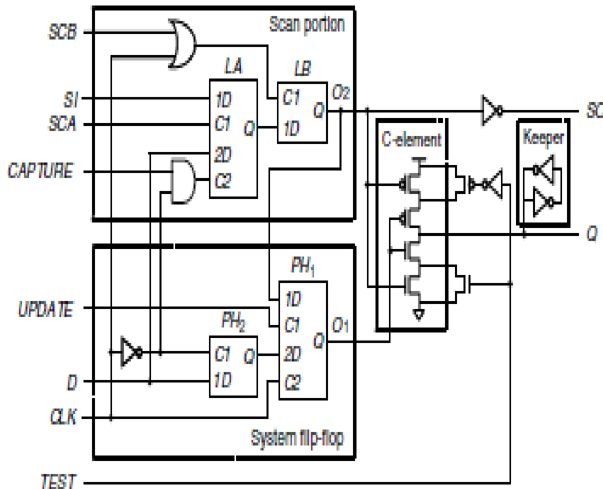


Fig.21 Error resilient scan design

The scan cell consists of flip-flop, a scan portion which is comprised of one-port D latch and two-port D latch, C element and a bus keeper. It operates in two modes: test and system mode. In test mode, TEST =1 and C element acts as an inverter. During shift operation, test vector is applied to the latches LA and LB by applying clocks SCA and SCB and the contents of LB are moved to PH_1 by applying UPDATE clk. During capture operation, CAPTURE=1 and CLK signal is applied which captures the system response.

In system mode, TEST=0, and the C-element acts as a hold-state comparator. The function of the C-element is shown in the Table. When the inputs are unequal, C-element retains its previous value. During this mode, CAPTURE=1 and SCA, SCB, and UPDATE signals are set to 0. When CLK= 0, the output of latches PH_1 and LB hold the previous logic values. When CLK=1, the output of latches PH_2 and LA holds the previous value. If a soft error occurs either at PH_2 or at LA, O_1 and O_2 will have different logic values. If the soft error occurs after the correct logic value passes through the C-element and reaches the bus keeper, the soft error will not propagate to the output Q and the bus keeper will retain the correct logic value at Q.

Built- in self-test (BIST)
Built-in self-test is the ability of the circuit to test itself. BIST techniques can be classified as on-line and off-line BIST.

On-line testing:
In on-line testing, testing occurs during normal functional operating condition.

Concurrent on-line BIST: In concurrent on-line BIST, testing occurs during normal function. This is accomplished by coding techniques or duplication and comparison.

Non-concurrent on-line BIST: Here testing is carried out while the system is in idle state which is accomplished by executing diagnostic firmware routines or diagnostic software routines.

Off-line testing:
In Off-line testing, testing occurs when the system is not carrying out its normal functions. Systems, board and chips can be tested in this mode. This type of testing is carried out using on-chip or on-board test pattern generators (TPG) and output response analyzers (ORA).

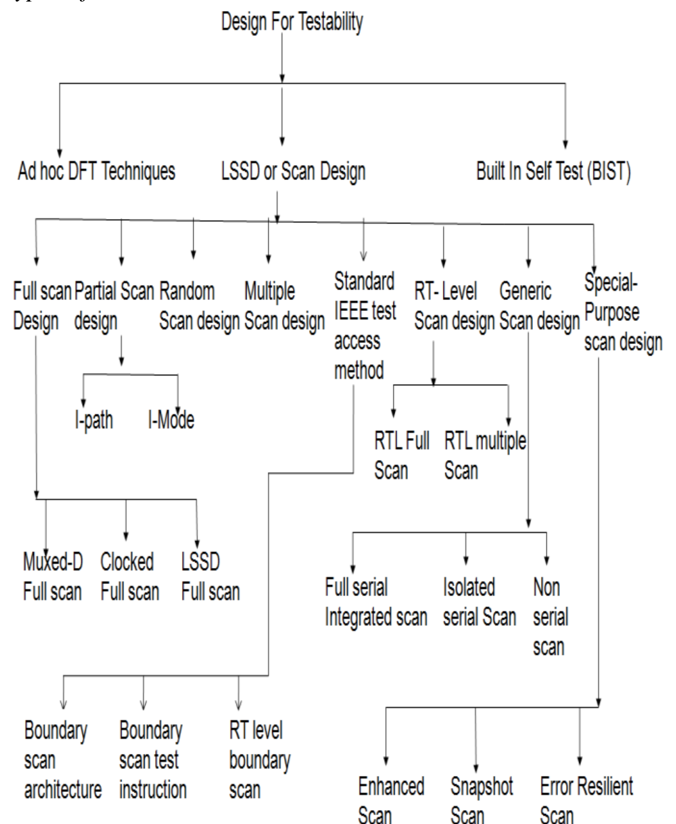
Functional off-line BIST: It deals with the execution of a test based on the functional behavior of the CUT.

Structural off-line BIST: It deals with the execution of a test based on the structure of CUT.

Advantages:
- At-speed testing for delay and stuck-at faults
- Drastic ATE cost reduction
- Field test capability
- Faster diagnosis during system test
- Less effort to design testing process
- Shorter test application times
- Tests can be performed throughout the operational life of the chip
- It can test many units in parallel.
- Better fault coverage

Disadvantages:
- Silicon area overhead
- Access time
- Requires the use of extra pins
- Correctness is not assured.

Types of scan architectures



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International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 6 Issue 11, November - 2017

CONCLUSION

After my in depth technical survey, I found out that, presently VLSI TEST SCAN ARCHITECTURE is not UNIVERSAL, i.e., for a particular design we need to utilise a different type of SCAN ARCHITECTURE or a strategy specific to various types design. Single SCAN cannot be applied to TEST all the types of VLSI DESIGNs.Each of those SCAN ARCHTECTURE types has its own merits, demerits, performance & applications; this has to be further Researched & experimented, as per my ongoing Research work plan.

REFERENCES

[1] Book, “VLSI Test Principal and Architecture”, Wang,Wu,Wen.
[2] Book, “Digital system test and testable design”, Zainalabedin Navabi.
[3] Book, “Digital systems testing and testable design”, Mirron Abramovici, Melvin Breuer, Arthur Friedman.
[4] PPT, Digital testing: scan path design, Based on text by S. Mourad "Priciples of Electronic Systems"

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