Comparitive Analysis of New High Performance Domino Full Adder With Static Full Adder

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***Abstract*— now a days design a low power VLSI circuits are one of the most important constraint. Full adder is one of the important basic blocks of many circuits for multiplication, division, and exponentiation operation. Therefore reduction in power consumption in full adders plays a stringent role in low power VLSI circuits. This paper proposed a domino logic approach to obtain a optimize solution for two constraint power and delay in full adder circuit. Simulations are carried out by Tanner EDA tool using PTM 90nm technology node with 1.1V supply voltage. The results show that proposed 27T domino full adder show 60% faster as compared to 28T static CMOS adder circuit and also it show least power delay product as compared to 28T static CMOS full adder.**

Keywords— Very large scale integration (VLSI), complementary metal oxide semiconductor (CMOS), Power Delay Product (PDP).

I. INTRODUCTION

With continuous increase in the complexity of chips and number of transistors, circuit power consumption is growing in now days. Also with increasing number of portable devices like laptops and mobile phones low power and high speed circuits become important. Full adder act as basic element of various circuits especially used for performing arithmetic operations such as comparator, parity checker compressor and so on hence it receive a lot of attention by researchers.

There are two logic approaches for designing a full adder first is static style and second is dynamic style. Static full adder are more reliable, simpler and low power than dynamic ones but dynamic full adder are more fast and some times more compact than static full adder[1]. On other hand there are lots of issues related to the full adder like power consumption, performance, and area, number of transistor count and noise immunity and good driving ability. There are two major contributions to power consumption in CMOS circuits. One is the active power due to discharging and charging of the circuit capacitances during switching and the other is leakage power due to leakage current.

As we scale down the supply voltage for reducing the power it makes decreasing in threshold voltage (V_t) and gate oxide thickness (t_{ox}) of the transistor which leads to increase in sub-threshold leakage (I_{sub}) current [1]. So many works have been done to decrease transistor count and consequently decrease power consumption and area [2, 3] like low swing technique and the multiple supply technique and the dual V_t technique but these technique helpful to reduced the power consumption, but at the same time they may degrade the speed and weaken the noise immunity of the circuits. In this paper used a mixed style approach called as domino style for designing a 1-bit full adder cell and then compared with static logic based basic 28 transistor full adder cell. In this paper comparative analysis carried out in terms of power, delay and power_delay_product (PDP) for 28T and 27T adder circuits. Voltage-scaling low power technique is used to analyze its effect on power, delay and PDP of the various adder circuits.

II. LOW POWER FULL ADDER DESIGN

There are so many sources of power consumption in any CMOS circuits.[4]

a) Switching Power due to output switching during output transitions.
b) Static Power due to leakage and static current
c) Short Circuit Power during transistor switching due to the current between VDD and GND.

There are several ways to reduce power consumption in CMOS full adder circuits.

1) By minimizing the output and input capacitance to reduce dynamic power.
2) By avoiding using both VDD and GND simultaneously in circuit's components. It can reduce static and short circuit power
3) By using pass transistor in circuit which reduce transistor count in return to reduce power consumption. But sometime pass transistor cannot give strong logic due to threshold loss.
4) By using variable W/L ration to minimize the conduction of transistor which also leads to reduce power of full adder.
5) By reducing the number of transistor to design XNOR and XOR gates power can be reduce in the full adder.
6)

III. 1-BIT FULL ADDER

Static based 1-bit full adder is basic structure for any arithmetical circuit Fig.1 shows the design of basic 1-bit static CMOS full adder, where A, B and C are inputs. Sum and cout are outputs of the full adder and V_{DD} is power supply, for this twenty eight transistors are used to realize sum and carry functions [5].

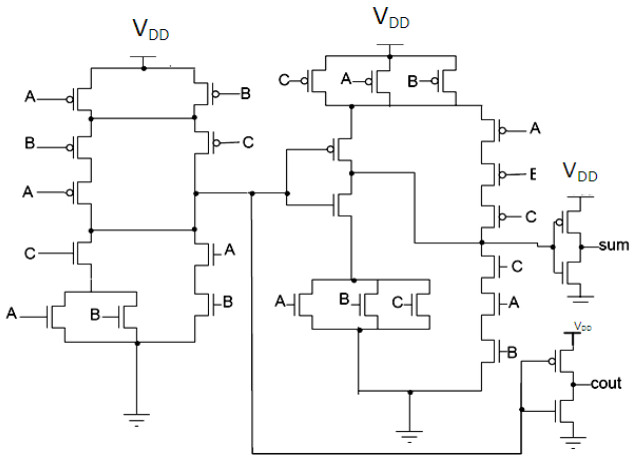

Figure.1. 28 transistor 1-bit full adder (28T).

The second full adder cell realization uses 27 transistors as shown in Fig.2. It has lower delay as compared to static adder circuit having 28 transistor counts. It is based on the 3-transistor implementations of the XOR and XNOR functions presented in, pass transistors, and transmission gates[4]. This circuit has several advantages viz. first it reduce the number of transistor count which decreases the cell area as well as delay. Second, it balances the delays of generating XOR and XNOR, which leads to fewer glitches at the outputs.

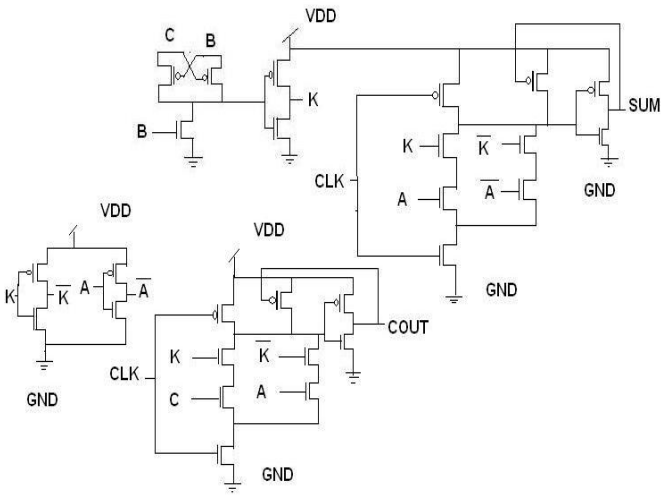

Figure.2. 27 transistor 1-bit Domino full adder

IV. PROPOSED LOGIC APPROACHES AND FULL ADDER

In this section proposed a 27 transistor 1 bit full adder circuit using domino logic as shown in fig 2. As shown in Table 1, the output of full adder cell SUM and COUT can be produced using intermediate signal $K = \overline{B \oplus C}$ or $\overline{K} = B \oplus C$ [4] so

in proposed circuit used a five transistors based one XNOR gate for designing full adder as shown in fig 3. In this Circuit there is no direct path between V_{DD} and GND and discharge of transistor depend on the clock signal. In proposed circuit when Clock is 0 it's a precharging phase at this point dynamic node is charge up to V_{DD}, when clock is 1 known as evaluation phase then according to the input values A,B,C get the output of full adder.. In proposed circuit for designing XNOR gate used static logic but while designing the full adder used a mixed style approach static as well as domino logic style as shown in fig 2, the output of full adder depend on the clock and A,B,C inputs

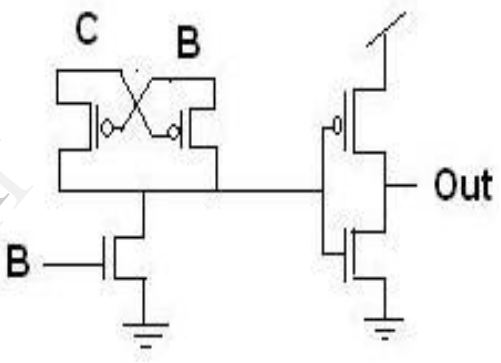

Figure.3. Five transistors XNOR Gate

TABLE 1
TRUTH TABLE FOR THE PROPOSED LOGIC

C	B	A	$\overline{B \oplus C}$	$B \oplus C$	COUT	SUM
0	0	0	1	0	C	A
0	0	1	1	0	C	A
0	1	0	0	1	A	$\bar{A}$
0	1	1	0	1	A	$\bar{A}$
1	0	0	0	1	A	$\bar{A}$
1	0	1	0	1	A	$\bar{A}$
1	1	0	1	0	C	A
1	1	1	1	0	C	A

Power delay product has been calculated from production of delay and average power consumption according to the equation (1)

$$PDP = Power_{Average} \times Delay \quad (1)$$

In the proposed circuit used a transistor length L_{min} = 90nm and Width W for all NMOS transistors is equal to L_{min} and for PMOS transistors is equal to $2L_{min}$. For XNOR gate transistor ratio should be changed in order to optimize glitches in the circuit. All the circuits have been optimized in 1.1 V supply voltage and 20 MHz input frequency conditions. To make fair
comparison these conditions has been made same for all circuits as.

V. RESULTS AND DISCUSSION

A. *Output waveforms*

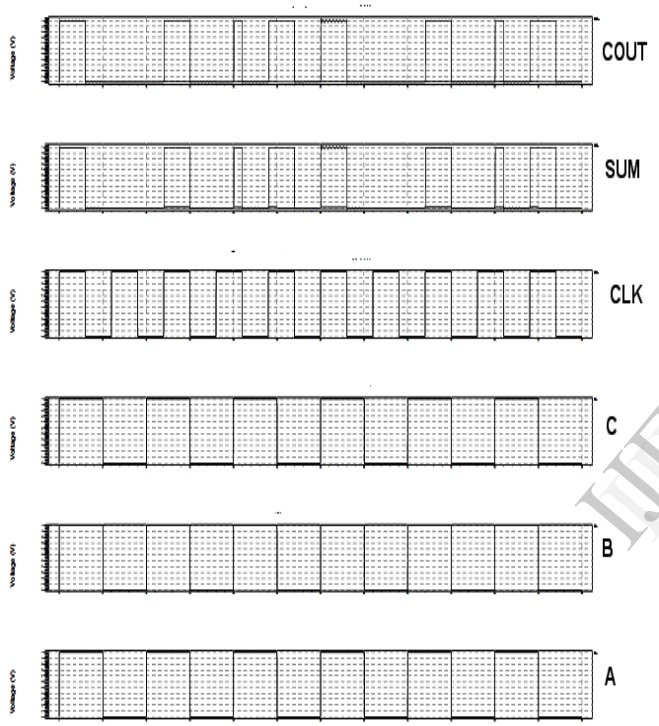

Figure.4. Input and output waveform of proposed 27T domino full adder

B. *Power Comparison*

In this section, discussed the effect of supply voltage variation vs power, delay and PDP.For analysis supply voltage ranges from 1V to 1.16V has been considered. Each circuit has been tested on same input patterns. The comparative analysis is carried out by using 90nm technology node. The simulation has been carried out using Tanner EDA tool and PTM BSIM4 MOS models [15-16]. The results of different adder circuits reveal that power, delay and power_delay_product at different supply voltage. Power delay product is considered here to check the energy efficient circuit design and results show the advantages or disadvantages of lowering the number of transistors. Fig.5 shows variation of average power with supply voltage variation at 90nm technology node. 27T adder shows its superiority over 28T adder but in terms of area centric design 28 transistor is superior. At 1.1V 27T adder give power dissipation of 0.7054µW and 28T adder give 0.4719µW power dissipation.
As per from TABLE 2 included that at 1.1V 27T adder uses approximately 1.49X more power than 28T adder.a

TABLE 2
POWER Vs SUPPLY VOLTAGE

		Power (µW)	
S. No	Supply Voltage(V)	28T Static Full Adder	27T Domino Full Adder
1	1	0.3922	0.50115
2	1.02	0.4348	0.5308
3	1.04	0.4733	0.576
4	1.06	0.4872	0.6232
5	1.08	0.464	0.6496
6	1.1	0.4719	0.7054
7	1.12	0.494	0.7259
8	1.14	0.5038	0.74206
9	1.16	0.5419	0.7962

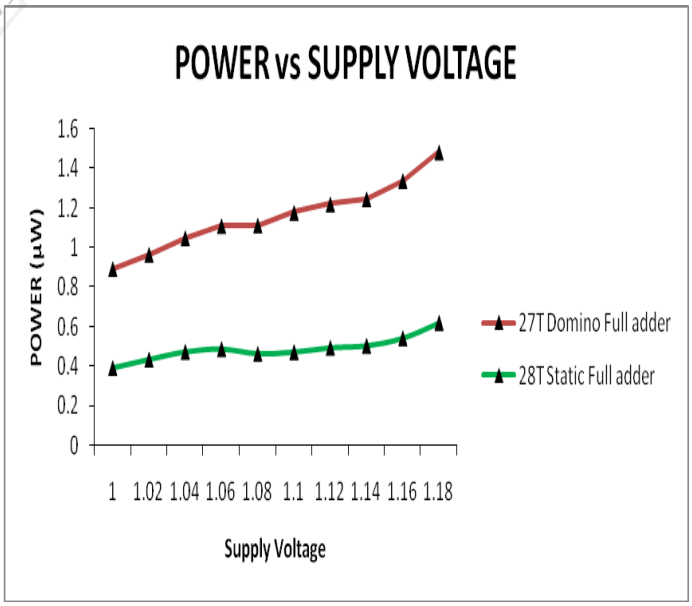

Figure.5. Variation of average power with supply voltage for different adders at 90nm technology.

Figure.6 depicts the delay of two adder circuits with supply voltage variation at 90nm technology node.Both full adder circuits shows approximately constant delay with varitation of supply voltage but in proposed full adder circuit delay is less as compared to static full adder. At 1.1V 27T adder shows minimum delay ie 30.963 ns where as in 28T adder it

50.75ns you can seen in TABLE 3. At higher V_{DD} of 1.16V 27T adder shows minimum delay of 30.66 ns.

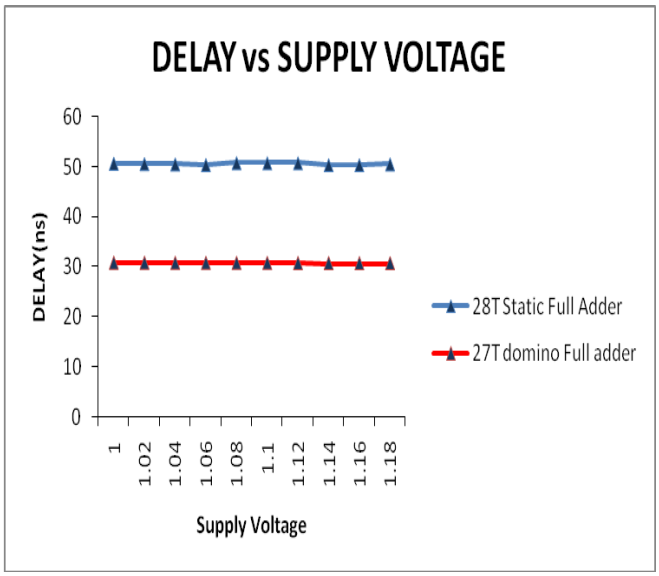

Figure.6. Variation of delay with different supply voltage for different adders at 90nm technology.

TABLE 3
DELAY Vs SUPPLY VOLTAGE

		Delay (ns)	
S. No	Supply Voltage (V)	28T Static Full Adder	27T Domino Full Adder
1	1	50.654	30.74
2	1.02	50.586	30.73
3	1.04	50.503	30.71
4	1.06	50.401	30.703
5	1.08	50.76	30.702
6	1.1	50.75	30.693
7	1.12	50.74	30.685
8	1.14	50.37	30.676
9	1.16	50.36	30.66

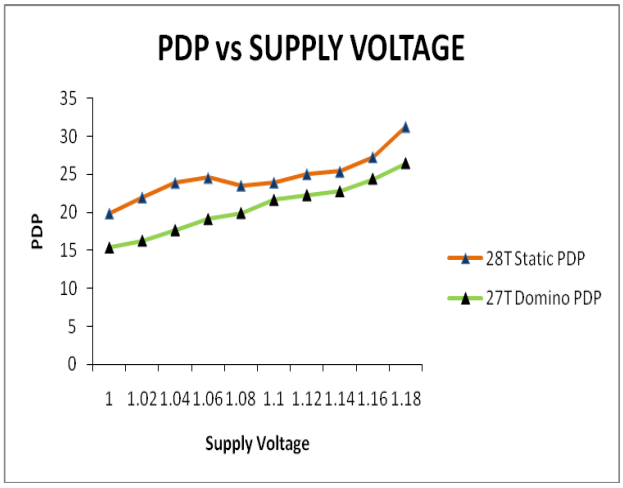

Figure.7. PDP for different adders at different supply voltage at 90nm technology.

TABLE 4
PDP Vs SUPPLY VOLTAGE

		PDP	
S. No	Supply Voltage (V)	28T Static Full Adder	27T Domino Full Adder
1	1	19.8664988	15.405351
2	1.02	21.9947928	16.311484
3	1.04	23.9030699	17.68896
4	1.06	24.5553672	19.1341096
5	1.08	23.55264	19.9440192
6	1.1	23.948925	21.6508422
7	1.12	25.06556	22.2742415
8	1.14	25.376406	22.76343256
9	1.16	27.290084	24.411492

Figure.7 depicts PDP of different adder circuits for supply voltage variation at 90nm technology node. 27T adder shows less PDP as compared to 28T as shown in TABLE 3. 27T adder shows minimum PDP of 15.40 at 1V and 28T adder shows PDP of 18.866 at this volatge.From TABLE 3and Fig 7 we can say that 27T adder circuit more ast compared to 28T adder circuit and 27T adder give PDP in range of 15.40 to 24.411 where as 28T give PDP in range of 19.866 to 27.29.

VI. CONCLUSIONS

In this paper different low-power adder circuits have been analyzed in terms of power, delay and power delay product. It has been included that 28T adder circuit shows less power dissipation as compared to 27T Domino full adder circuit but if we compare area constraint and transistor count that minimum in 27T adder circuit. As domino logic based circuit dissipate more power as compared to static logic [11] but still optimizing a power in proposed circuit, it dissipate 1.49X more power as compared to 28T adder circuit at 1.1v supply

voltage. If we talked about in terms of delay 27T adder show least delay and PDP as compared to 28T adder circuit. Finally, it is concluded that 27T adder is better in terms of delay and PDP as compared to 28T adder circuits for highly scaled 90nm technology nodes. Proposed circuit is 60% more faster as compared to 28T adder.

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