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Comparison of Multipliers for VLSI Application

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Abstract— Multipliers are very important component in Digital Signal Processing Systems and Embedded application. The performance of any multiplier will depend upon power, delay and area. Recent works in VLSI Design to reduce significant amount of Multiplier's power consumption. Multipliers perform one of the most frequently arithmetic operations. This spurious switching activity can be mitigated by balancing internal paths through combination of architectural and transistor-level optimization techniques. In this paper, deals with comparison of different multipliers are done for low power requirement. The power management has become a great concern due to the increased usage of multimedia devices. Multipliers are the main sources of power consumption in these devices. The area and speed of the multiplier is an important issue, increment in speed results in large area consumption and vice versa.

Keywords— Partial Products, Digital Signal Processing, Multiplicand, Multiplier, Booth Algorithm.

INTRODUCTION

With the recent trends in increasing mobility and performance in small hand-held mobile communication and portable devices, among three thrust areas i.e speed, area and power, speed has become one of the significance in modern VLSI design. The objective of good multiplier to provide a physically compact high speed and low power consumption unit. Being a core part of arithmetic processing unit multipliers are in extremely high demand on its speed and low power consumption.

To reduce significant power consumption of multiplier design it is a good direction to reduce number of operations thereby reducing a dynamic power which is a major part of total power dissipation. In the past considerable effort were put into designing multiplier in VLSI in this direction. Parallel multipliers are used to speed up the processors compared to serial multipliers

Multipliers perform one of the most frequently encountered arithmetic operations in digital signal processors (DSPs). For embedded applications, it has become essential to design more power-aware multipliers. The power aware of multipliers uses new technology called Multi precision which include some characteristics (i) non negligible silicon and power overhead,(ii)Performance and throughput reduction brought by the shut-down of parts of the circuit and/or use of reduced supply voltage and(iii) restriction and great margins to the operating condition versatility of the multiplier. High

performance energy efficient logic style is having crucial importance in VLSI circuits. Multiplication in hardware can be implemented in two ways either by using more hardware for achieving fast execution or by using less hardware and end with slow execution [3]. Traditional hardware multiplication is performed in the same way multiplication is done by hand: partial products are computed, shifted appropriately, and summed. In this paper compare the performance of three multiplier structure like array multiplier, Booth multiplier and Wallace tree Multiplier. In all those technique

Booth Algorithm having superior Performance Parameter. This algorithm can be slow if there are many partial products (i.e. many bits) because the output must wait until each sum is performed. Booth's algorithm cuts the number of required partial products in half. This increases the speed by reducing the total number of partial product sums that must take place.

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1

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$$a + b = \gamma \tag{1}$$

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2

An excellent style manual for science writers is [7].

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TABLE I. TABLE STYLES

Table Head	Table Column Head		
	Table column subhead	Subhead	Subhead
copy	More table copy ^a		

a. Sample of a Table footnote. (Table footnote)

ь.

Fig. 1. Example of a figure caption. (figure caption)

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