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Comparison of Level Shifting Modulation Techniques using Designed Seven Level Multilevel Inverter

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***Abstract*- With rapid development of high voltage and high power applications, multilevel inverter plays a critical role. With conventional power inverter, one may have high switching losses and more THD. In order to reduce switching losses and THD, a new inverter topology with seven level output voltage is proposed with less number of switches. In this paper, various level shifting modulation techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) are compared along with individual THD analysis and the same were used for the generation of required pulses with the help of MATALB/SIMULINK.**

Keywords- Multi Level Inverter; THD; reduced number of switches; Logic gates; PD; POD; APOD.

I. INTRODUCTION

Power Electronic devices are used for power conversion and power conditioning at various frequencies. In general, traditional inverter is used for DC to AC conversion for different applications like solar, wind, Hybrid Electric Vehicles and which are associated with high voltage systems. With the help of Multi Level Inverter (MLI) [1], we can generate high level of voltages which are very near to sinusoidal and even very low distortions in input voltages cannot interrupt inverter output waveform. Similarly, we can feed the same output to different types of rotating machines [2]. Generally, Conventional MLI are of different configurations such as Diode Clamped, Flying Capacitor, Cascaded H Bridge which consisting of high number of switches, capacitors and diodes which may result in more switching losses with less reliability. In general, to obtain more level of voltages, more number of dc voltage sources are required or one can take help of dc capacitors to increase the level of voltages. So, taking less number of voltage sources is focused much in recent trends. Proper selection of number of sources, switches, capacitors, diodes are also taken into account before designing any Multi level Inverter with various configurations and various available modulation techniques. However, detailed number of dc sources, switches, capacitors, linear and non linear devices are tabulated [3] in Table:1.

Hence, Various configurations are proposed with symmetric and Asymmetric dc voltages are presented in many papers. After careful investigation [4]-[7] on available resources and papers, we propose a new design of MLI using only six switches. Out of six switches, two switches were used for level generation and the remaining four are used for polarization in the form of H Bridge. Generation of switching pulses is done with the help of different types of logic gates.

Table:1 Required components for MLI

Type of MLI	No. of dc sources	No. of Switches	No. of capacitors	Clamping Capacitors	Clamping diodes
Diode-clamped	1	2*(L-1)	(L-1)	-	(L-1)*(L-2)
Flying capacitor	1	2*(L-1)	(L-1)	(L-1)*(L-2)/2	-
Cascaded H Bridge	(L-1)/2	4*(L-1)/2	-	-	-

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II. PROPOSED MLI

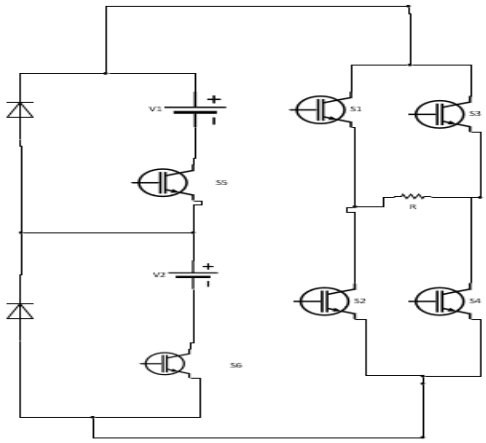

Fig: 1 proposed circuit

A proposed Multi Level Inverter (MLI) is designed in such a way that it can produce seven level of output voltage with less switching losses, less distortions in output.
It consisting of only two Asymmetric dc voltage sources V_1 and V_2 in the ratio of 1:2 format which are enough to generate such seven levels of output voltage and six power semi conducting devices as shown in fig.1. Out of them, two switches S5, S6 are used as auxiliary switches in order to get different output voltage levels with the help of non linear devices i.e., diodes D_5, D_6 which are connected in parallel with the combination of dc voltage source and switch. Remaining four switches S_1, S_2, S_3, S_4 at the right half of the circuit forms a Cascaded H bridge, which is used for generating positive and negative half cycles. In Cascaded H bridge, S_1 and S_4 are responsible for generating positive half cycle and similarly S_2, S_3 are responsible for negative level of voltages.

III. MODULATION TECHNIQUES:

In many Industrial and power applications, various modulation techniques are adopted in order to generate desired pulses. Some of the modulation techniques are Single Pulse Width Modulation, Multiple Pulse Width Modulation, Sinusoidal pulse Width Modulation, Modified pulse Width Modulation, phase displacement control, Advanced pulse Width Modulation techniques such as trapezoidal modulation, Staircase modulation, Stepped modulation, Harmonic injection modulation, delta modulation. Among all the existing techniques, the proposed circuit makes use of sinusoidal PWM which is very common. This technique is preferred due to the variation of each pulse width in proportion with the amplitude of sinusoidal signal.

Desired gating signals are obtained by comparing sinusoidal (Reference) with Triangular (Carrier) signals. As the proposed circuit is designed for seven level of output voltage, we require (L-1) carrier signals along with level shifting as these are associated with output voltage levels (L). To generate level shifting pulses, there are different techniques which are presented in various papers [8] [9].

After detailed study, three techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition are discussed in this paper.

Phase Disposition (PD) PWM technique has carriers in same phase above and below zero reference line as shown in the fig. 2. This method provides low THD along with fundamental frequency.

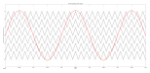

Fig. 2 Phase Disposition (PD) signals

Phase Opposition Disposition (POD) PWM has carriers with zero degree displacement above the Zero reference line and exact 180 degree displacement below Zero reference line as shown in the fig.3

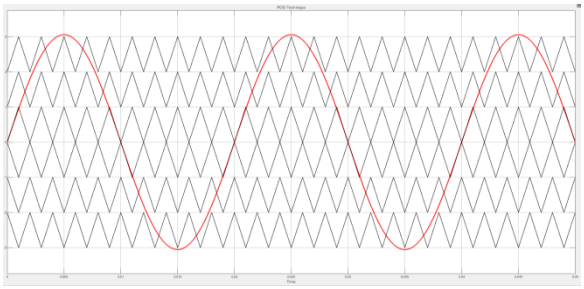

Fig. 3 Phase Opposition Disposition (POD) Signals

Similarly, Alternate Phase Opposition Disposition (APOD) PWM has carrier signal arrangement in such a way that each carrier signal is having 180 degree phase displacement with the other carrier signal as shown in the fig.4

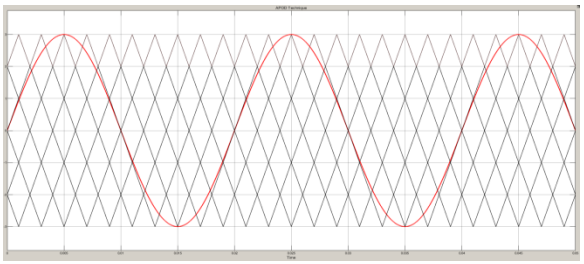

Fig. 4 Alternate Phase Opposition Disposition (APOD) Signals

IV. LOGICAL SEQUENCE FOR SWITCHING:

As proposed circuit requires 6 triangular carrier signals as the system is designed for seven level output voltage. Here, one full cycle is divided for seven level output voltage as shown in fig.5.

The number of total divisions per one full cycle and the time divisions are presented as given below.

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Frequency of the proposed system (f) =50Hz.
Time period for one full cycle (t) = (1/f) =0.02 sec
Number of total divisions/ 1full cycle (D_t) = (L*2)+2.
Time divisions of each D_t (t_d) = [(L*2)+2]/t.
In most of the available technical papers, it was discussed about different Multi level inverter configurations with reduced number of switches and their switching states. But however most of the papers were not presented in detail about how logical gates are selected and the logic behind the switching of particular design.

In this paper, the technical explanation along with logical relation between the generated pulses which are done by using modulation strategies and pulses which are required for the proper switching sequence is clearly presented. By taking conventional BCD binary coded representation as reference, different pulse patterns for 6 triangular carrier signals and different available switches in the proposed circuit such as S_1, S_2, S_3, S_4, S_5, S_6 are tabulated clearly in the below table:2.

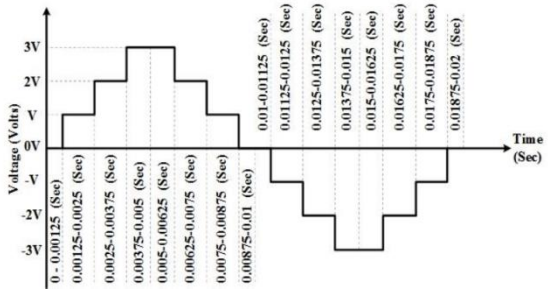

Fig. 5 Time division of one full cycle or 7 level MLI

Time divisions (secs)	Voltages	P3	P2	P1	N1	N2	N3	S5	S6	S1	S2	S3	S4
0-0.00125	**0V**	0	0	0	1	1	1	0	0	1	0	0	1
0.00125-0.0025	**+1V**	0	0	1	1	1	1	1	0	1	0	0	1
0.0025-0.00375	**+2V**	0	1	1	1	1	1	0	1	1	0	0	1
0.00375-0.005	**+3V**	1	1	1	1	1	1	1	1	1	0	0	1
0.005-0.00625	**+3V**	1	1	1	1	1	1	1	1	1	0	0	1
0.00625-0.0075	**+2V**	0	1	1	1	1	1	0	1	1	0	0	1
0.0075-0.00875	**+1V**	0	0	1	1	1	1	1	0	1	0	0	1
0.00875-0.01	**0V**	0	0	0	1	1	1	0	0	1	0	0	1
0.01-0.01125	**0V**	0	0	0	1	1	1	0	0	0	1	1	0
0.01125-0.0125	**-1V**	0	0	0	0	1	1	1	0	0	1	1	0
0.0125-0.01375	**-2V**	0	0	0	0	0	1	0	1	0	1	1	0
0.01375-0.015	**-3V**	0	0	0	0	0	0	1	1	0	1	1	0
0.015-0.01625	**-3V**	0	0	0	0	0	0	1	1	0	1	1	0
0.01625-0.0175	**-2V**	0	0	0	0	0	1	0	1	0	1	1	0
0.0175-0.01875	**-1V**	0	0	0	0	1	1	1	0	0	1	1	0
0.01875-0.02	**0V**	0	0	0	1	1	1	0	0	0	1	1	0

Table:2 Logical Switching Sequence for proposed circuit

In order to design logical gated sequence for switch S_5, Consider one full cycle for the purpose of analysis. The time period of modulating sinusoidal signal for one full cycle is 0.02 seconds. Whereas the carrier signal frequency is chosen as 2KHz. To get the positive logical gate circuit for switch S5, observe P3, P2, P1 pulses and for negative logical gate circuit take N1, N2, N3 pulses into account. By examining different combinations of logical gates such as AND, OR, NAND, EXOR, EXNOR, NOT implement the complete logical sequence circuit for switch S_5 which is shown in the fig.6 below by using different combinations of logical gates.

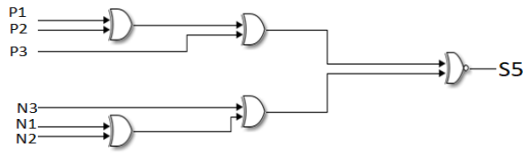

Fig:6 Logical circuit for S5

Similarly, for S_6 on careful analysis implement the logical circuit for S6 as shown in the fig. 7.

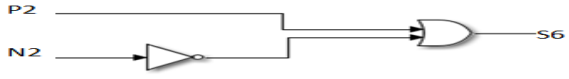

Fig. 7 Logical circuit for S6

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These Obtained logical gates S5 and S6 are fed directly to the switches in order to generate level shifting voltage levels.

V. SIMULATION RESULTS

The proposed multi level inverter is designed with the help of MATLAB software as shown in the fig.8 below.

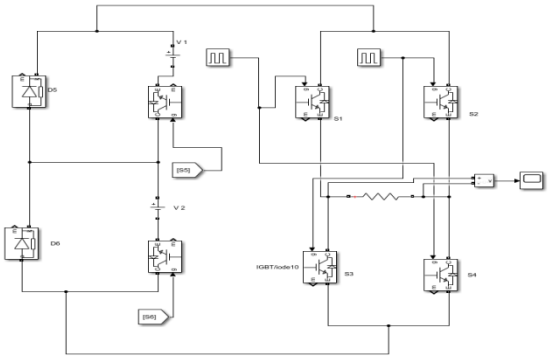

Fig: 8 Proposed 7-level MLI

The gating pulses to the above circuit can be given by using PD, POD, APOD techniques with the same load. However irrespective of any technique, the produced gating pulses will be almost similar. The gating circuit along with gating pulses are as shown in the fig.9, fig.10 below.

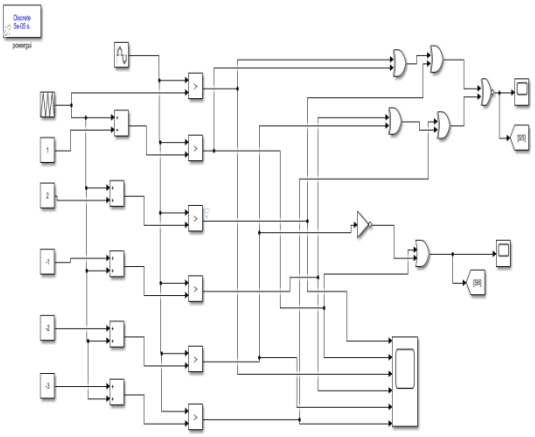

Fig: 9 Gating circuit for proposed MLI

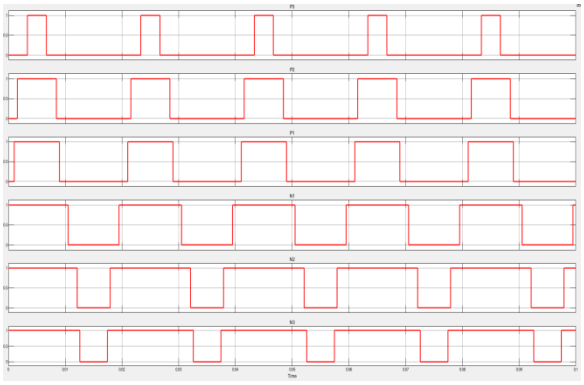

Fig: 10 Gating pulses

From the designed MLI, the seven level output voltage is obtained as shown in the fig.11 below

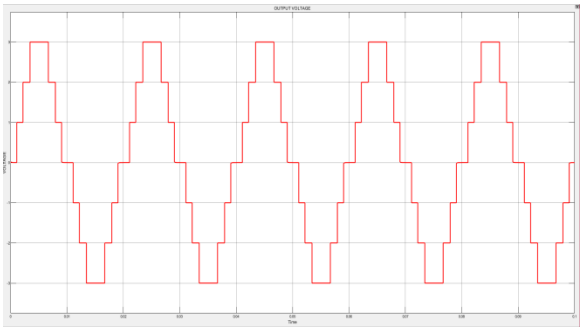

Fig: 11 7 level Output voltage

VI. THD ANALYSIS BY PD, POD, APOD TECHNIQUES

The proposed MLI is executed by using three techniques such as PD, POD, APOD individually and harmonic content of each technique is captured and presented below in the fig.12, 13, 14 below.

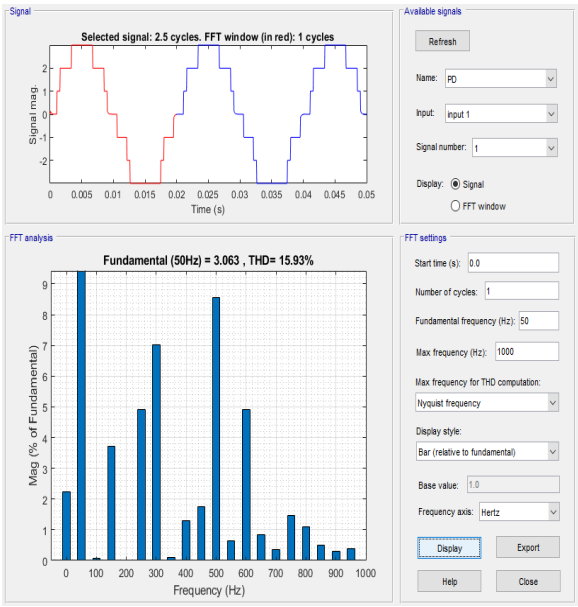

Fig: 12 THD Analysis of PD technique

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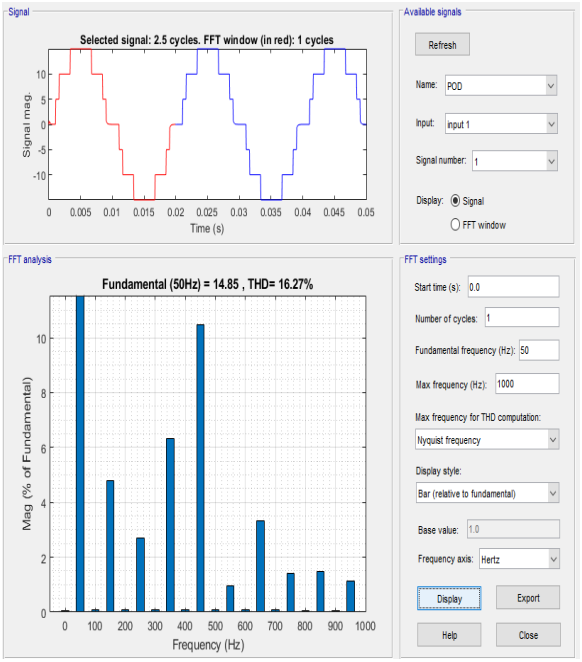

Fig: 13. THD Analysis of POD technique

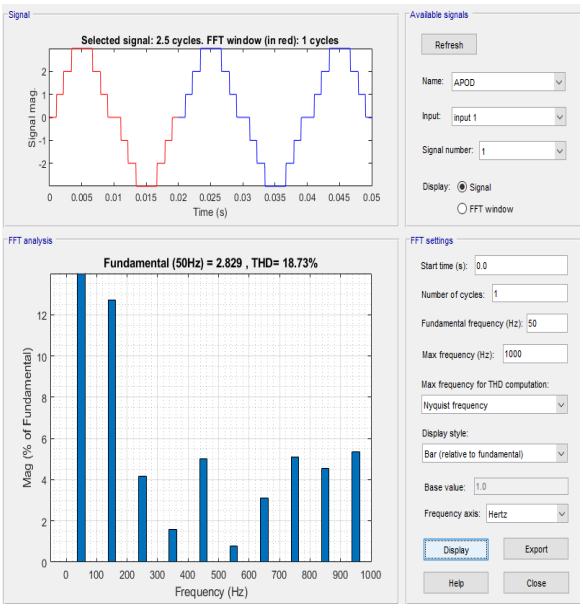

Fig: 14 THD Analysis of APOD Technique

On observing all the above methods, a comparative study is done and the values are tabulated in table:3 given below.

TABLE:3 Comparison of PD, POD, APOD techniques

Technique	Fundamental frequency	THD (%)
PD	3.063	15.93
POD	14.85	16.28
APOD	2.83	18.49

VII. CONCLUSION AND FUTURE SCOPE:

The proposed model provides 7 level output voltage with less distortions and gating pulses generated here are more reliable with simple logical gates. As generation of different harmonics can affect the circuit, detailed study is performed by using different techniques. On Careful investigation of all the above techniques Phase Disposition (PD) gives less THD as compared to POD and APOD techniques. The same work can be extended for solar applications [10] using PV panels; Battery based applications like Hybrid Electric Vehicles.

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