Comparision and Analysis of Different Types of Low Power Techniques with Drdaal(Dual Rail Domino With Asynchronous Adiabatic Logic) Full Adder

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Abstract:-**As low power circuits are most popular now a days as the scaling increases the leakage power in thecircuit also increases rapidly, so for removing these kind of leakages and to provide better power efficiency, we are using different types of low power techniques. In this paper we are going to analyze the different types low power VLSI design techniques with DRDAAL full adder. In this work,a low power techniques with DRDAAL full adder (Dual-Rail Domino with Asynchronous Adiabatic Logic) is designed and simulated, which exhibits better power-delay product and reliable logical operations.To improve the speed of circuits, dual-rail domino logic is introduced. The power-delay product of the proposed designs is compared withthe DRDAAL full adder (Dual Rail Domino with Asynchronous Adiabatic Logic). Simulation results show better power-delay product characteristics for clock rate 50MHz to 500MHz.**

Keywords – ***Asynchronous adiabatic logic, Full adder, Sleepy Stack Technique, Power-Delay product***

I. INTRODUCTION

In recent years, low-power design is becoming a crucial design objective due to the growing demand on portable electronics devices. Over the past few decades, design of low power techniques have steadily accelerated the list of VLSI researcher's design concerns, in terms of rising cost of energy, an increasing sensitivity to greenpractices, and low power consumption. Moore's law describes the requirement of the transistors for VLSIdesign; it gives the empirical observation that component density and performance of integrated circuits, doubles every year, which was then revised to doubling every two years. Transistor count is a major concern which largely affects the design complexity of many function units such as full adders and multipliers. Full adder is an important module in digital signal processors and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication and division Thus, the design of an energy efficient full adder cell is of great interest [1].

In recent years, the literatures have brought out several types and designs of low power techniques, namely,dual stack technique,[3], [4] and sleepy stack technique, [2]which achieved considerableenergy saving compared with DRDAAL full adder is discussed and detailed in further sections.

II. OVERVIEW OF DRDAAL FULL ADDER

The main objective paper is to design and implementation of full adder using asynchronous adiabatic logic with dual - rail

domino logic. The basic idea of the proposed scheme for designing full adder cell isillustrated in Fig.-1.The overall system consists of two main blocks, namely logical block and control andregeneration (C&R) block. As opposed to the conventional synchronous adiabatic circuits, instead ofdriving each adiabatic logic unit with an externally supplied clock phase, each block is controlled andpowered using the control signal generated by the C&R block with the help of the logical output of the previousstage, which at the same time is the input to the current logical stage. The power clock design is a majorcomplication to the design of VLSI circuits, because the whole transistor logic system shares the power clock, then the power clock switching circuit will dissipate the most power in the logic.

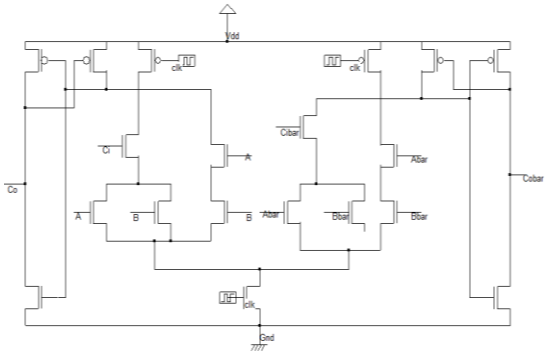
The simple structure of the pass-transistor logic makes it easy to tweak the sizing of transistors to get thedesired charging and discharging time and hence the slope of the output control signal minimizes the power.In asynchronous clock system, the clock energy is locally stored in the C&R block and it has been used forsubsequent gates, the loss of energy of each operation will be taken from its clock source.Data out signal of any logical block is not only going into next logical block as data input, but at the same time, it is used to generate a control signal for the next logical block using C&R block [8]. The construction of the C&R promotes the local storage of the energy and switching circuit for the recovery. This technique will help us to save the required power clock generator with less power. The local regeneration stores the intermediate energy and supplies to the required next level of logic operations. Even though the initial requirement of power from the clock generator remains same, after power up the logical sequence, power taken from the power clock is reduced dramatically.

A. Dual-Rail Domino Logic

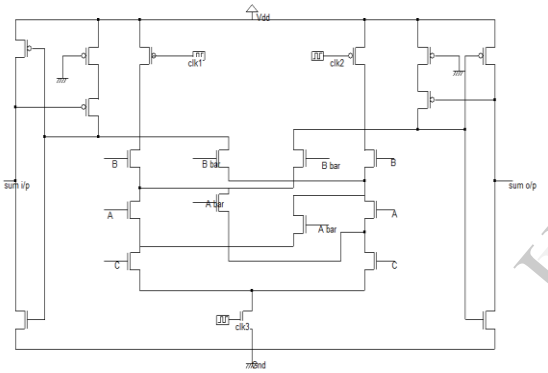
Dual-Rail Domino Logic (DRDL) is a pre-charged technique which is used to improve the speed of CMOS

circuits. It exhibits a low delay; it is usually used in highperformance circuits. DRDL full adder cell is shown inFig.:-1. It is based on an NMOS pull-down network and a PMOS pair, driven by the clock, which brings the gate in the pre-charge or evaluation mode. The output inverters ensure that no race occur, while the weak feedback PMOS transistors allow to reduce the charge-redistribution problemincreases the noise immunity. The major scope of the dynamic, pre-charged design styles over the static styles is

Is that they eliminate the spurious transitions and the corresponding power dissipation [6], [7], [9].



(a)



(b)

Fig.-1Dual-rail domino full adder (a) C_{out} (b) Sum

B. *Dual-Rail Domino with Asynchronous Adiabatic Logic (DRDAAL)*

Asynchronous adiabatic full adder design uses dualrail domino logical blocks with C&R structures. It hasbeen designed and tested to get the energy efficiency out of the proposed system. A simple implementation of the proposed system is depicted in the Fig. 2. It is a full adder cell, with the logical part designed using DRDAAL, and whereas the control part of the C&R block and regeneration part is made of pass-transistor logic. This pass transistor logic is functioning as transmission gate in the output logic of each gate structure.

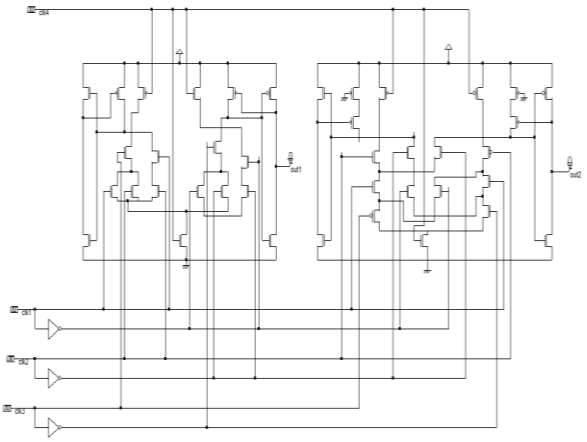


Fig.-2 DRDAAL full adder schematic diagram

III. PROPOSED LOW POWER TECHNIQUES WITH DRDAAL FULL ADDER DESIGN

A. *Low power techniques with DRDAAL full adder*

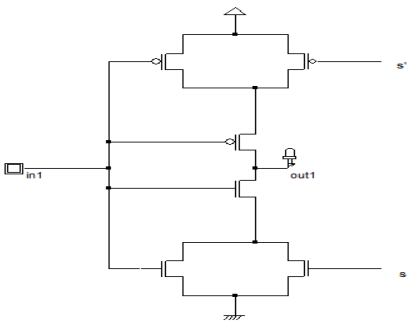


Fig.:-3Sleepy stack Technique

The sleepy stack technique shown in Fig.-3, combines the sleep and stack approaches [3], [4]. The sleepy stack techniquedivides existing transistors into two half Size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistorsand since additional wires are added for S and S', which are sleep signals.

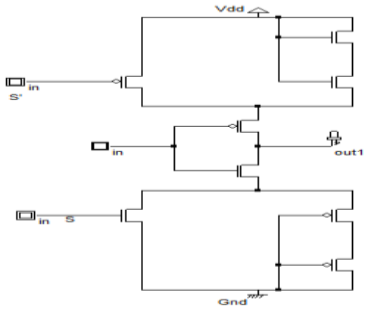


Fig.-4Dual Stack Technique

Thetechnique is dual stack approach [2],is shown in Fig.-4. Insleep mode, the sleep transistors are off, i.e. transistor N1 andP1 are off. We do so by making S=0 and hence S'=1. Now wesee that the other 4 transistors P2, P3 and N2, N3 connect themain circuit with power rail. Here we use 2 PMOS in the pulldownnetwork and 2 NMOS in the pull-up network. Theadvantage is that NMOS degrades the high logic level whilePMOS degrades the low logic level. Due to the body effect,they further decrease the voltage level. So, the pass transistorsdecreases the voltage applied across the main circuit. As weknow that static power is proportional to the voltage applied,with the reduced voltage the power decreases but we get theadvantage of state retention. Another advantage is got duringoff mode if we increase the threshold voltage of N2, N3 andP2, P3. The transistors are held in reverse body bias. As aresult their threshold is high. High threshold voltage causeslow leakage current and hence low leakage power. If we useminimum size transistors, i.e. aspect ratio of 1, we again get low power due to low leakage current. As a result of stacking, P2 and N2 have less drain voltage. So the DIBL

effect is less for them and they cause high barrier for leakage current. While in active mode i.e. S=1 and S'=0, both the sleep transistors (N1 add P1) and the parallel (N2, N3 and P2, P3) are on They work as.transmission gate and the power connection is again established in uncorrupted way. Further they decreases the dynamic power consumption.

IV. SIMULATION RESULTS AND ANALYSIS

Low power techniques with DRDAAL full adder have been implemented. DRDL is introduced to improve speed performance in the circuits. It also exhibits a low delay. Domino logic has betterpower-delay product characteristics. The simulation results of the proposed low power technique with DRDAAL full adder are presented in Fig.-5.For the various frequency ranges, the (Power Delay Product)PDP of the proposed designs is compared with the low power techniques with DRDAAL and DRDAAL full adder design, reported in Table 1.

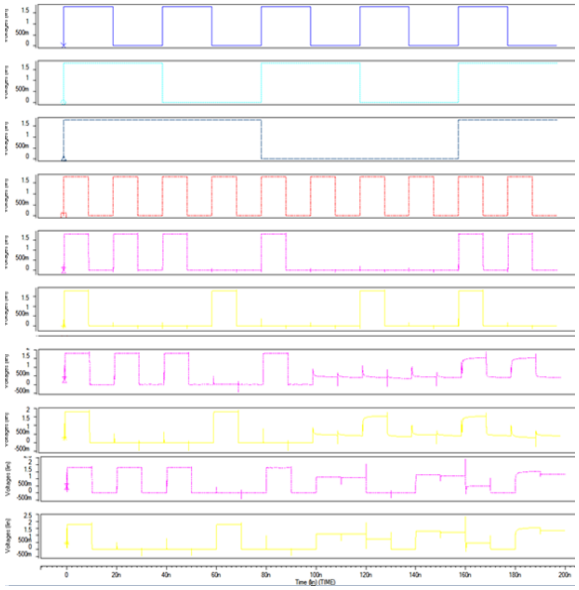


Fig.-5 Low power techniques with DRDAAL full adder Simulation Results

Compared with low power techniques with DRDAAL full adder implementation and DRDAAL full adder of fulladder cell designs, the proposed design achieves better PDP characteristics. The low power techniques with DRDAAL full adder design is studied at90nm CMOS process technology. DSCH Tool and HSPICE support is used for simulation. PDP versus frequency comparison analysis is shown in the Fig-6.

TABLE 1.POWER DELAY PRODUCT OF VARIOUS DRDAAL FULL ADDERS

Power Delay Product (PDP)	**Circuit Technique**	**Frequency(MHz)**			
		50	100	200	500
	DRDAAL Full Adder	2.4477	4.1738	7.6302	4.8018
	Dual Stack Technique	2.7223	2.3006	2.505	9.549
	Sleepy Stack Technique	1.9534	3.1938	4.6556	5.2822

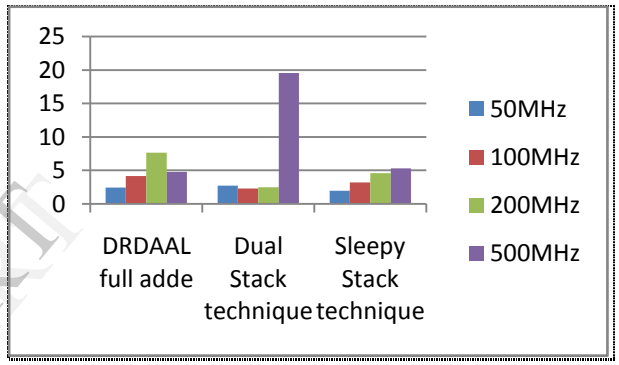


Fig.-6 PDP Vs. Frequency comparison

V. CONCLUSION

In this paper we have presented a novel methodology for designing the low power techniques with DRDAAL full adder. Dual-Rail Domino Logic (DRDL) is a pre-charged technique which is used to improve the speed of CMOS circuits. This technique is combined with asynchronous adiabatic logic (AAL) design technique to obtain the energy saving benefits in the full adder circuit. The performance of power-delay product (PDP) characteristics of this design is compared with the low power techniques with DRDAAL full adder and DRDAAL full adder. PDP is observed for frequencies between 50MHz to 500MHz. The Sleepy Stack technique has better PDP than the DRDAAL full adder .This approach confirms the feasibility of different low power techniques with DRDAAL full adder in low power computing applications.

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