Comparative Study of Space Vector Pulse Width Modulation based T-Type Three-level Inverter

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***Abstract*—A three-phase T-type three-level inverter configuration is demonstrated. Analysis of suggested three-level inverter has been presented. An improved three-level space vector pulse-width modulation technique, which utilize the state redundancies has been explained and verified over recommended three-level inverter and neutral point clamped inverter under linear range of operation. Modelling and simulation of T-type three-level inverter using presented space vector pulse width modulation is carried out in MATLAB/SIMULINK environment and results are presented. Proposed inverter is also compared with other configurations.**

Keywords — Space vector pulse width modulation; T-type Inverter; total harmonic distortion; multi-level inverter.

I. INTRODUCTION

Multilevel inverter (MLI) was first introduced by Baker and Bannister in the year 1975 [1-2]. It came after the limitations of two-level inverter such as higher total harmonic distortion (THD), high switching frequency, high dv/dt losses, higher commutation problem and higher rating devices. Multilevel inverter can produce any desired higher output voltage by incorporating small DC sources. Application of multilevel inverter includes industrial drive control, renewable energy system, HVDC, STATCOM etc. [3-7].

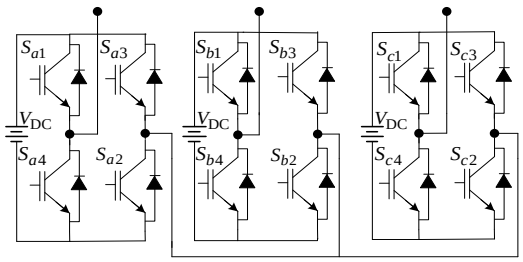
Some early introduced multilevel inverters such as Cascaded H-bridge (CHB) [2], Neutral Point clamped (NPC) [8] and Flying Capacitor (FC) [9] are termed as classical inverter due to.an extensive application in research and industries. A single cell of H-bridge inverter have a DC-source with four switches, combination of such cell can produce any output voltage level by cascading the cells. Of H-bridge inverter is popular for multilevel application with photovoltaic (PV) as it require isolated sources. Larger number of DC source for higher level is the limitation for H-bridge multilevel inverter. An inverter where one DC source with extra diodes connected to the neutral point thus avoiding use of larger number of DC source as earlier and this structure named as neutral point clamped (NPC) inverter. Large number of Diode restricts the application of NPC with increase in output voltage level. Flying capacitor inverter uses capacitors in place of diodes but the number of capacitors also limits it for higher level application.

Synthesizing a nearly sinusoidal output voltage is accomplished using various switching methods. Numerous modulation techniques such as sinusoidal pulse width modulation (SPWM) [10-12], selective harmonic elimination [13-14], hybrid modulation methods [15-16] nearest level technique [17] have been proposed and analyzed depending of inverter configurations. Among the numerous pulse width modulation (PWM) techniques sinusoidal pulse width modulation and space vector pulse width modulation are most widely used modulation techniques. Space vector PWM [11, 18] enables the efficient use of DC voltages that smartly works with vector control hence contributes less THD, better power factor and less switching losses at higher frequencies.

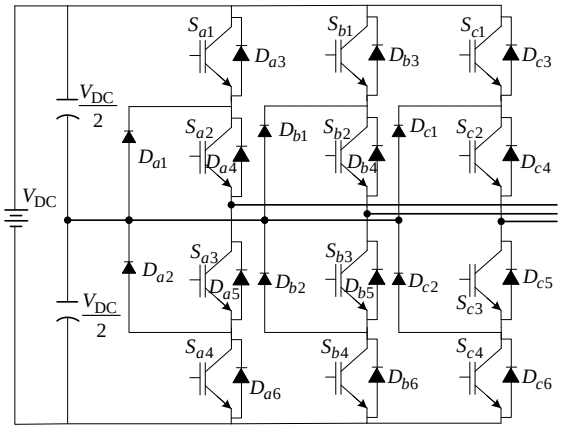
In this paper, analysis of three phase T-type inverter [19] configuration is done using a modified SVPWM as control strategy for providing switching pulses.

II. THREE- LEVEL T-TYPE INVERTER

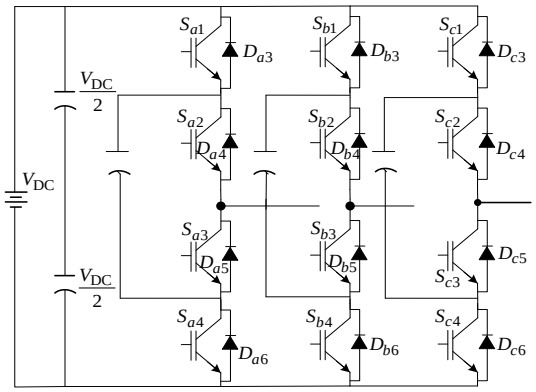
Three-phase three-level inverter configuration for Cascaded H-bridge (CHB), Neutral Point Clamped (NPC) and Flying Capacitor is shown in Fig.1. Present work is focused on a three-phase T-type inverter having comparatively reduced number of switches as depicted in Fig.2. Each phase of the three-phase T-type inverter constitutes two IGBT switches and one bi-directional switch. The IGBT switches (S_{x1} and S_{x2}) $_{x=\ (a,\ b,\ c)}$, and the bi-directional switch (S_{x3}) blocks only half of the DC-link voltage. Whereas, the neutral-point clamped (NPC) inverter uses two switches connected in series to block the full DC-link voltage. Thus the conduction losses of T-type inverter are considerably reduced compared to that of NPC inverter.



(a) Three-level *Cascaded H-Bridge*



(b) Three-level *Neutral point clamped*



(b) Three-level *Flying capacitor*

Fig.1 Basic three-level inverter topology.

Bidirectional switch in Fig.2 has only one IGBT switch and four diodes where two diodes connected in series for forward conduction and two of them used for blocking half of DC-link voltage.

TABLE . 1. SWITCHING TABLE FOR PHASE-A THREE-PHASE T-TYPE MLI

S_{a1}	S_{a3}	S_{a2}	Output voltage
ON	OFF	OFF	0.5 V_{DC}
OFF	ON	OFF	0
OFF	OFF	ON	- 0.5 V_{DC}

Three-phase T-type inverter generates three levels of output voltage of magnitude 0.5V_{DC}, 0 and -0.5V_{DC} with proper switching pulse. The switching table for Phase-A of T-type inverter is shown in table 1. A delay must be introduced between the switching of switches to avoid the short-circuiting of DC source.

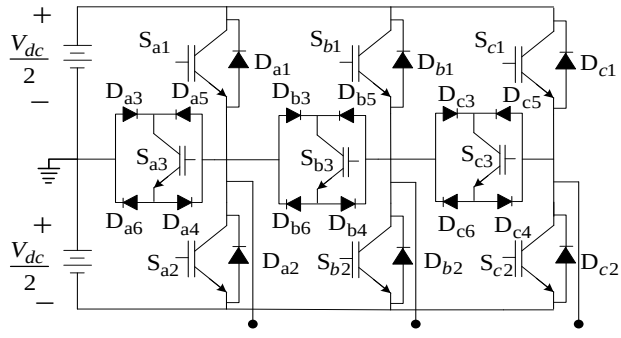


Fig.2. Three-level *T-type Inverter configuration.*

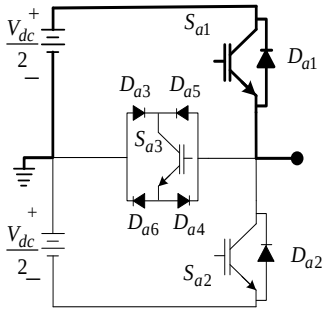
III. PRINCIPLE OF OPERATION

Each phase of three-level T-type inverter operates in three different modes and generates output voltage in three-levels.

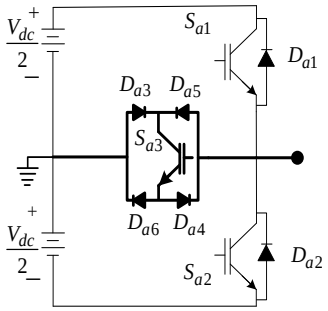
Mode-I: In this mode of three level T-type inverter, switch S_{a1} is turned ON and the phase current flows through the switch S_{a1} and the output voltage becomes 0.5 V_{DC}.

Mode-II: In this mode of three-level T-type inverter, switch S_{a3} is turned ON and the phase current flows through the switch S_{a3} and the output voltage becomes 0. In this mode always two diodes conducts irrespective of the direction of current.

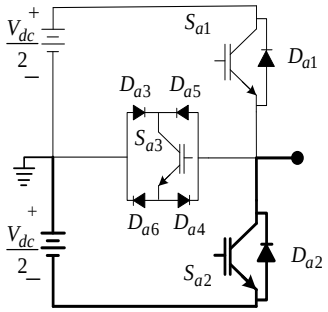
Mode-III: In this mode of three-level T-type inverter, switch S_{a2} is turned ON and the phase current flows through the switch S_{a2} and the output voltage becomes -0.5 V_{DC}.



(a) *Mode-I.*



(b) *Mode-II.*



(c) *Mode-III.*

Fig.3. *Modes of operations*

Keeping in mind the cost and efficiency of the overall given systems, our keen interest in the reliability is increasing. Thus most of the modern research works are conducted keeping in mind the reliability of efficient power conversions particularly in the area of fault diagnosis and fault tolerant control strategy.

IV. CONTROL STRATEGY

The Space Vector Pulse Width Modulation (SVPWM) schemes are developed to find the three nearest nodes on the voltage hexagon lattice with respect to the reference vector. The mathematical formulation of the early SVPWM were complex, because the voltage hexagon lattice was used in the Cartesian co-ordinate system. The co-ordinates of the nodes on the lattice are fractional numbers, which made the node selection difficult. The idea was that the reference vector was transformed from the Cartesian co-ordinate system to the 60 degree co-ordinate system. The 60 degree co-ordinate system represents one sector on the lattice and its benefit is that the co-ordinates for the nodes can be represented as integers. Therefore determination of the nodes could be accomplished by simple rounding functions and integer calculation.

In linear modulation region (0≤ Mi≤ .907):

Here a modified SVPWM technique is introduced for the three-phase three-level inverter. For a particular reference vector, the sector of operation (P_i) and the angle (ϕ) is determined by using equations (1) and (2), respectively.

$$P_i = \text{int}\left(\frac{\varphi}{60}\right)+1 \quad (1)$$

$$\phi = \text{rem}\left(\frac{\varphi}{60}\right) \quad (2)$$

Where, φ is denoted as the angle of reference vector with respect to α-axis,int and rem indictes the function for integer and remainder respectively. The SVPWM diagram is divided into six sectors and each sector has four triangle depicted in Fig.4 with corresponding switching states.

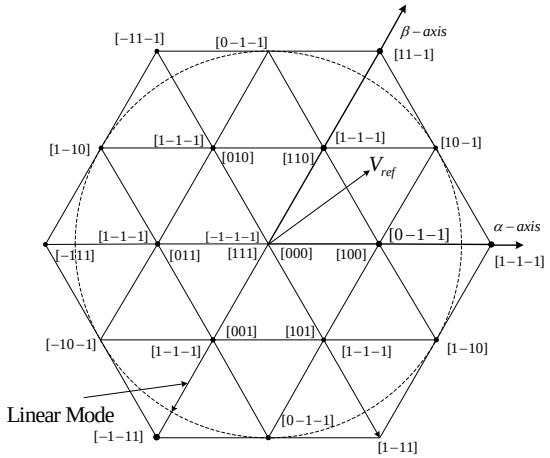


Fig. 4 *Space vector diagram of a three level inverter.*

The reference voltage vector with magnitude V_{ref} moves on a circular trajectory. The modulation index M_i can be controlled as the trajectory is laying inside the hexagon. The decomposition vector ($V_{r\alpha}$, $V_{r\beta}$) of the reference voltage into α-β axis having 60^0 angle to each other, for an N-level inverter can be determined as

$$V_{r\beta} = \frac{2(N-1)V_{ref}}{\sqrt{3}V_{dc}}\sin\phi \quad (3)$$

$$V_{r\alpha} = \frac{2(N-1)V_{ref}}{\sqrt{3}V_{dc}}\sin\left(\frac{\pi}{3}-\phi\right) \quad (4)$$

The modulation index (M_i) depends on the magnitude of reference voltage V_{ref}. The ideal relationship between modulation index M_i and V_{ref} is defined as:

$$M_i = \left(\frac{0.907V_{ref}}{0.866V_{DC}}\right) \quad (5)$$

The location of reference vector in any particular triangle (Δ_i) can be determined with the decomposition vector ($V_{r\alpha}$, $V_{r\beta}$) of reference vector. According to "NEAREST THREE VECTOR"(NTV) method, every vertex of a triangle is considered as a switching vector and every switching vector is represented by many switching states for selected location in a particular triangle. For a three-level inverter there are 27 switching states (n^3 states for an n-level inverter). The space vector pulse width modulation is determined by selecting and analyzing every switching state for the given triangle of their respective on-times. Every switching state is responsible for the significant performance of the inverter.

The on-time is defined as $T_s=T_a+T_b+T_c$. The volt-sec equation time averaging is followed:

$$V_{ref}T_s=V_aT_a+V_bT_b+V_cT_c \quad (6)$$

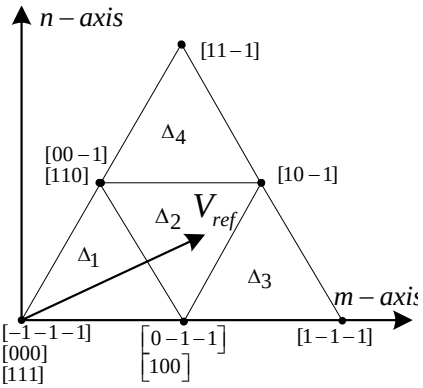


Fig.5. *Triangles in sector one.*

Where, V_{ref} is the reference voltage and T_s is the PWM time. Here, two active vectors (V_a, V_b) and zero vector is used as V_c.

For a three-level inverter time T_a, T_b, T_c are defined as:

$$T_a = T_s\left[1-2M_i\sin\phi\right]$$
$$T_b = T_s\left[2M_i\sin\left(\frac{\pi}{3}+\phi\right)-1\right] \quad (7)$$
$$T_c = T_s\left[1-2M_i\sin\left(\frac{\pi}{3}+\phi\right)\right]$$

V. SWITCHING PATTERN GENERATIONS

A variable switching-pattern has been developed for better harmonics. The seven-segment switching patterns can be applied for triangle (or space vectors) having less number of switching redundancy and nine-segment for higher number of switching redundancy. Depending on the redundancies of the switching states at the vertices of the triangles seven segment and nine segment time division is distributed for the three-level inverter as shown in Fig. 6-7.

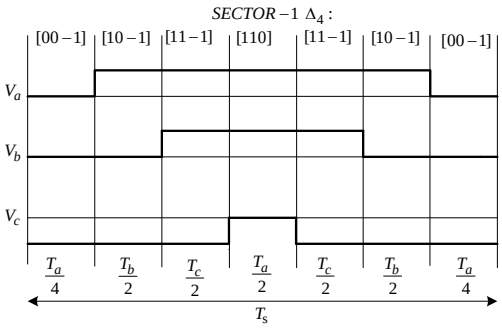


Fig. 6 seven segment switching-diagram.

Nine-segment switching pattern implementation is preferred to the seven-segment switching sequence, where redundancies of switching states are increased for triangle say Δ_1 and Δ_2. The switching pattern for the seven-segment and the nine-segment is shown in table II.

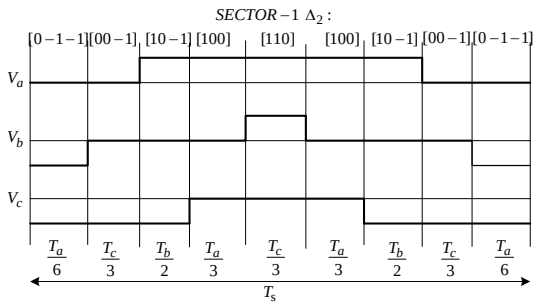


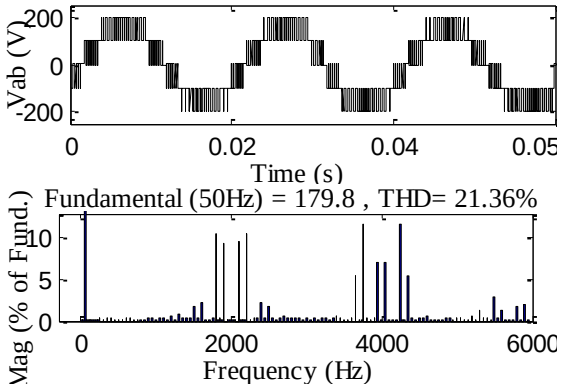
Fig.7. *Nine-segment switching-diagram.*

TABLE II. SWITCHING SEQUENCE PATTERN OF FOUR TRIANGLES IN SECTOR ONE

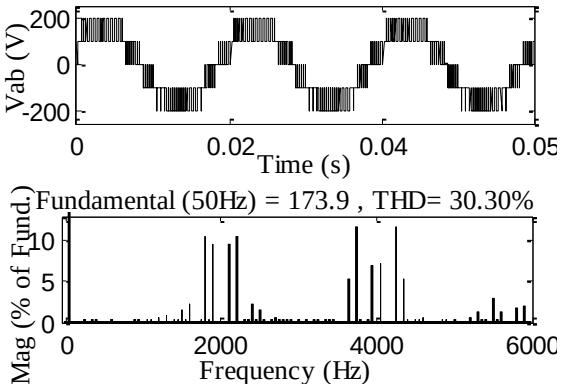
Seven Segmentation	Nine Segmentation
$\Delta_3 : [0-1-1] \rightarrow [1-1-1] \rightarrow [10-1] \rightarrow [100] \rightarrow [10-1] \rightarrow [1-1-1] \rightarrow [0-1-1]$	$\Delta_1 : [-1-1-1] \rightarrow [0-1-1] \rightarrow [00-1] \rightarrow [000] \rightarrow [100] \rightarrow [000] \rightarrow [00-1] \rightarrow [0-1-1] \rightarrow [-1-1-1]$
$\Delta_4 : [00-1] \rightarrow [10-1] \rightarrow [11-1] \rightarrow [110] \rightarrow [11-1] \rightarrow [10-1] \rightarrow [00-1]$	$\Delta_2 : [0-1-1] \rightarrow [00-1] \rightarrow [10-1] \rightarrow [100] \rightarrow [110] \rightarrow [100] \rightarrow [10-1] \rightarrow [00-1] \rightarrow [0-1-1]$

VI. SIMULATION RESULTS

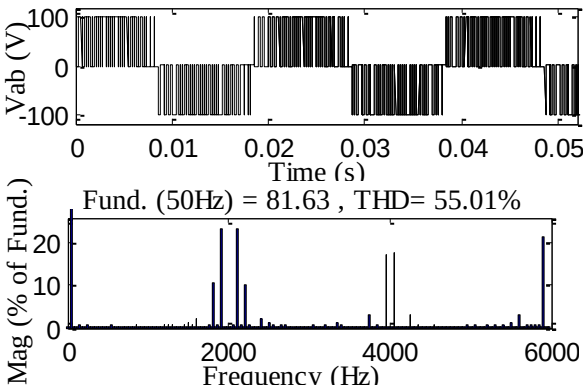
Modified three-level space vector pulse width modulation technique is applied on T-type inverter and NPC and corresponding output voltage with total harmonic distortion is depicted in Fig. 5. It is observed that T-type inverter have relatively reduced THD than NPC. The benefit for T-type inverter is the requirement of number of switches which reduces the cost of the inverter and complexity of circuit. Table.3. represents the comparison of T-type with classical configuration for component count.



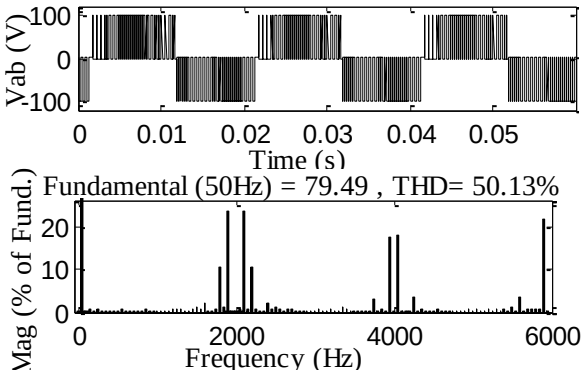
(a) Output voltage waveform and THD of T-type inverter with modulation index (M_i) =0.907 for seven segment implementation.



(b) Output voltage waveform and THD of NPC inverter with modulation index (M_i) =0.907 for seven segment implementation.



(c) Output voltage waveform and THD of T-type inverter with modulation index (M_i)=0.454 for nine segment implementation.



(d) Output voltage waveform and THD of NPC inverter with modulation index (M_i)=0.454 for nine segment implementation.

Fig.8. Output voltage waveform and THD for different modulation index (M_i).

TABLE 3. COMPARISON OF THREE-PHASE MLIS WITH T-TYPE MLI.

Inverter Type/ Number of Component	CHB MLI (Symm.)	NPC MLI	FC MLI	T-Type MLI
IGBTS /MOSFETS	12	12	12	6
Bidirectional controlled switches	0	0	0	3
Diodes	12	18	12	18
Separate Supply/DC link Capacitor	3	2	2	2
Flying Capacitor	0	0	3	0

VII. CONCLUSION

The selection of T-type inverter is made based on the benefits of reduced component count in the multilevel than the classical multilevel inverters. A modified space vector pulse width modulation is modelled that proposed variable switching patterns by using seven-segment for space vectors having less number of switching redundancy and nine-segment for higher number of switching redundancy to reduce harmonics. The whole circuit is simulated using MATLAB/SIMULINK platform. The simulation results of line voltages of two different multilevel inverters are presented. It is observed that, for a T-type inverter, there is a significantly improved harmonic profile than the neutral point clamped inverter for the same voltage level.

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