Comparative Study of Gate Underlap and Overlap in Junction-less DG-MOSFET with High k-Spacer through Simulation

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***Abstract*—In this paper a comparative study is shown between gate underlap and gate overlap of Junction less Double Gate MOSFET with high k-spacer (HfO_2). The impact of gate underlap and overlap on the DC and RF performance of JL-DG MOSFET is analyzed with the help of a numerical TCAD device simulator. We engage Transconductance (g_m), Cut-Off Frequency (f_T), Total capacitance (C_{gg}), Miller capacitance as the key figure of merits for the analysis. The results conclude that the device with gate underlap has the efficacy for the usage in analog/mixed signal System On Chip (SOC) application, whereas the higher frequency operating devices are better operated with overlap. Underlap is undesirable due to current degradation in ungated region where as in case of gate overlap we got a very good I_{ON} current.**

Keywords*—Junctionless Transitors, Overlap, Underlap, TCAD, Haufnium dioxide (H_fO_2)

I. INTRODUCTION

Microelectronics industry has experienced tremendous progress in the last fifty years, especially with regard to the evolution of the products (i.e. integrated circuits) for better performances. So far, this considerable growth of the semi-conductor industry has been due to its technological capability to constantly miniaturize the elementary components of circuits, namely the MOSFET (metal-oxide-semiconductor field effect transistor), the basic building block of VLSI (very large scale integration) integrated circuits. However, the continuous decrease of the silicon surface in order to satisfy the famous “Moore's Law” has resulted in serious physical and technological limitations, mainly related to the gate oxide (SiO2) leakage currents, the large increase of parasitic short channel effects and the dramatic mobility reduction due to highly doped silicon substrates. Recently, we come across a device called Junction-less double-gate MOSFETs (JL-DGMOSFETs) that has been shown to be more optimal for ultra-low power circuit design due to the improved sub-threshold slope and the reduced leakage current compared to bulk CMOS. Transistors are becoming so tiny that it is becoming increasingly difficult to create high-quality junctions. In particular, it is very difficult to change the doping concentration of a material over distances shorter than about 10nm. Junction less transistors could therefore help chipmakers continue to make smaller devices.Here we are using JL-DG MOSFET with high k-spacer along with the concept of gate overlap and underlap. We use Hafnium dioxide as high k-spacer. The Analog/RF performance of this device has been analyzed here for comparison between underlap and overlap gate. This paper is organized as stated: section II highlights the various device structures, Section III provide the variation of DC, analog and RF performance parameter as a function of overlap and underlap gate with SiO_2 as the gate dielectric, in section IV we draw the conclusions. An acknowledgment to our guide and the references used to illustrate this paper are also mentioned.

II . DEVICE STRUCTURE

The figures reveal 2- dimensional cross section view of a JL-DG-MOSFET considered in our study. The devices comprises of a uniform doping concentration of 10^{20} cm^{-3} all throughout the structure. The nominal transistor dimension is given as channel length (L) = 15nm, thickness of substrate materials (t_{sub}) = 10mm and Effective Oxide Thickness (EOT) = 0.8 nm[6]. 2-dimensional device simulations are performed for JL-DG-FET with SILVACO ATLAS. Fermi Dirac carrier statics hand on hand with conventional Drift Diffusion model is included in this simulation. Concentration Dependent Mobility Model (COMMOB), and Field Dependent Mobility Model (FLDMOB), Shockley-Read-Hall (SRH) recombination, Auger recombination model and Newton & Gummel’s numerical iteration are used in the mobility reduction, recombination characteristics and to solve differential equation in ATLAS respectively. In this study we have rescinded Quantum Mechanical Effect (QME) due to the fact that QMEs and Ballistic transport are significant for devices with feature size less than 10 nm.[9]. The underlap and overlap gate structure are created by reducing 1nm from alignment or by extending 1nm from alignment respectively.

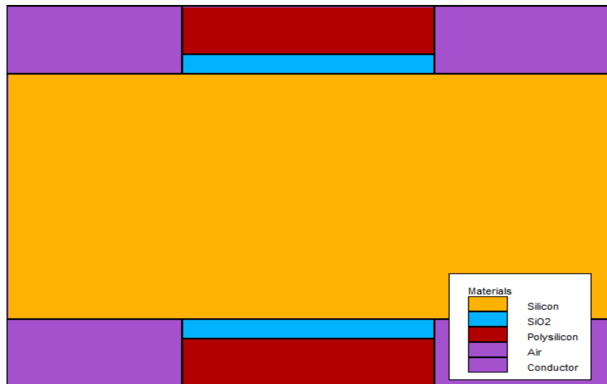

Fig. 1: 2-D cross sectional structure of Jl-DG-MOSFET with Si as substrate material, gate aligned,air as spacer.

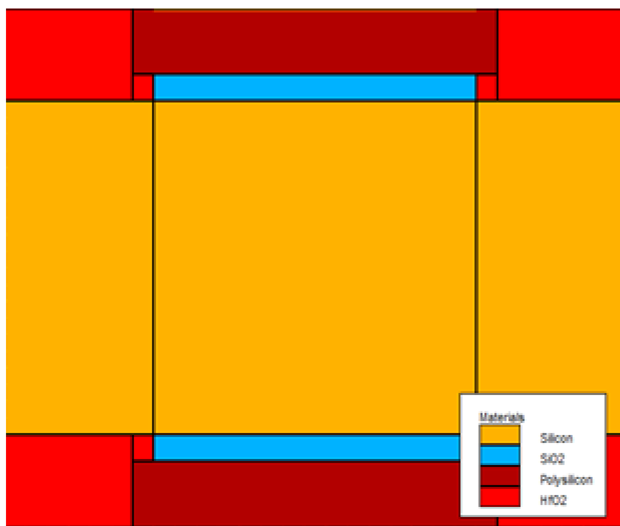

Fig. 2: 2-D cross sectional structure of Jl-DG-MOSFET with Si as substrate material, gate overlap,H_fO_2 as k-spacer

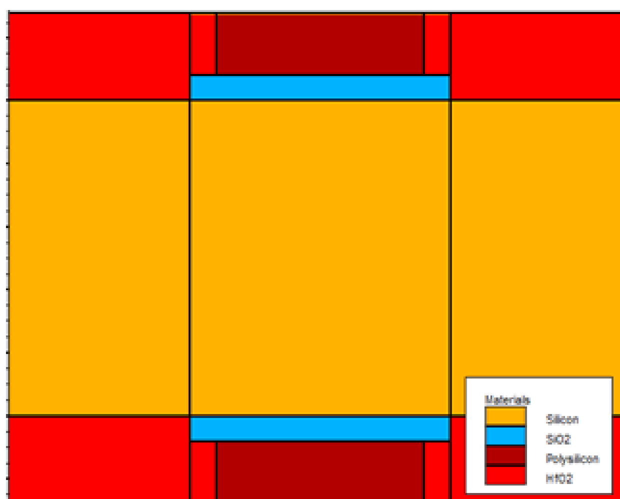

Fig. 3: 2-D cross sectional structure of Jl-DG-MOSFET with Si as substrate material, gate underlap, HfO2 as k-spacer. The various comparison analysis are done in section III.

II. RESULTS & DISCUSSIONS

3.1. DC PERFORMANCE INVESTIGATION

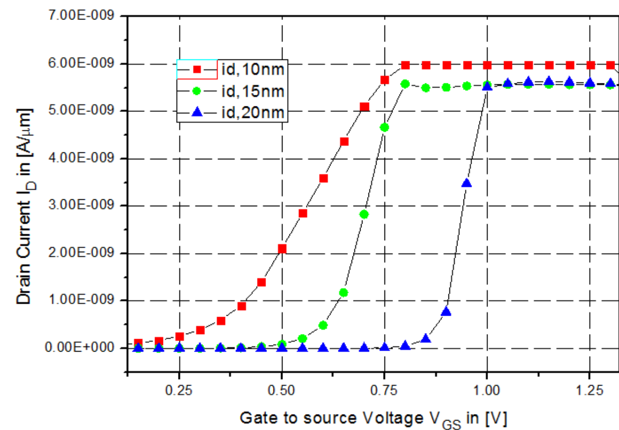

Fig.4: Variation of Drain Current I_D as a function of Gate-to-source voltage V_{GS} for different channel length L=10nm, 15nm and 20nm with device parameter values V_{DS}=0.2v, t_{Si}=10nm and t_{OX}=0.8nm for gate underlap.

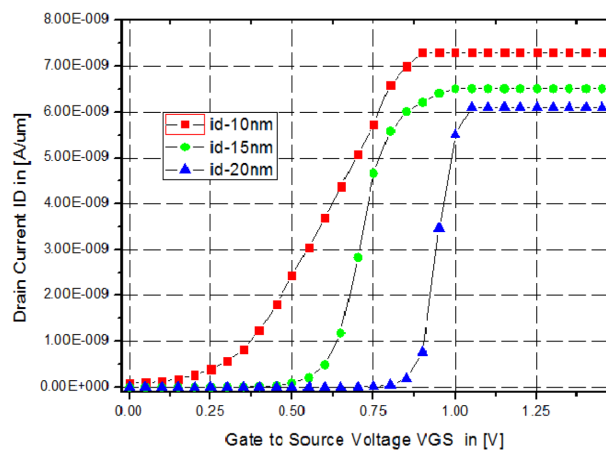

Fig.5: Variation of Drain Current I_D as a function of Gate-to-source voltage V_{GS} for different channel length L=10nm, 15nm and 20nm with device parameter values V_{DS}=0.2v, t_{Si}=10nm and t_{OX}=0.8nm for gate overlap.

By analysing the above graphs, we come to a conclusion that the gate overlap devices have good I_{ON} current as compared to gate underlap devices. Underlap is undesirable due to current degradation in ungated region .We also conclude that at 10nm channel, overlap device works better. Even after channel length downscaling, the device works better due to use of high k-spacer.[5]

3.2. ANALOG PERFORMANCE INVESTIGATION

In this section, the analog performance parameters of a JL-DG-MOSFET with high k-spacer are evaluated. We use the

Transconductance (g_m) as the key figure of merit for comparing underlap and overlap gate .

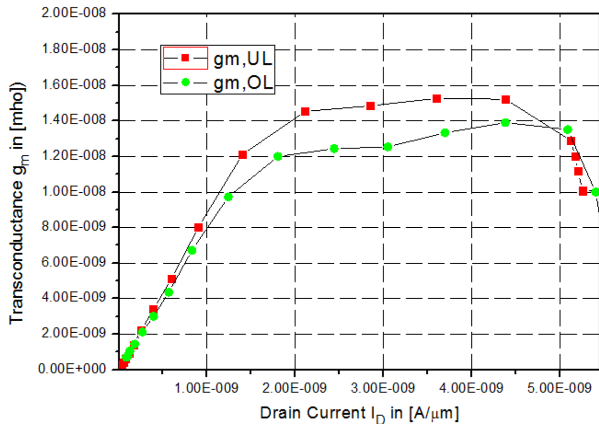

Fig. 6: Plot of variation of transconductance (g_m) as a function of Drain current for Channel Length L=10nm with device parameter values V_{DS}=0.2v, t_{Si}=10nm and t_{OX}=0.8nm.

The above figure shows gate underlap has a high transconductance as comparison to gate overlap. The basic challenge in analog/RF design lies in achieving a good balance between bandwidth and power efficiency of a circuit. Underlap S/D design suppresses short channel effects (SCEs) leading to improved gate controllability thus leading to higher *gm* as compared to overlap. The peak *gm* is reduced later on in the graph due to the additional series resistance of the wider spacer region.

3.2. RF PERFORMANCE INVESTIGATION

In this section we investigate the RF performance using 3 standard figure of merits such as: - (a) Cut-Off frequency (f_T)
(b)Total capacitance(Cgg) (c) Miller capacitance.

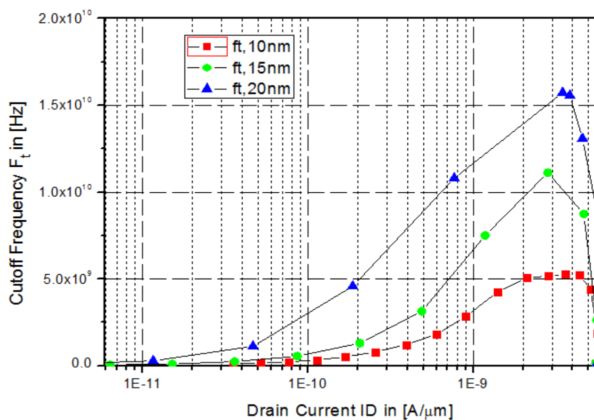

Fig 7:Variation of Cut-off Frequency (f_t) as a function of drain current I_D for different Channel Length L=10nm,15nm and 20nm with device parameter values V_{DS}=0.2v,t_{Si}=10nm and t_{OX}=0.8nm for underlap gate.

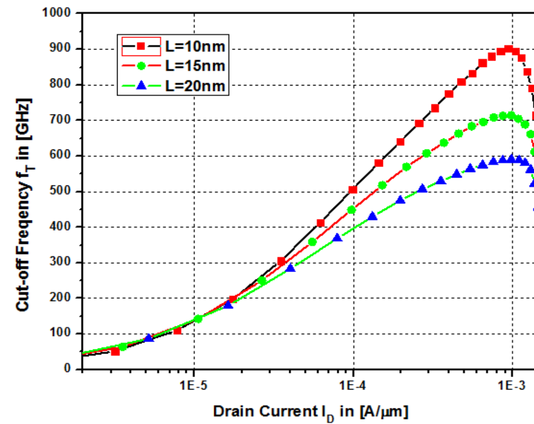

Fig 8:Variation of Cut-off Frequency (f_t) as a function of drain current I_D for different Channel Length L=10nm,15nm and 20nm with device parameter values V_{DS}=0.2v,t_{Si}=10nm and t_{OX}=0.8nm for overlap gate.

Fig. 8 shows the variation of cut-off frequency f_T as a function of I_D. f_T is demonstrating a 1/L^2 dependency as gm proportional to1/L at the sub threshold region f_T attains a lower value and increases with I_D until it reaches a maximum value at a specific gate bias. At the maximum point of f_T ,gate to source/drain capacitance is minimum. As L increases f_T decreases .Where as it is inverse in case of underlap in Fig 7.So overlap has a high cutoff frequency while downscaling.

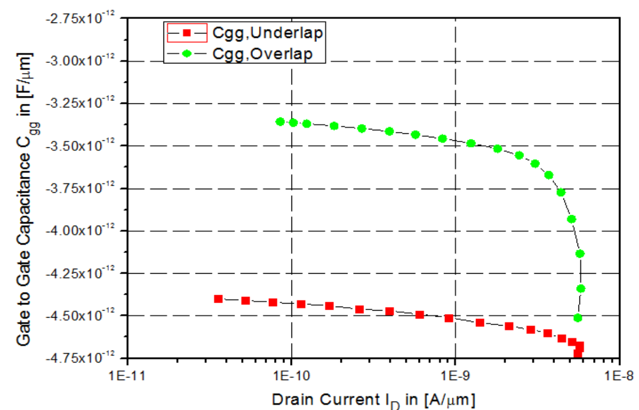

Fig 9:Variation of Cgg as a function of drain current I_D for Channel Length L=10nm with device parameter values V_{DS}=0.2v, t_{Si}=10nm and t_{OX}=0.8nm.

The above graph shows that the total capacitance is reduced in case of underlap to a great extent. The reduction in the internal fringing capacitance due to the underlap profile results in lowering of the gate capacitance, *C*gg, by nearly 40% at lower current levels whereas at higher current levels C_{gg} is reduced by only 10%.

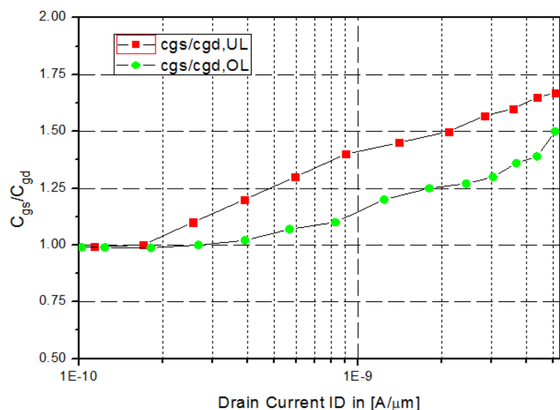

Fig 10:Variation of Cgs/Cgd as a function of drain current I_D for Channel Length L=10nm with device parameter values V_{DS}=0.2v, t_{Si}=10nm and t_{OX}=0.8nm.

The above graph shows Underlap channel design also results in an improvement in gate–to–source (*C*gs) to gate–to–drain (*C*gd) capacitance ratio (*C*gs/*C*gd). A decrease in *C*gs/*C*gd ratio implies a loss of channel charge and the increase in parasitic feedback capacitance. It is well established that *C*gs/*C*gd is an important limiting factor for the RF performance of short channel MOSFETs . As shown in Fig.10 the use of underlap channel architecture improves *C*gs/*C*gd ratio by 30% at high *I*ds due to an enhanced gate controllability.

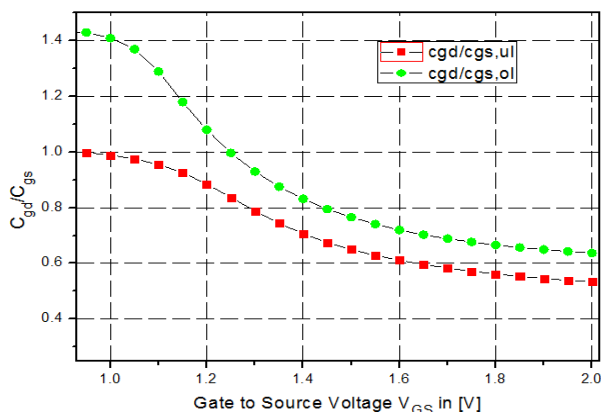

Fig. 11: Variation of Cgd/Cgs as a function of V_{GS} for Channel Length L=10nm and Comparison between underlap and overlap.

The above graph shows that the parasitic capacitance value or the miller capacitance ratio is reduced in case of underlap.

III. CONCLUSIONS

In this work, ability of Junctionless DG MOSFET with gate underlap and overlap concept ,to suppress SCEs, and to increase performance are investigated. Among various,JL-DG MOSFETs with K-spacer ,underlap DG provides reduced parasitic capacitance to a great extent along with good transconductance ,on the other hand Overlap gate shows higher cutoff frequency and good I_{ON} current. In near future Linearity study of Underlap and Overlap and their comparison can be done for further analysis. Better RF performance is obtained in overlap DG MOSFET. For low power dissipation and reduced heating effect underlap DG-MOSFET are the best, as we see reduced paracitic capacitance there. Overlap DG MOSFET can be used in Devices that require good Ion current.

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