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Comparative Study of Fault Modeling for SG-mode and LP-mode INV

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***Abstract*— FinFETs are expected to take the place of planner CMOS field-effect transistors (FETs) in the near future, due to their superior electrical characteristics. Double-gate FinFETs has better SCEs performance compared to the conventional CMOS and stimulates technology scaling. In this paper we are design 25nm DG-FinFETs and extracting their characteristics by using Sentaurus TCAD. DG-FinFET has independent gate; threshold voltage of one gate can be change by varying the voltage of other gate. By using this phenomenon INV circuit can be configured in one of the modes such as SG mode and LP mode. From a circuit testing viewpoint, it is unclear if CMOS fault models are absolute enough to model all defect in the FinFET circuits. In this work we address the above problem using mixed-mode Sentaurus TCAD device simulation. Results indicate that new fault model are needed to appropriately capture the behavior of INV based on independent-gates FinFETs with opens on the back gate and shorted-gate FinFETs which have been accidentally described into independent gate structures.**

Keywords—Gate FinFET, TCAD, Fault models, Independent gate (IG) mode, Low power (LP) mode, Leakage, Delay, Shorted gate (SG) mode.

1. INTRODUCTION

The device scaling continues for the 21st century, it turns out that the historical growth, doubled circuit density and increased performance by about 40% every technology generation, followed by "Moore's Law," [1]. With continued technology scaling, the twin problems of dissipated leakage power and circuit reliability have been increases. Double-gate FETs in which a second gate is added opposite the first gate, are supposed to replace planar MOSFETs because double-gate FETs have excellent short-channel characteristics [2].The structures of double-gate FETs may be classified into one of three basic categories [3]. Planar DGFETs are not easy to fabricate [3, 6]. A various DGFET that can be easily fabricated is the FinFET. Amongst double-gate devices, FinFETs have emerged as the most suitable candidate because their ease of fabrication [3].

FinFET (with the silicon resembling the dorsal fin of a fish), in which the body of silicon has been rotated on its edge into a vertical direction so only the source and drain regions are placed horizontally about the silicon body, as in a conventional planar FET.When the top oxide is made much thicker than the side oxides in order to effectively on hold the top gate. The electrical width of a triple-gate FinFET is given by following: $W=2H_{fin}+W_{fin}$ (some papers refer to W_{fin} as t_{Si}). In many cases, *Wfin* is small in order to have a small SCE. As a result, *W* is approximately $2H_{fin}$. As a result, the physics of a FinFET becomes similar to that of a DGFET.

There are two primary types of DG FinFETs, simultaneously, driven DG (SDDG) and independently driven (IDDG) [4] FinFETs. When both the gates (front and back) are connected to each other then it is called SDDG, also behave like three-terminal MOSFET, since the IDDG has two independent gates. SDDG structure also has a third gate on the top of the gate called the tri-gate FinFETs, since the top gate of IDDG FinFET is disconnected by thick nitride layer. IDDG FinFETs have been introduced for changing threshold-voltage control [5] and leakage-current control but the delay is increased. The variety of physical defects is present in the FinFET circuits.

Fault modeling is the process of developing physical defects models of CMOS at higher levels of abstraction. Bridging [8]-[9], stuck-at [10], delay [11], and stuck-open [12] faults are the most widely used fault models for CMOS, However on account of the double-gate configuration. When two leads in a logic network are connected accidentally and wired logic is performed at the connection then Bridging fault occurs in the circuit. If CMOS fault models can absolutely model defects in FinFET circuits. Here, the important questions that need to be considered are 1) how do FinFET logic gates behave in the presence of defects like opens and shorts; and 2) are CMOS fault models capable for covering all defects in FinFET logic gates.

In the history, a limited number of FinFETs fault models are available to date. Vazquez et al. [13] explained that the hold time for stuck-open faults in CMOS is much higher than the clock period. In the SG-mode FinFET stuck-open faults, increased sub-threshold leakage and gate tunneling
currents decrease the hold time. It is very difficult to test FinFET faults in many cases when the clock period is close to the hold time. It must be noted that a stuck-open fault is only one type of defect that can occur in the SG-mode FinFET gate. Also, defects in the I_G FinFET structure were not considered.

The main significant addition of this work can be summarized as follows:

- We model opens and shorts in FinFET inverter (INV) with SG- and IG-mode devices using mixed-mode device simulation in Synopsys Sentaurus TCAD [14].

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• In the case of a floating back-gate node due to an open defect, we show that a new fault model is needed to account for the observed leakage-delay trends of the logic gates.

• We also show that when an open defect isolates the front and back gates then pure SG-mode logic gates continue to maintain functionality, but may suffer in delay, while logic gates with I_G FinFETs fail to operate correctly for a range of voltages that can be shown at the floating back-gate node.

The rest of the paper is classified as follows. Fault modeling related work is reviewed in Section II. In Section 3, FinFET device characteristics are considered (Section 3.1) followed by the design of FinFET logic INV (Section 3.2). We established the need for new FinFET fault models in Section IV. Section V presents the conclusions.

2. RELATED WORK

For CMOS circuits, it is surveyed that around 80% of physical defects can be detected using the stuck-at fault model [15].The testing for bridging and delay faults becomes critical due to scaling of the device. For different input combinations, a bridging fault causes a connection between supply and ground, and direct change in the supply current in the steady state. This behavior can be detected by guiding the supply current through I_{DDQ} test [16]. While bridging, stuck-at, stuck-open and delay faults are most of the defects in CMOS gates, it is unclear if they completely map defects in FinFET gates as well, which is the focus of the current analysis. In the resulting sections, we deal with different FinFET logic gates and show that defects as cuts on the back-gate are unique to FinFETs presenting a threatening challenge towards the development of a fault model.

3. LOGIC DESIGN

In this section, performance and power characteristics of FinFET INV using transistors in various modes are considered. Two modes of FinFET operation may be considered, shorted-gate(SG) mode in which two gates (front and back) are biased together to turn on the device, in this case we get improved drive strength and have better control over the channel. Independent-gate (IG) [7] in which back gate biased can change the threshold voltage (*V*th) of front gate. This may reduce the number of transistors in the circuit.

3.1 Device Realization

The top view of a single-fin double-gate (DG) FinFET simulate using *Sentaurus Structure Editor [12] is shown in figure 1.The structure of DG FinFET is having two gates (front and back gate).*The device dimensions and doping levels of both p-type FinFET and n-type FinFET transistors are shown in table1.When we are using the thickness of the fin equal to half of the channel length (L_G) then it control the short channel effect in the device.

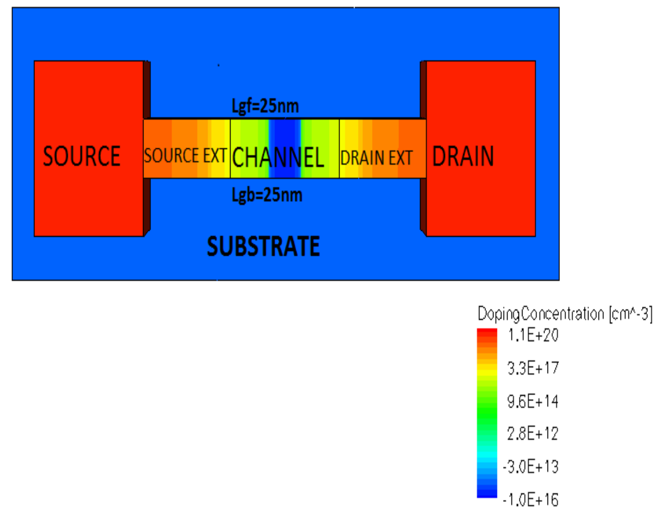

Fig.1 Simulated FinFET Structure

Table 1
FinFET Device parameters and Doping

L_{FG},L_{BG}	25nm
T_{SI}	10nm
T_{FXO},T_{BXO}	1nm
H_{FIN}	50nm
H_{FG},H_{BG}	20nm
L_{SFP} ,L_{SBP}	20nm
ϕnFinFET	4.4eV
ϕPFinFET	4.8eV
N_{SD}	10^{20} cm^{-3}
N_{BODY}	10^{15} cm^{-3}
V_{DD}	1V
LP-mode nominal V_{hi}	2.1V
SG-mode nominal V_{low}	-0.2V

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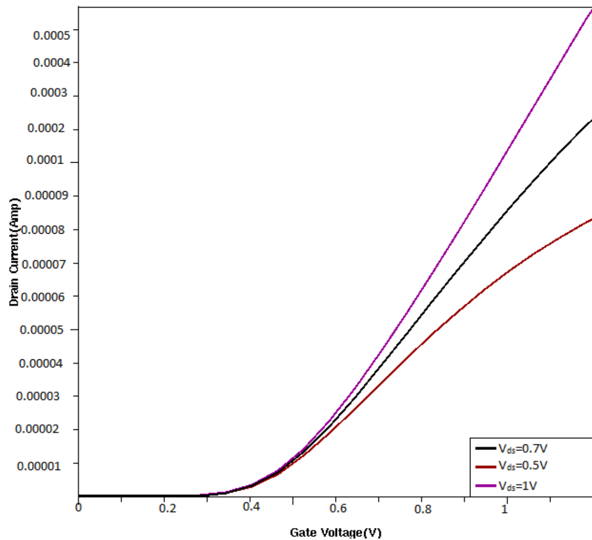

Figure 2 I_D-V_{GS} characteristics double-gate n-type FinFET Device of gate length L_G=25nm

Figure 2 shows the the current-voltage (I_D-V_G) characteristics of double-gate (DG) FinFET. The graph is plotted for V_{DS} = 0.5V to V_{DS} = 1V.

Figure 3 shows the I_D-V_{DS} characteristics of NMOS device with the gate length (L_G) of 25 nm, where V_{GS} is varied from 0.3V to 1V; same characteristics are also drawn for p-type FinFET.

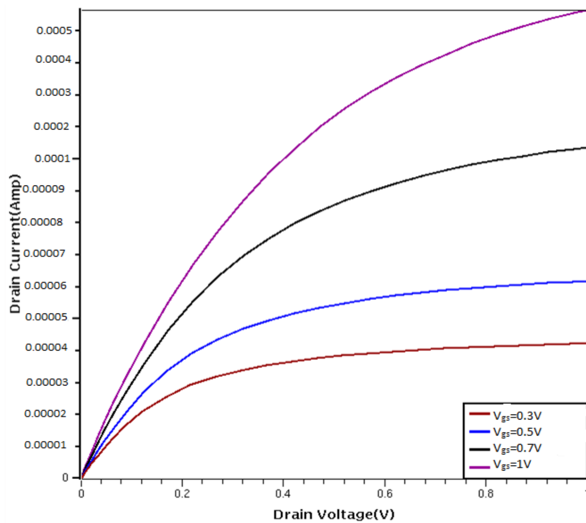

Figure 3 I_D-V_{DS} characteristics double-gate n-type FinFET Device of gate length L_G=25nm

3.2 *Design of FinFET INV*

Using SG and IG FinFETs, a CMOS Inverter can be constructed. In Fig. 4, the simplified of SG and low power (LP)-mode INV are respectively, shown. *SG-mode logic gates consist of pure*

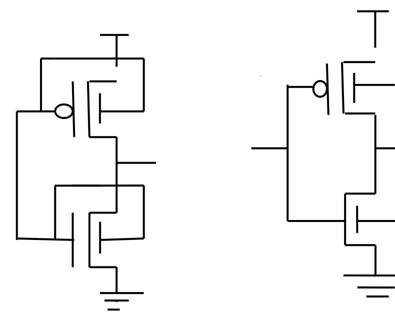

Fig.4. (a) SG-mode INV (b) LP-mode INV

TABLE 2
ON-STATE CURRENT FOR INDIVIDUAL FINFET DEVICES

Configuration	nFinFET I_{ON}(A)	PFinFET I_{ON}(A)
SG-mode LP-mode	$7.63*10^{-5}$ $5.05*10^{-5}$	$14.16*10^{-5}$ $6.01*10^{-5}$

SG FinFETs and have no flexibility in dealings off leakage versus delay. The LP-mode INV consist of pure IG FinFETs, where the back gate of the pFinFETs (nFinFETs) is connected to a positive (negative) voltage source denoted by *V*hi (V_{low}). *LP-mode INV provides an opportunity for tuning the leakage-delay characteristic of the gate by adjusting the back-gate bias dynamically.* The on-state currents for SG and IG n/pFinFETs are presented in Table 2.

From the testing, we observed the metrics of delay and leakage power consumption. The low-to-high transition delay t_{pLH} and high-to-low transition delay t_{pHL} were measured from the 50% transition of the input to 50% transition of the output. To obtain the gate delay t_{gate}, t_{gate} was set to max (t_{pLH} , t_{pHL}). For transient simulations, the rise and fall times of the input signal were set to 10 ps. Since leakage power consumption is input vector dependent, we observed the maximum leakage of each configuration. The maximum leakage was around six times higher than the minimum in the SG and LP-mode.

The trends of leakage and delay for an LP-mode- INV are shown in fig. 5(a) and 5(b) .The increment (decrement) in the back-gate bias for pFinFETs (nFinFETs) in the LP mode is denoted as ΔV. The back-gate bias voltages in simulations are calculated as follows (note that V_{DD} = 1 V):
$V_{hi} = 1+\Delta V$ and $V_{low} = 0- \Delta V$
From Fig. 5(a) and (b), reverse biasing the back gate (above the rail for pFinFET and below the rail for nFinFET) increases the effective transistor threshold voltages linearly, whereby leakage decreases exponentially and delay increases roughly linearly. We also simulated fault-free SG-mode INV, to compare their leakage and delay values with respect to their fault-free LP-mode INV. The results are presented in Table III. The nominal voltage V_{hi} and V_{low} of LP-mode INV are shown in Table I. From Table 3, SG-mode implementations result is around three times faster gates at the magnitude higher leakage.

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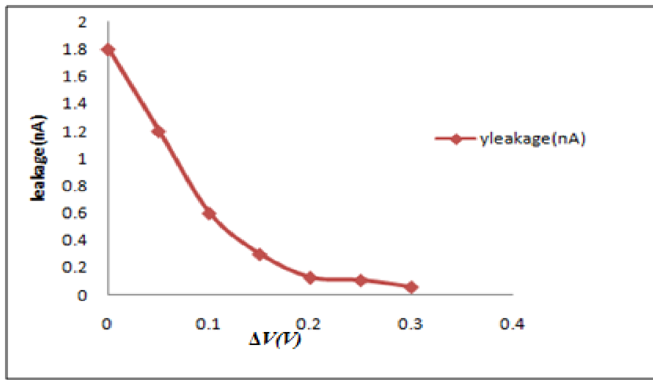

Fig. 5(a) LP-mode INV leakage vs. ΔV

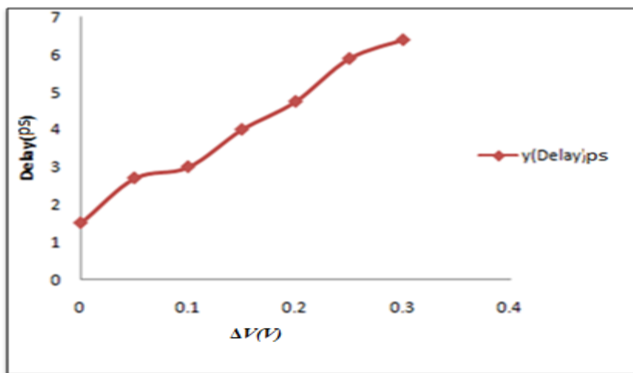

Fig. 5(b) LP-mode INV delay vs. ΔV

TABLE 3
METRICS OF SG/LP-MODE FINFET INV

INV	Leakage(nA)	Delay(ps)
SG-mode	6.66	3.9
LP-mode	0.003	4.8

1. *Fault modeling in the FinFET INV*

In this section, we study the behavior of FinFET INV in mode INV and shorted each transistor's source and drain terminals. We applied test vectors that detect all faults in CMOS-based INV to the SG- and LP-mode FinFET INV.

TABLE 5
SHORTING SOURCE AND DRAIN OF AN N/P-FINFET IN SG/LP-MODE INV

INV	Maximum leakage(A)
SG-mode INV	$7.04*10^{-5}$
LP-mode INV	$1.25*10^{-5}$

When the value of a wire is fixed at 0 (1) and cannot be changed then it shows stuck-at 0 (1) fault in the circuit. When we short the source and drain terminals of a transistor then transistor is always ON then it shows stuck-on fault in the circuit. A stuck-open fault is always the case opposite to the stuck-on fault, that is, a transistor is always OFF regardless of the applied gate voltage.

When test vector assigns a value opposite to the assumed stuck-at fault then stuck-at faults will be detected and ensures that the faulty value is observed at the output. The stuck-at faults are assumed to be at the gate inputs and output.

A stuck-on fault present in the circuit causes a VDD-to-ground connection for a particular set of input combinations. In this case, the static leakage current increases. In the presence of the stuck-on faults, the leakage currents observed during test of SG-and LP- mode INV are shown in Table 5. The four to six orders of magnitude increase in current, in comparison to the nominal leakage shown in Table 3, enables detection of these defects using I_{DDQ} testing.

4.1 *Effect of an open on the pFinFET back gate in LP-mode INV*

In this case we simulated LP-mode INV with open faults on the back gates of the pFinFETs. For the defect-free cases back-gate biases, V_{hi} and V_{low} were set to their nominal values shown in Table I. When the back gate wire is open then the node is called floating node, the voltage value for a cut on the back-gate wire, V_{cut}, was varied from V_{low} to V_{hi}.

The variation in leakage and delay with respect to Vcut is shown in Fig. 6(a) and (b).

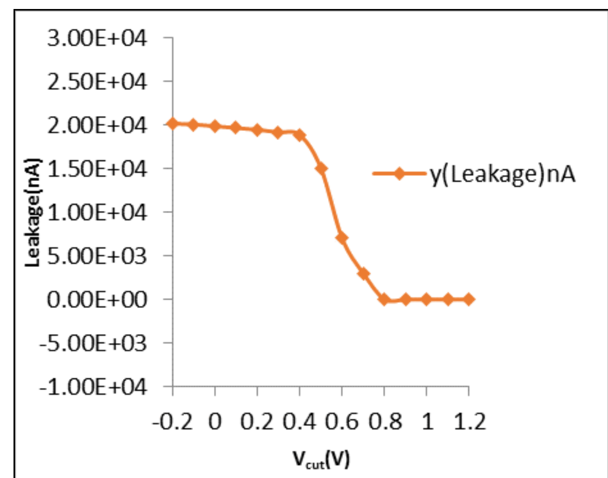

Fig.6 (a) Leakages characteristics with different pFinFET back-gate bias voltages for LP-mode INV

Also, as Vcut decreases from the value of V_{hi}, the logic gates switch faster due to the fact that the pFinFET has greater current drive capability, which reduces the gate delay. However, below 0.6, the high to- low transition delay t_{pHL} dominates the maximum delay as most of the current through the pull-down network consists of the pFinFETs leakage current, therefore limiting the current that discharges the output capacitance. Beyond a certain point, the pFinFET is always on, so that the output is high and the logic gates fail to function correctly.

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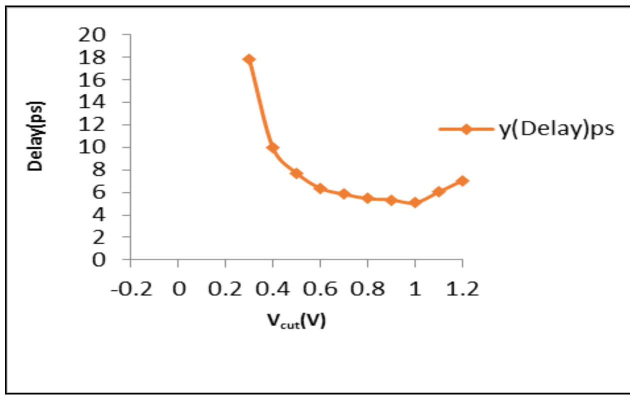

Fig.6 (b) Delay characteristics with different pFinFET back-gate bias voltages for LP-mode INV

Therefore, it is conclude that a cut on the back gate of a pFinFET in an LP-mode logic gate corresponds to many fault models, depending on the observed voltage on the cut. If Vcut is below 0.5V, the fault is pFinFET stuck-on and can be detected using I_{DDQ} testing. In the extreme case, the output is stuck-at 1. On the other hand, because of coupling effects, if Vcut values greater than 0.6V, then the logic gates switch faster, but have increased leakage power. This does not have a corresponding fault model in CMOS and is unique to FinFETs.

4.2 Effect of an open on the nFinFET back gate in LP-mode logic gates:

To apply the open faults on the back gates of nFinFETs in LP-mode INV, Vcut was varied from V_{low} to V_{hi}. We inserted a cut on the back gate wires of the top and bottom nFinFETs in the pull-down network and observed delay and leakage current from the circuit.The variation of leakage and delay values with changing Vcut is shown in Fig.7(a) and(b).When opens on nFinFETs then leakage is increase exponentially but delay is not affected until nFinFETs become severely forward-biased, which happens after 0.4 V. In this region, t_{pHL} decreases but it is not dominating factor and t_{pLH} limits the overall delay of the gate. When nFinFETs becomes severely forward- biased, it causes a drastic increase in delay of low-to-high transition. In the supreme case, the nFinFET is always ON and the output is stuck-at 0.

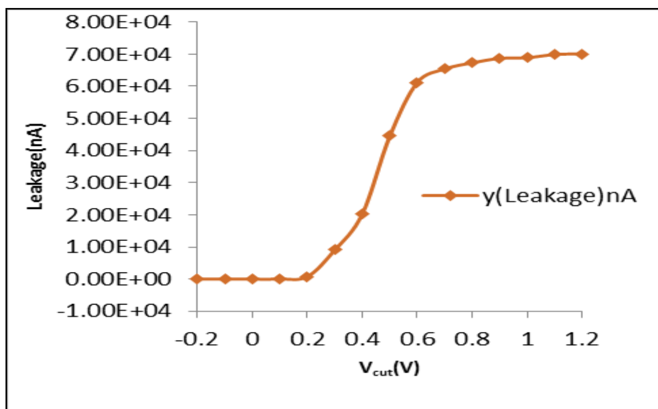

Fig. 7(a) Leakages characteristics with different nFinFET back-gate bias voltages for LP-mode INV

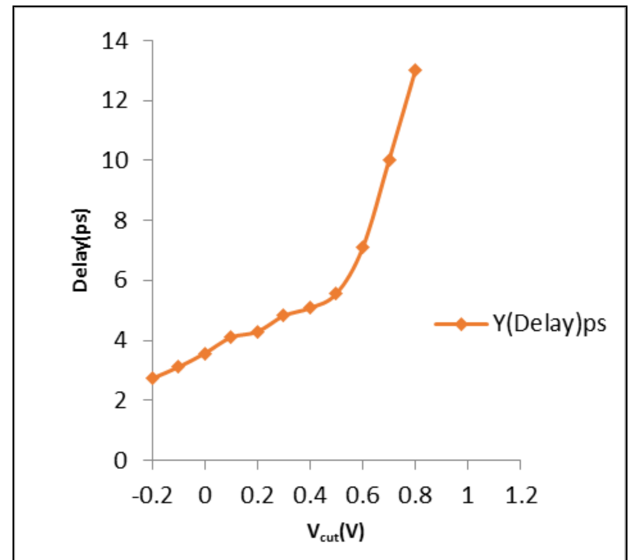

Fig.7 (b) Delay characteristics with different nFinFET back-gate bias voltages for LP-mode INV

4.3 Effect of an open on the p/nFinFET back gate in SG-mode logic gates

An IG FinFET in an LP-mode logic gate has two independent (front and back) gates. Therefore, a cut on the back-gate wire corresponds to a change in this voltage. However, a cut on the gate connection on an SG FinFET changes the FinFET into an IG FinFET with floating back gate. For a cut on a pFinFET, V_{cut} is swept between two extreme cases, namely, V_{low} and V_{hi}. Thevariation in leakage and delay are shown in fig. 8 (a) and (b).

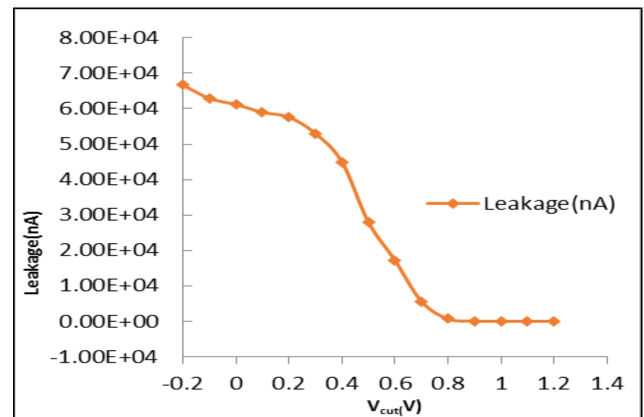

Fig.8 (a) Leakages characteristics with different pFinFET back-gate bias voltages for SG-mode INV

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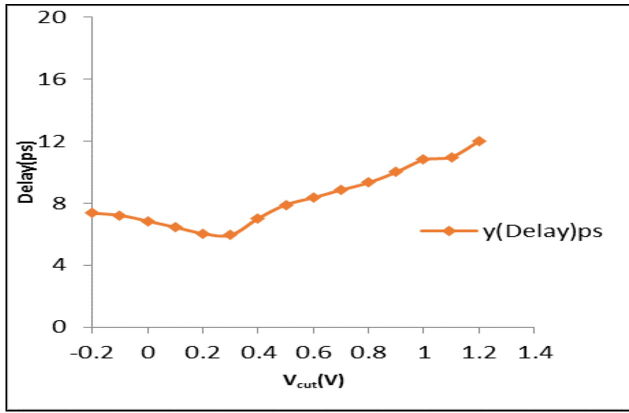

Fig.8 (b) Delay characteristics with different pFinFET back-gate bias voltages for SG-mode INV

On decreasing $V_{cut,}$ leakage increases. When the pFinFET is extremely forward biased, the leakage current approaches very high values, similar to those of LP-mode INV. However, the difference between the LP-and SG-mode INV lies in the delay characteristics. In comparison to the fault-free case (for all the swept back-gate biases in the INV) the delay increases typically the cut on the SG-mode INV. The logic gate remains functional for the back-gate voltages spanning V_{low} to V_{hi}.

This result can be explained by the greater drive strength of SG-mode FinFETs as compared to LP-mode FinFETs. By using similar setup simulations for the cuts on nFinFET back gate connections for the SG-mode logic gates were performed, the resulting leakage-delay characteristic is shown in fig. 9(a) and (b).

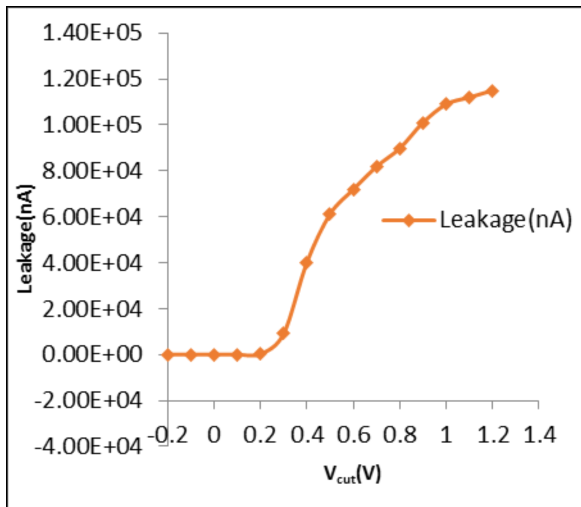

Fig. 9(a) Leakages characteristics with different nFinFET back-gate bias voltages for SG-mode INV

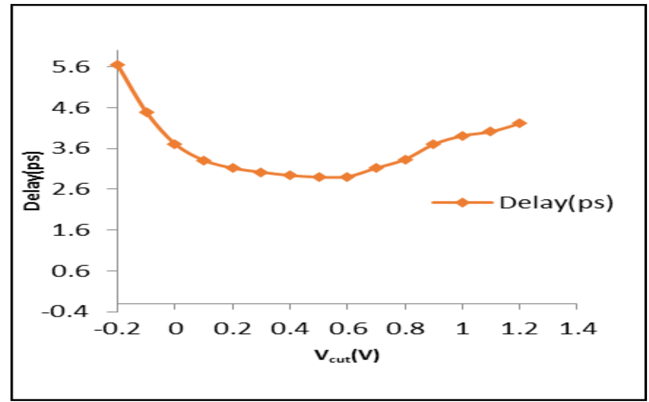

Fig.9 (b) Delay characteristics with different nFinFET back-gate bias voltages for SG-mode INV

The leakage current increases drastically and delay tends to decrease up to a certain point when nFinFETs are forward biased. To summarize, cuts on the back-gate connections of SG FinFETs cause an increases in leakage and delay in the worst case. The INV maintain functionality, when back-gate voltage varies V_{low} to V_{hi}. This behavior is different from that observed for the LP-mode INV.

CONCLUSION

Double-gate (DG) FinFET device of n-type and p-type has been simulated using Sentaurus TCAD and its various characteristics are plotted. Back gate is used to control the threshold voltage (*VT*) of the front gate, which is very important for the performance of the circuit. The simulation of different modes of INVERTER with 25nm FinFET shows that, we can get a minimum delay in SG mode, low power is obtained in LP configuration at the expense of increased delay while in IG mode we can give the inputs to the two different gates and the number of devices in a circuit can be reduced, reducing the area requirement of the circuit. An IG / LP mode is a mix of IG and LP modes and results in low leakage, reduced area and higher delay. In this work, simulation of the effects of “Opens” in LP-mode and SG-mode FinFET INV has done. It showed that most opens have a corresponding fault model in CMOS. However, opens on the back gates cause delay and leakage problems, which are unique to FinFETs. Depending on the voltage at the cut on the back gate, the defect could cause an increase in delay. On the other hand, it could also decrease delay while increasing leakage.

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