Comparative Study of 1-Bit Full Adder using Transmission Gate and CMOS Logic Style

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***Abstract*—Paper discusses comparative study of 1-bit full adder cells with two logic styles namely, Complementary MOS (CMOS) and Transmission Gate (TG). The simulations of 1 Bit full adder at 180nm, 45nm and 32nm technology is carried. Analysis of performance and efficiency of 1-bit full adder cell designs is carried out for different parameters like average power, supply voltage and transistor count is done. The average power for CMOS technology for 32nm is 1.474uW and for Transmission gate technology for 32nm is 1.193uW. It is observed that within a given logic style, as the technology decreases the average power decreases with decrease in the area for a constant supply voltage of 1 V. It is observed that less power is consumed by transmission gate based 1-Bit full adder than the conventional CMOS 1-Bit full adder for all technologies.**

***Keywords*— CMOS; TG; Full Adder; Logic Styles; SPICE simulator component;**

I. INTRODUCTION

These days close-packed, high performance, efficient, low power microprocessor is in demand. The central processing unit (CPU) is the integral part of each microprocessor. Key element of CPU is Arithmetic Logic Unit. ALU can perform basic arithmetic and logical operations. Addition is the most commonly used arithmetic operation in microelectronic systems and it is one of the speed-limiting elements. There are various full adder designs have been designed owing to its significance in many micro-electronic circuits. The full adder circuit is the core of many digital and analog circuits. Therefore, the development of the adder in terms of efficient parameters such as speed and power consumption should be pursued. It is necessary to optimize the performance of full adder cell for fast and low energy operations of arithmetic block. So, energy efficient, high speed, low power and reliable microprocessors are in demand in the recent and innovative silicon technology processes have resulted in the rapid growth of modern IC. Various performance determining

Factors are strongly influenced by chosen logic style. So, the objective of the paper is to find the most efficient logic style between CMOS and Transmission Gate for 1-bit Full Adder circuit.

In Section II, the overview of the full adder has been given along with its mathematical equations. In Section III the logic styles used in experimentation are discussed. Section IV shows the Full Adder circuit simulation results with different logic styles. Performance analysis is done in section V and obtained results are presented with the comparative results of cell designs in section VI. The paper concludes in Section VII.

II. OVERVIEW OF FULL ADDER

The circuit diagram of a 3-bit full adder is shown in the figure. The output of XOR gate is called SUM, while the output of the AND gate is the CARRY. The AND gate produces a high output only when both inputs are high. The XOR gate produces a high output if either input, but not both, is high. The truth table of 3-bit full adder is given. The 3-bit full adder circuit has a provision to add the carry generated from the lower bits.

Table 1: Truth table of 1-bit full adder

INPUT			**OUTPUT**	
A	***B***	***C***	***SUM***	***CARRY***
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The expression for SUM and CARRY is given by,
SUM=A $\oplus$ B $\oplus$ Cin
CARRY= A.B + Cin (A $\oplus$ B)

III. CIRCUIT DESCRIPTION

A. *Complementary MOS Logic Style (CMOS)*

D Complementary MOS Logic Style consists of Pull-Up Network (PUN), which has PMOS transistors and the Pull-Down Network (PDN), which consists of NMOS transistors. The Pull-Up Network connects the output of the gate with Vdd whenever the output of the gate is high. The Pull-Down Network connects gate output and GND when the gate output is low. This logic style consists of 28 transistors.

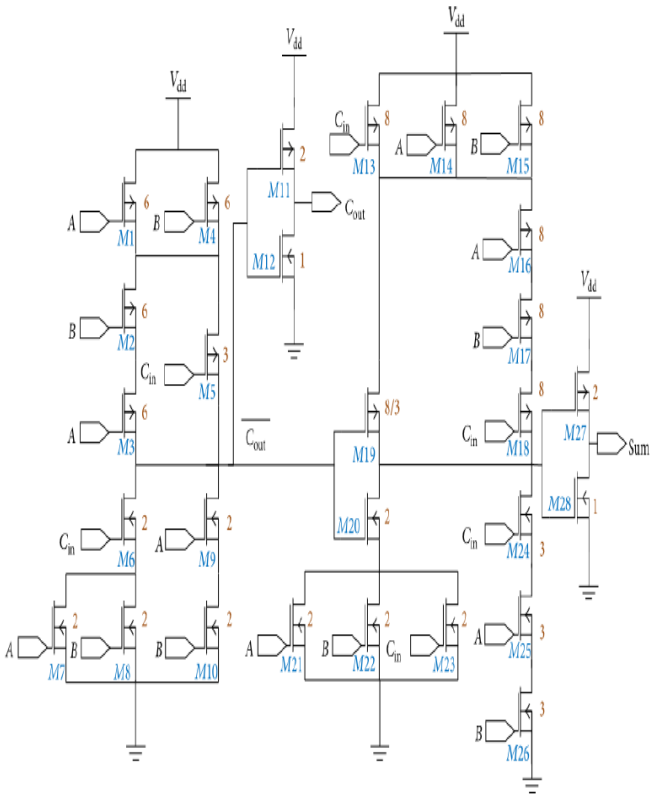

Figure 1: 1-Bit CMOS Full Adder [2]

B. *Transmission Gate*

It consists on n-channel and p-channel transistors with common connections for source and drain and separate gate connection. The circuit has a total of 20 transistors, comprising of transmission gates, PMOS and NMOS. The use of transmission gates enables the circuit to have high speed and low power dissipation.

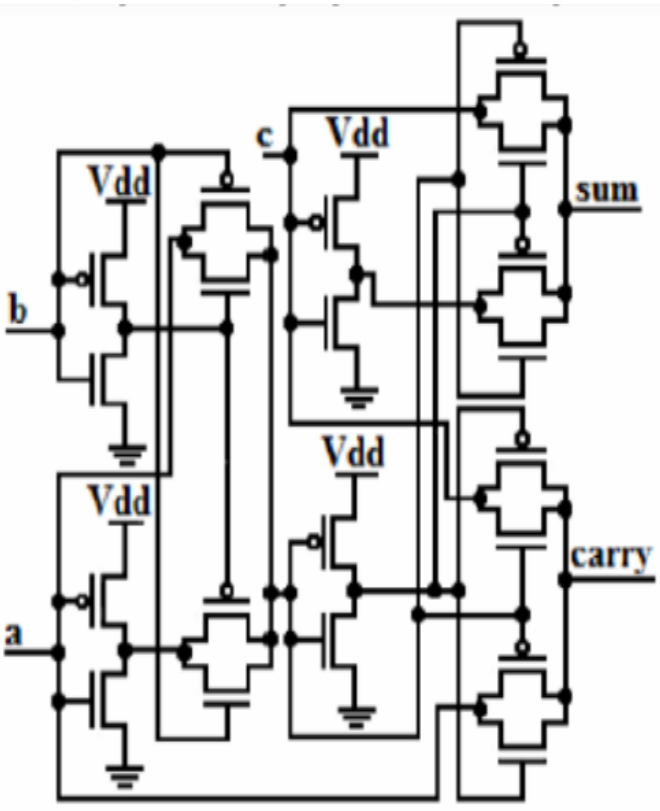

Figure 2: 1-Bit Transmission Gate Full Adder [1]

IV. SIMULATION RESULTS

The CMOS based 1-bit full adder and transmission based 1-bit full adder circuits are simulated on the SPICE simulator in the 180nm, 45nm and 32nm technologies. Signals having equal rise and fall time with 50% duty cycle are used for the simulation. Optimization of the length and width of the MOSFETs are carried out such that simulation results have minimum error. The power supply for MOSFET based circuits for all the technologies is 1V. The simulation analysis is carried out with three inputs (A, B, C) and two outputs (Sum and Carry) of full Adder.

Table 3 shows the transistor specification for CMOS and Transmission gate logic style for different technologies.

Table 3: Transistor specifications

Technologies	NMOS	PMOS
32nm	Length=32nm	Length=32nm
	Width=42nm	Width=216nm
45nm	Length=45nm	Length=45nm
	Width=129.375nm	Width=303.75nm
180nm	Length=180nm	Length=180nm
	Width=517.5nm	Width=1.21um

Following results in Fig. 3 to Fig. 8 show behavior of 1-bit full adder for CMOS and Transmission gate logic style for different technologies (180nm.45nm, 32nm).Simulation has been carried out for the supply voltage of 1V

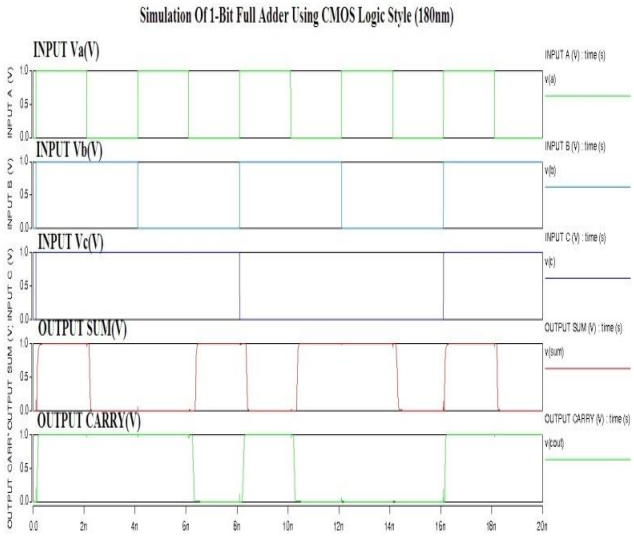

Figure 3: Simulation result of 1-Bit Full Adder using CMOS logic style using 180 nm technologies

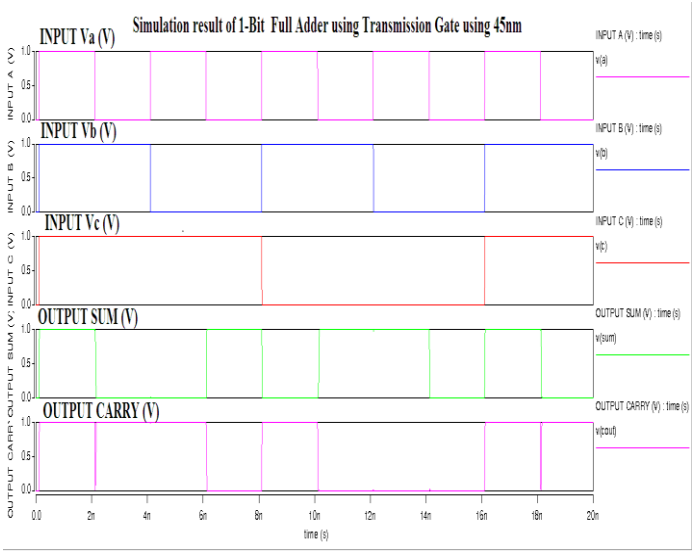

Figure 4: Simulation result of 1-Bit Full Adder using CMOS logic style using 45 nm technology

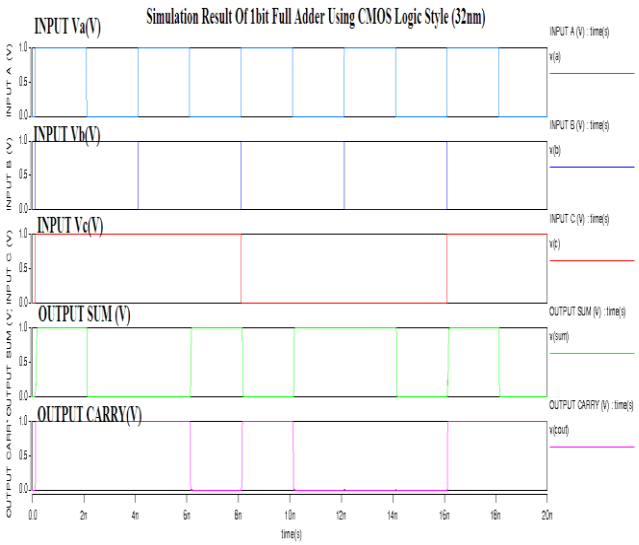

Figure 5: Simulation result of 1-Bit Full Adder using CMOS logic style using 32 nm technology

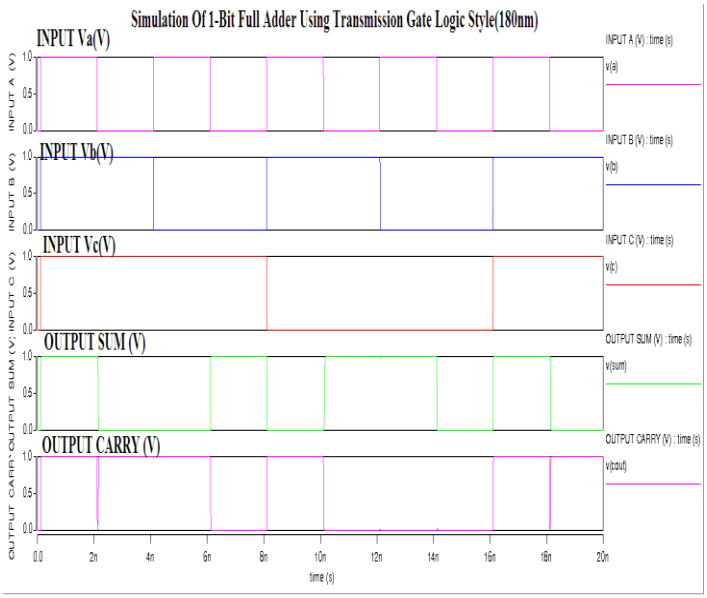

Figure 6: Simulation result of 1-Bit Full Adder using Transmission Gate using 180nm technology

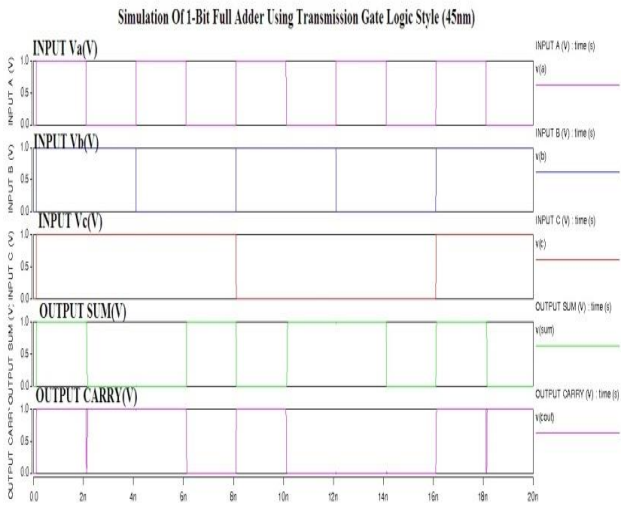

Figure 7: Simulation result of 1-Bit Full Adder using Transmission Gate using 45 nm technology

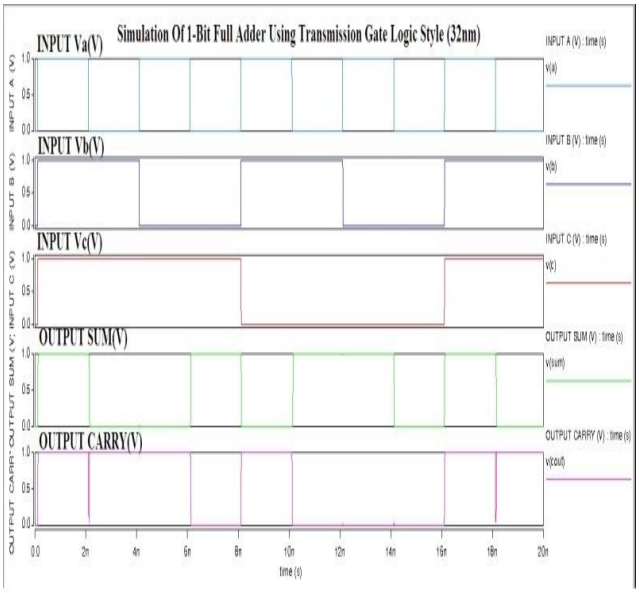

Figure 8: Simulation result of 1-Bit Full Adder using Transmission Gate using 32 nm technology

V. PERFORMANCE ANALYSIS

Table 2: Performance parameters of 1-bit CMOS & Transmission gate Full adder

Parameters	**1-Bit full adder using CMOS logic style**			**1-Bit full adder using Transmission Gate logic style**		
Technology (nm)	180	45	32	180	45	32
Transistor Count	28	28	28	20	20	20
Tool	Spice Simulator	Spice Simulator	Spice Simulator	Spice Simulator	Spice Simulator	Spice Simulator
Supply Voltage (V)	1	1	1	1	1	1
Average power (uW)	7.057	1.735	1.474	6.792	1.677	1.193

From the above Table 2 following is the comparative analysis of 1-Bit full adder circuit:

- On comparing performance analysis, it is observed that 1-bit full adder using CMOS and Transmission gate, the average power for CMOS is more than the Transmission gate for different technology.
- In CMOS technology, it is found that keeping the voltage constant, as technology decreases from 180nm to 32nm, the transistor count remains the same but the average power decreases from 7.057uW to 1.474uW.The minimum power is 1.474uW for 32nm.
- In Transmission gate technology, it is found that keeping the voltage constant, as technology decreases from 180nm to 32nm, the transistor count remains the same but the average power decreases from 6.792uW to 1.193uW.The minimum power is 1.193uW for 32nm.
- CMOS 1-bit full adder contains more number of transistors than Transmission gate 1-bit full adder, hence it is bulky.

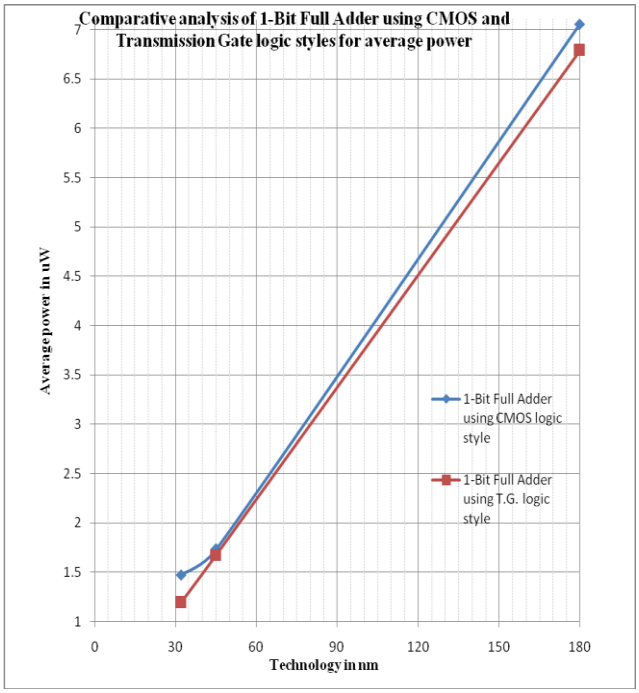

Figure 9: Comparative analysis for 1-bit full adder using CMOS and Transmission gate logic style

Figure 9 shows comparative analysis of 1-Bit full adder using CMOS and Transmission gate logic style. From the graph it is observed that

1) The average power increases as the technology increases.
2) The 1-bit full adder designed using transmission gate has lesser average power than CMOS for all the technologies.

VI. CONCLUSION

Low power consumption is preferred in V.L.S.I systems owing to their greater reliability. In this paper, the performance of 1-Bit full adder using CMOS and Transmission gate logic styles are compared and analyzed over three different technologies (180nm, 45nm, 32nm) for the parameters like average power supply voltage, transistor count. It is observed that within a given logic style, as the technology decreases the average power decreases with decrease in the area. Also it is observed that for one given technology the transmission gate based 1-Bit adder has lower average power, less transistor count and smaller area than the CMOS based 1-Bit full adder circuits.

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