Comparative performance analysis of JL DG- MOSFET with Underlap JL DG-MOSFET

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***Abstract*-The CMOS technology has seen immense development in the last decade with number of analog and RF applications. An important aspect of this technology now is system on chip applications i.e. SOC applications. Numerous investigatory studies have been done on Junctionless devices to examine their aptness for various applications. Though the absence of junctions and presence of double gates enhanced the device performance, it was sighted to be susceptible to SCEs (Short Channel Effects). The replacement of this architecture by an Underlap device showed reduced SCEs. The gate underlap also reduces gate edge direct tunneling leakage [9] and gate sidewall fringe capacitance, resulting in an improved circuit performance. This paper investigates the D.C, analog and linear performance of the aforesaid devices. Further comparative investigations are done using TCAD SILVACO device simulator to establish the superiority of either device for specific applications.**

Keywords— Junction less transistor, Transconductance(gm), Transconductance Generation Factor(gm/id),Parasitic capacitances

I. INTRODUCTION

The remarkable performance of CMOS based devices has made the CMOS technology a formidable force in the digital market. With the need for increase in packaging density on IC and low power consumption the downscaling of devices has become an obvious need [1]. However downscaling leads to more pronounced SCEs like DIBL(Drain Induced Barrier Lowering),high off state leakage current, Threshold voltage roll off, bringing down the device performance [3-6]. In order to overcome DIBL and SCEs the Double Gate (DG) structure has been proposed. The absence of junctions (Junction-less) offers simplicity of design as well as overcomes the problem of leakage current. A plethora of investigative studies have been done on JL DG-MOSFET establishing their superior DC, Analog, RF and Linear performance. The substrate of the device proposed is Silicon (Si) and oxide layer is SiO_2. However, aggressive downscaling in sub 45nm region has led to effect of SCEs even in the double gate device. Consideration of fabrication defects and theoretical studies have brought another device with Underlap Gate structure into domain of research. The basic D.C investigation is necessary to establish the efficiency of device under biasing conditions.
Analog investigation and study of parasitic capacitances of device are necessary to model the device. Linearity property of any device is highly important to predict their performance in mobile communication, computing & multimedia application has resulted interest in SOC application based on CMOS technologies, which is low cost. The inter modulation distortion & higher order harmonics at the output need to be mitigated. Various figure of merits (FOM) such as Transconductance(g_m), Gate to source and Gate to drain capacitances(C_{GS} and C_{GD}), Transconductance Generation Factor(TGF) and VIP2. Further, different parameters like work function, substrate doping, oxide layer of both the devices are also studied in order to obtain overall device performance. The result obtained from both models are verified and simulated for obtaining a good result, validating the models.

This paper is organized as follows: Section II illustrates the device structure and the simulation setup considered in this study. Section III provides the variation of analog performance parameter as a function gate-length downscaling. In section IV gives the idea about the impact of gate length downscaling on RF performance. Section V provides the Linearity performance. Finally, in section VI, the conclusions is drawn.

II. DEVICE STRUCTURE AND SIMULATION

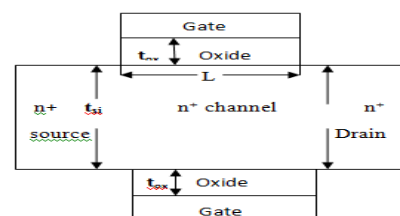


Fig. 1: 2D schematic view of a DG JL FET

The structure under consideration have uniform doping type and concentration 10^{19} cm^{-3} throughout the structures. L is the channel length with an oxide thickness t_{ox}=0.8nm,thickness of **Si** body t_{si}=10nm. A p-type polysilicon gate with work function ϕ_m=5.5eV is used. The MOS model is selected using Newton Maxtrap method. while AuGe/Ni/Au is used for the formation of ohmic contacts in different terminals. The two dimensional device performances are simulated for JL-DG-MOSFET and Underlap JL-DG-MOSFET using SILVACO-ATLAS [10]. In this simulation Fermi Dirac carrier statistics along with conventional Drift Diffusion (DD) model has been adapted to model carrier transport. Shockley-Read-hall (SRH) recombination model combined with Auger Recombination model has been employed in order to model recombination

characteristics. Newton and Gummel's numerical iteration method are used to solve coupled differential equation such as continuity equation of electron and hole and current equation of electron and hole in ATLAS. The simulation software was used to generate layouts for both normal and underlap device.

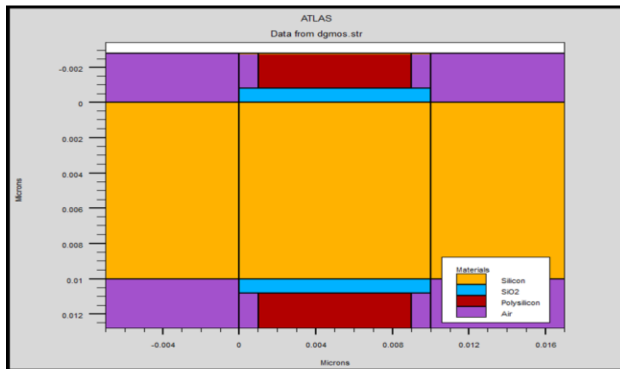


Fig. 2: Device Layout of Underlap JL DG-MOSFET using SILVACO TCAD device simulator for 10nm channel length with Si substrate

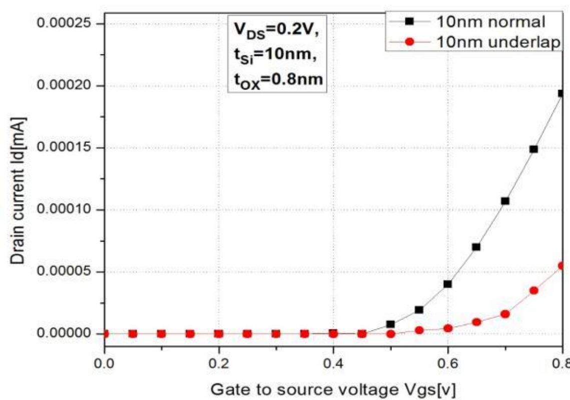
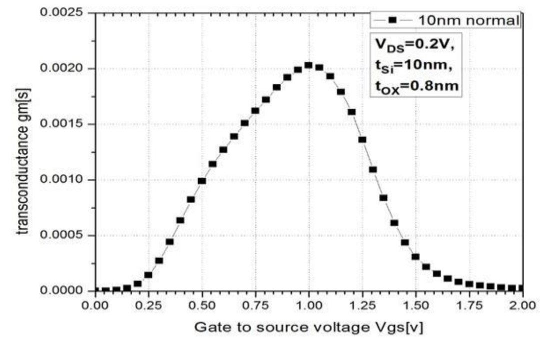


Fig. 3: Variation of Drain Current I_D as a function of Gate-to-source voltage V_{GS} for channel length L=10nm with device parameter values V_{DS}=0.2V, t_{Si}=10nm and t_{OX}=0.8nm

III. ANALOG PERFORMANCE INVESTIGATION

This Section shows evaluation of the analog performance parameter of Junction-less DG MOSFET and Underlap Junction-less DG MOSFET.



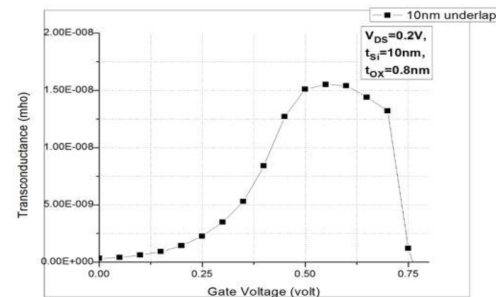


Fig. 4. Plot of variation of transconductance (gm) as a function of Gate-to-source voltage Vgs for different Channel Length L=10nm for normal and underlap device with device parameter values V_{DS}=0.2v, t_{si}=10nm and t_{ox}=0.8nm.

t is clear that in Fig. 4 that transconductance increase with Gate to source Voltage of both the devices are comparable.
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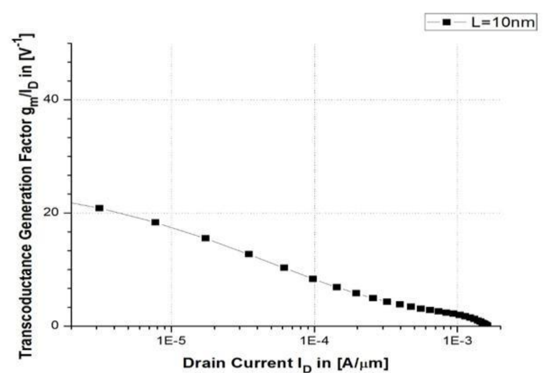

Fig.5. Variation of Transconductance Generation Factor (TGF) as a function of Drain current Id for Channel Length L=10nm with device parameter values Vds=0.2V, tsi=10nm and tox=0.8nm.

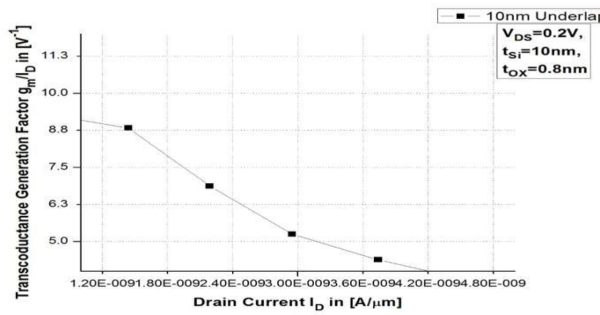

Fig.6. Variation of Transconductance Generation Factor (TGF) as a function of Drain current Id for different Channel Length L=10nm with device parameter values Vds=0.2V, tsi=10nm and tox=0.8nm for Underlap device

Fig. 4&5, this figure of merit shows that the measure of efficiency to convert the current into transconductance. It indicates that lower TGF reduces input device performance and higher power dissipation. It is clear from Fig. 4&5 that lower TGF is obtained with a device of shorter gate length.

IV. RF PERFORMANCE INVESTIGATION

This Section shows evaluation of the analog performance parameter of Junction-less DG MOSFET .The cutoff frequency f_T and the maximum frequency of oscillation f_{max} are two important parameters for evaluating the device potentials for RF applications. The cutoff frequency f_T is the frequency when the current gain is unity ,whereas f_{max} is the frequency when the power gain is unity [11].

Standard figure of merits (FOMs) require to examine the RF performance are,

(a) Cut-off frequency (f_T)

(b)Maximum frequency of oscillation (f_{max})

(c) Gain Bandwidth Product (GBW)

The standard analytical expression for evaluating f_T, f_{max}, GBW are given by

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1+2\frac{C_{gd}}{C_{gs}}}} \approx \frac{g_m}{2\pi\left(C_{gd}+C_{gs}\right)} \approx \frac{g_m}{2\pi C_{gg}} \quad (1)$$

$$f_{max} \approx \frac{g_m}{2\pi C_{gs}\sqrt{4\left(R_s+R_i+R_g\right)\left(g_{ds}+g_m\frac{c_{gd}}{c_{gs}}\right)}} \quad (2)$$

(3)

$$GBW = \frac{g_m}{2\pi \times 10 \times C_{gd}}$$

where, Cgs , Cgg , Cgd represents the Gate to Source, Gate, Drain capacitance and total gate capacitance including the fringing and overlap parasitic capacitances. .

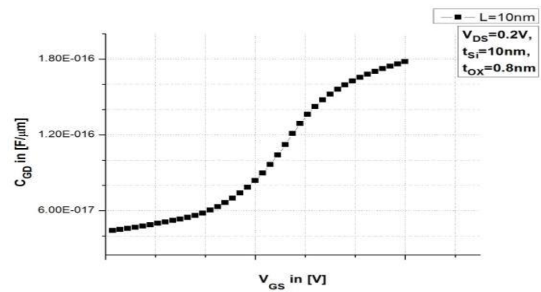

Fig. 7 Variation of Gate-to-Drain Capacitance C_{gd} as a function of V_{gs} for Channel Length L=10nm with device parameter values Vds=0.2V, tsi=10nm and tox=0.8nm

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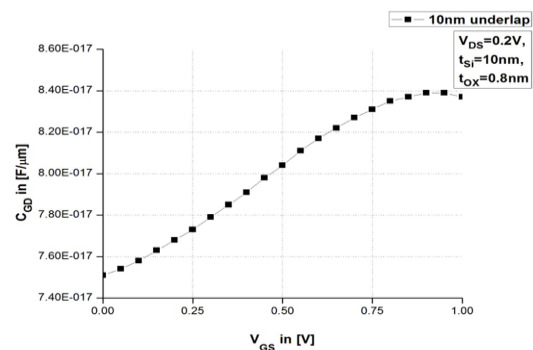

Fig. 8: Variation of Gate-to-Source Capacitance C_{gs} as a function of V_{gs} for different Channel Length L=10nm, with device parameter values Vds=0.2V, tsi=10nm and tox=0.8nm for Underlap device

Fig. 7 shows the plot of C_{gs} as a function of V_{gs} for 10nm JL DG-MOSFET. Fig. 8 shows the plot of C_{gs} as a function of V_{gs} for 10nm underlap JL DG-MOSFET. As we see the values of C_{gs} are substantially lower compared to normal JL DG MOSFET.

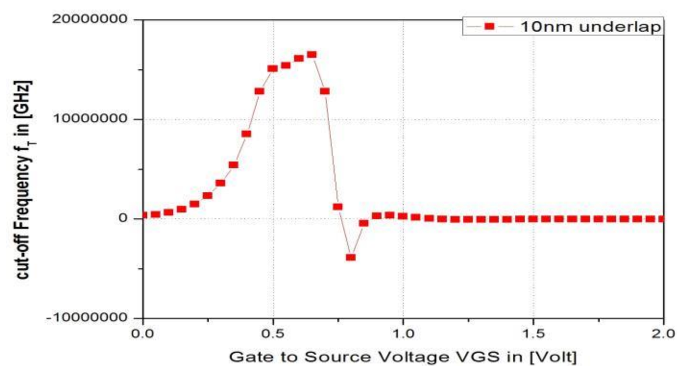

Fig. 9: Variation of Cut-off Frequency (f_T) as a function of Gate to Source Voltage V_{gs} for different Channel Length L=10nm with device parameter values V_{DS}=0.2V,t_{Si}=10nm and t_{OX}=0.8nm.

At the sub-threshold region f_T is proportional to a $1/L^2$ as gm proportional to1/L and C_{gd}/C_{gs} proportional to L f_T attains a

lower value and increases with I_D until it reaches a maximum value at a specific gate bias. At maximum transconductance f_T is at maximum point and gate to source/drain capacitance is minimum.

V. LINEARITY TESTING

Linearity is an essential requirement in all RF system in order to ensure minimal inter-modulation and higher order harmonics at the output. Intermodulation Distortion (IMD) due to non-linearity, generate unwanted signal with different frequencies [12]-[15]. These unwanted (noise) signals may interfere, change or even corrupt the desired output components. So there is a need to estimate the linearity distortion analysis for JL DG MOSFETs as well as Underlap device. A transistor-level linearization is more appropriate for power amplifiers in portable systems, which requires an analysis of the linearity behavior at the device level.

In this section we investigate the RF performance using standard figure of merits

$$VIP_2 = \frac{4.g_{m1}}{g_{m2}}\Big|_{const.V_{ds}}, \quad (4)$$

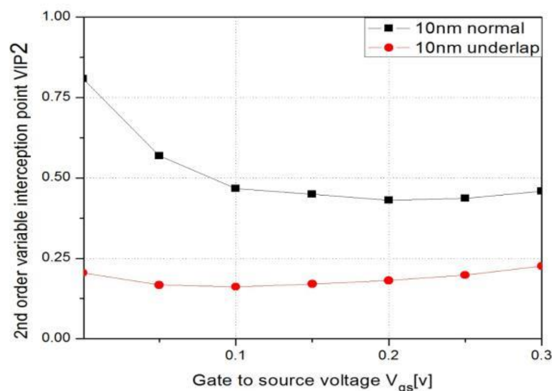

Fig. 10: Variation of VIP_2 as a function of Gate to Source Voltage V_{gs} for Channel Length L=10nm for simple device compared with underlap with device parameter values V_{DS}=0.2v,t_{Si}=10nm and t_{OX}=0.8nm.

The comparison plot shows distinctively low VIP2 values for the Underlap device compared to the simple JL DG MOSFET. It can be a prospective linear device.

VI. CONCLUSION

In this paper, selected FOMs(Figure Of Merits) of DC, Analog, RF and linearity performances of JL DG MOSFET and Underlap JL DG MOSFET were compared in terms of transconductance Generation Factor(TGF) gm/I_{ds}, cutoff frequency f_T, gain band width product GBW and VIP_2.Comparison has been performed for different channel length and it was observed that device shows excellent RF performance for shorter channel length but the analog performance of the Device was poor. Hence, this paper concluded that Underlap JL DG MOSFET is a competitive contender for next generation SOC applications with an improved linearity and analog performance. The major drawback of the device is its high power dissipation and low TGF. However, it may be a contender for select RF/Analog applications. Our work also opens up probable substrate variations, change in number of gates and their material, use of higher order dielectrics and other investigations.

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