Comparative Analysis of Various Adiabatic Logic Techniques

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***Abstract*:This paper present Power Consumption being the prime concern of VLSI designers has always been the source of motivation behind today's VLSI state of the art. Adiabatic technique is an emerging field promising significant reduction in the power consumption of the chip. Among several existing techniques, exhaustive comparison is made between SCRL, ECRL and PFAL techniques. The performance of each circuit is studied in terms of the maximum frequency of operation, area overhead over its conventional counterpart and the circuit energy consumption with different load capacitance. Power measured for adiabatic logic techniques and conventional CMOS circuit shows substantial difference in values. Circuit simulation is carried out in LTSPICE.**

Keywords— Adiabatic technique, Power, Conventional CMOS circuit.

I. INTRODUCTION

Adiabatic technique plays a vital role in portable devices that are inherently available with constraint in battery life. Long battery operating life requirement of portable devices can be addressed by investigating adiabatic logic.

To enhance the battery life of integrated circuit devices several design styles are devised among which the most promising technique is adiabatic logic. Due to increase in demand of hand held devices, we require enduring power battery life. Moreover today's IC's work at very high speed implying more switching activity .Consequently they tend to dissipate large power which necessitate use of bulky heat sinks. This imposes increase in device area. So we need to develop power efficient techniques to overcome the area overhead. Power dissipation is main constrain when it comes to portability. Power dissipation in a conventional CMOS circuit can be: (1)Dynamic Power Dissipation, the power which is consumed by device when it is in switching operation. Dynamic power also consist of short- circuit power and (2) Static Power Dissipation, the power which arises when system is in standby mode or not powered . There are different strategies available at different level in VLSI design process for optimizing the power consumption level. Supply voltage scaling has been also adapted for power minimization. However reducing the supply voltage affects the circuit speed also. So, the adiabatic logic techniques are explored here in this paper to reduce the dynamic power. In this paper, several adiabatic techniques like ECRL, PFAL and SCRL are analyzed using inverter circuit for power dissipation. LTSPICE [3] is used for circuit implementand simulation. Transistor count for implementation of SCRL, ECRL and PFAL are 2, 4 and 6 respectively. Power consumed in microwatt for inverter using SCRL, ECRL and PFAL are observed to be279.16 µW, 353.55µW and 334.84µW respectively. From the result it is found that fully adiabatic technique SCRL has less power and less transistor count. But it is slow. While the output levels for quasi adiabatic technique PFAL is better than ECRL based circuit. But in PFAL, transistor count increases.

ADIABATIC LOGIC : This term comes from thermodynamic system which means no heat transfer from system to environment and vice versa. Adiabatic logic is also known as "energy recovery logic" as it reuses the energy. It indicates that instead of dissipating the stored energy during the charging process, it recycles the energy back to the power supply thus reducing the power dissipation. Adiabatic techniques are based on adiabatic logic principle. Following section describe how the adiabatic logic differs from conventional switching. A. Conventional Switching As seen above, the power dissipation have mainly 3 sources: dynamic, short circuit and leakage power dissipation. Among all, dynamic power dissipation is main component. The equivalent CMOS logic for charging and discharging circuit is shown in figure (1), where the equation of the power dissipation is given by,

Power = α .CL . Vdd2. fclk + Isc .Vdd + Ileakage .Vdd

First term represents the dynamic power, where α is the switching activity, CL is the loading capacitance, fclk is the clock frequency and Vdd supply voltage. The second term represents short circuit current Isc which arises when both the NMOS and PMOS transistors are simultaneously active, resulting into conducting current directly from supply to ground. Last is leakage current Ileakage which can arise from substrate injection and sub threshold effects is primarily determined by fabrication technology considerations.

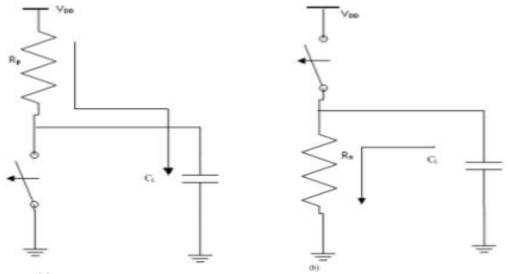

Fig1.Conventional CMOS a) Charging b) Discharging2.2

Adiabatic Switching Adiabatic switching can be achieved by ensuring that the potential across the

switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time-varying voltage source or constant current source[12][13][14] as shown in Fig. 2.

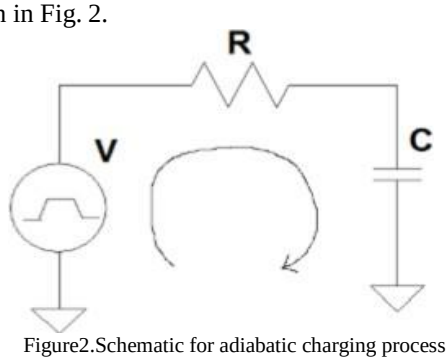

Figure2.Schematic for adiabatic charging process

Here, R represents the on resistance of the PMOS network. Also note that a constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage VC is zero initially, the variation of the voltage as a function of time can be found asVc (t) = Is .t / 2

The amount of energy dissipated in the resistor R from t = 0 to t = T, Ediss = R. ∫ T Is 2 .dt = R. Is2.T (4)

$$Ediss = \frac{R \times C}{T} \times C \times Vc^2$$

From (5) we can say that the dissipated energy is small if the charging time T >>2RC so it can be made small by increasing the charging time.

II. ADIABATIC LOGIC FAMILIES

Types Of Adiabatic Logic,

- Fullyadiabatic families
- Quasi adiabatic families

QUASI ADIABATIC FAMILIES:

A quasi adiabatic process is a thermodynamic process that happens infinitely slowly. No real process is adiabatic, but such processes can be approximated by performing them very slowly. Any reversible process is necessarily a quasi adiabatic one. However, some quasi adiabatic processes are irreversible, if there is heat flowing (in to or out of the system) or if entropy is being created in some other way. An example of a quasi adiabatic process that is not reversible is a compression against a system with a piston subject to friction although the system is always in thermal equilibrium, the friction ensures the generation of dissipative entropy, which directly goes against the definition of reversible. Adiabatic logic circuits are one that are based on adiabatic switching principal.Quasi adiabatic circuits have simple architecture and power clock system. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock [5].Popular Partially Adiabatic families include the following:

III. FULLY ADIABATIC FAMILIES:

1. Efficient Charge Recovery Logic (ECRL).
2. 2N-2N2P Adiabatic Logic.
3. Positive Feedback Adiabatic Logic (PFAL)
4. NMOS Energy Recovery Logic (NERL).
5. Clocked Adiabatic Logic (CAL).
6. True Single-Phase Adiabatic Logic (TSEL).
7. Source-coupled Adiabatic Logic (SCAL).

Among these logic families two of them are chosen ECRL and PFAL, which shows the good improvement in power dissipation and mostly used as reference in new logic families for less power dissipation.

Efficient Charge Recovery Logic (ECRL):

The schematic and simulated waveform of the ECRL inverter gate is shown in Fig.3 and Fig.4 respectively. Initially, input ‘in’ is high and input ‘/in’ is low. When power clock (pck) rises from zero to VDD, since F is on so output ‘out’ remains ground level. Output ‘/out’ follows the pck. When pck reaches at VDD, outputs ‘out’and ‘/out’ hold logic value zero and VDD respectively. This output values can be used for the next stage as an inputs. Now pck falls from VDD to zero, ‘/out’ returns its energy to pck hence delivered charge is recovered. ECRL uses four phase clocking rule to efficiently recover the charge delivered by pck. For detailed study follow the reference [10] and ‘/out’ hold logic value zero and VDD respectively. This output values can be used for the next stage as an inputs. Now pck falls from VDD to zero, ‘/out’ returns its energy to pck bar are generated .

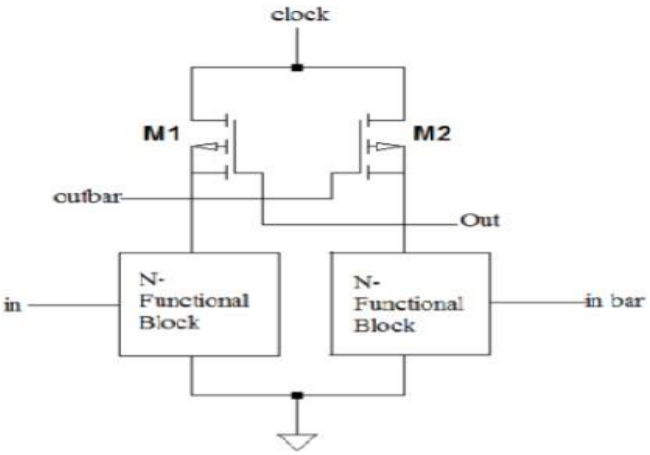

Fig. 4 Schematic for ECRL Logic Block [5]

So the recovery path to the power clock is disconnected. Thus, it is incomplete recovery. Vtp is the threshold voltage of PMOS transis

tor.

The amount of loss is given as E=C.|Vtp|2/2 From the above equation, non-adiabatic energy loss is dependent on the load capacitance and independent of the frequency of operation. The ECRL circuits are operated

with the four- phase supply clocks. When the output is directly connected to the input of the next stage, only one phase is enough for a logic value to propagate. ECRL consume unnecessary power with two-phase clocking, because transition of logic value in the previous stage can affect the next stage. So four-phase clocking is recommended for effective energy saving [1]. Initially, in signal is at high and in bar signal is at low. At the beginning of a cycle, supply clock rises from zero to VDD, out remains at a ground. This turns on N2 and out bar follows supply clock through M1. When supply clock reaches VDD, the out and out bar holds valid logic levels. These values are maintained during the hold phase and also used as inputs for the evaluation of the next stage. After the hold phase, supply clock falls down to a ground, out returns its energy to clock so that the charge is recovered. A major disadvantage of this circuit is the coupling effects, because the two outputs are connected by the PMOS latch also two complementary outputs can interfere each other.

Positive Feedback Adiabatic Logic (PFAL):

Positive feedback adiabatic logic was introduced in 1996 by Vetali [12-14] and shows very positive aspects in addressing the power issues. PFAL comes in dual rail logic family which requires availability of both the complementary and uncomplimentary inputs for the logic function. The logic function (F) and (Fbar) are implemented using NMOS networks alongside the two cross coupled inverts as latch known as sense amplifier which drives the two complementary outputs of the circuit. It consists of two PMOS and two NMOS switches which ultimately prevents the output terminals from degradation of logic levels [15-17]. One of thelogic blocks connects the concerned input to the power clock with a low resistance path and on the same time the other function network provide a very high resistance in between the power clock and the other concerned output. But the inverter's network provides the second output a conducting path to the ground. In this way one of the two outputs (either complementary or un-complementary one) is pulled up to the power clock and other down to the ground. The same is evident from the basic structure depicted in the Figure 1.

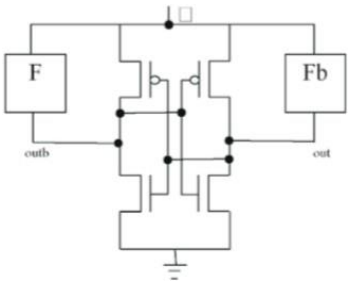

Fig.5 Basic structure of PFAL

Positive Feedback Adiabatic Logic (PFAL) shows the lowest energy consumption compared to other partial logic technique and a good robustness against technological parameter variations. The general schematic of the PFAL gate is shown in Figure. Here the latch made by the two PMOS M1-M2 and two NMOS M3-M4, that avoids a logic level degradation on the output nodes. The two N- functional blocks are placed parallel to

PMOS transistor and it forms a transmission gate [7].

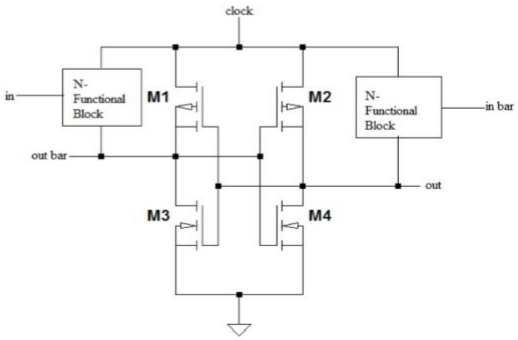

Fig. 6 Schematic for PFAL Logic Block [5]

The two major differences with respect to ECRL are that the latch is made by two PMOS transistors and two NMOS transistors, instead of only two PMOS transistors as in ECRL logic, and that the functional blocks are in parallel with the transmission PMOS transistors [8]. Thus the equivalent resistance is smaller when the capacitance needs to be charged [9]. During evaluate phase of clock, in is high and in bar is low. Also one of the two NMOS (N1 at in side, N2 at in bar side) from N-functional block, N1 is on. Out follows raising edge of power clock by charging nodal capacitance Cout. At this time, N1 remains off because in bar signal is low. Now because of high out at its gate, M3 conducts to pull low out bar. This results in Charging of out node as g M2 was pushed ON. Now M1 is off and M3 is on due to high out at their gate terminal. Also M4 is off due to low out bar at its gate terminal. During hold phase, in starts falling and N2 continues its conduction until clock is more than threshold voltage of PMOS, beyond its stops conductions. During recovery phase, recovery occurs through M2 PMOS transistor. Then, conduction happens through M2 and N2. Now, when in bar is high, N2 conducts providing ground to out. This avoids floating output problem [10-11]. B. Fully Adiabatic Circuits Some Fully adiabatic logic families include: Pass Transistor Adiabatic Logic (PAL) and Split- Rail Charge Recovery Logic (SCRL). Full-adiabatic circuits do not have non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. Here all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits have problems with respect to the operating speed and the power clock synchronization [12]. One of them is SCRL which is described below:

1) Split- Rail Charge Recovery Logic (SCRL): The schematic of the SCRL inverter is shown in Fig. The SCRL inverter consists of one PMOS and one NMOS with time varying supply and also an additional transmission gate at the output [12].

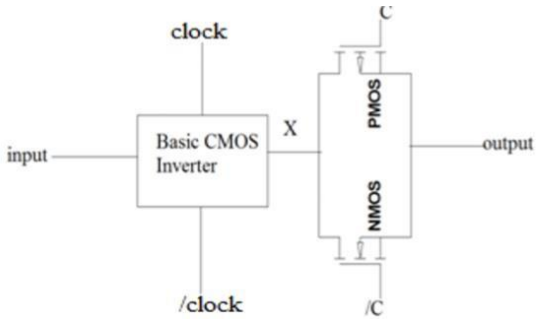

Fig. 7 Schematic for SCRL Inverter

The basic CMOS inverter have two complementary power clocks 'clock' and '/clock' rather than Vdd and ground terminals. The power clock varies between Vdd and Vdd/2 whereas /clock varies between Vdd/2 and 0. Initially all the nodes (clock and /clock) are at Vdd/2, at this time the transmission gate is turned OFF by the control signals C and /C. The output is also at Vdd/2. After appling valid input the transmission gate at the output is gradually turned ON by swinging C and /C to Vdd and ground respectively. clock and /clock also swing to Vdd and ground respectively. If the input to the gate is Vdd then the node x and the output will follow /clock and ground but if the input was at ground the node x and output follow /clock and Vdd.

IV. CIRCUIT SIMULATION AND IMPLEMENTATION

The CMOS inverter is tested by LTSPICE [3] simulation using a standard CMOS technology for different set of load capacitances.. In the following subsections, inverter circuits have been implemented based on mentioned SCRL, ECRL, PFAL designs and measured the power. The results pertaining to maximum frequency, minimum voltage, maximum load and area are tabulated in Tables. The results are graphically analyzed and shown in figure.

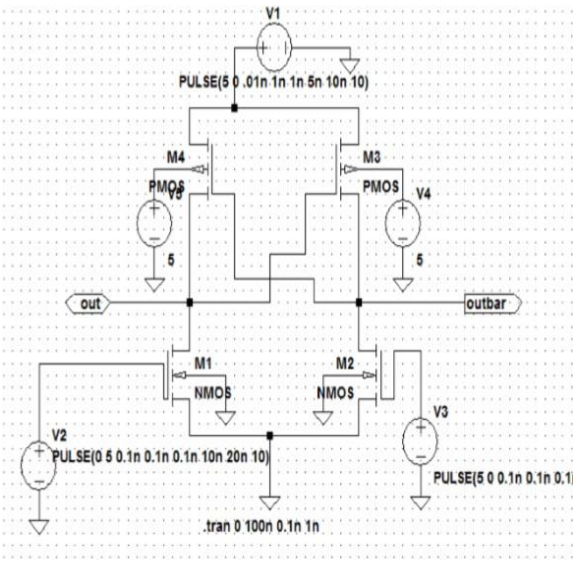

Fig.8 ECRL inverter simulation in LTSPICE

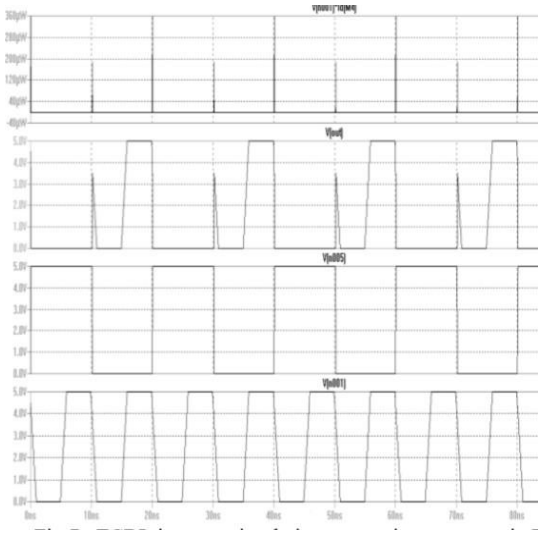

Fig.9 ECRL inverter simulation power, input, output in LTSPICE

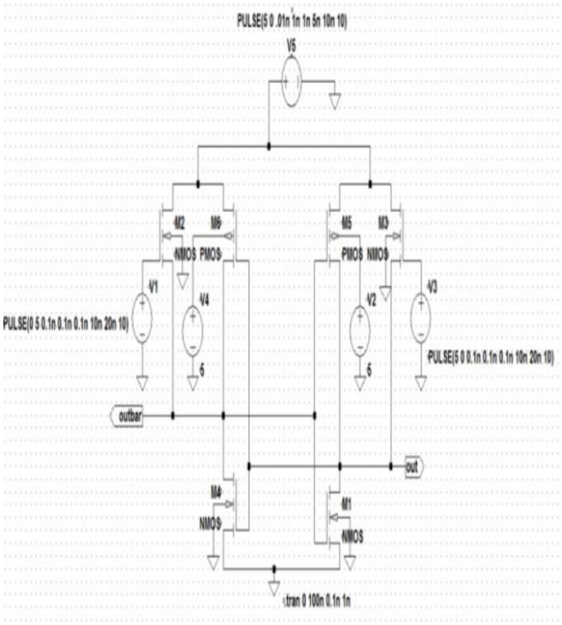

Fig.10 PFAL inverter simulation in LTSPICE

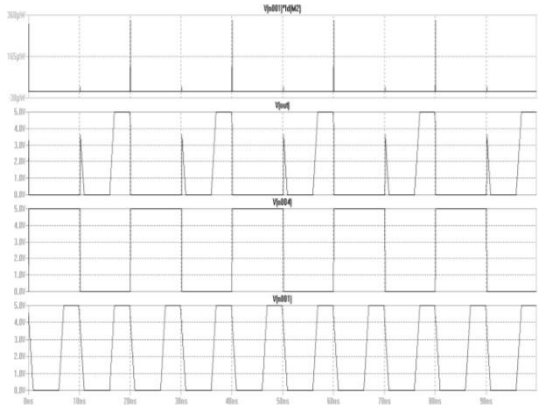

Fig.11 PFAL inverter simulation power, input, output in LTSPICE

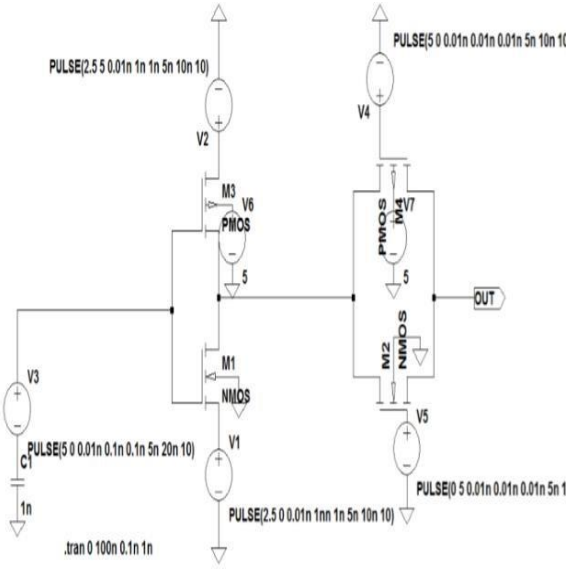

Fig.12 SCRL Inverter Simulation in LTSPICE

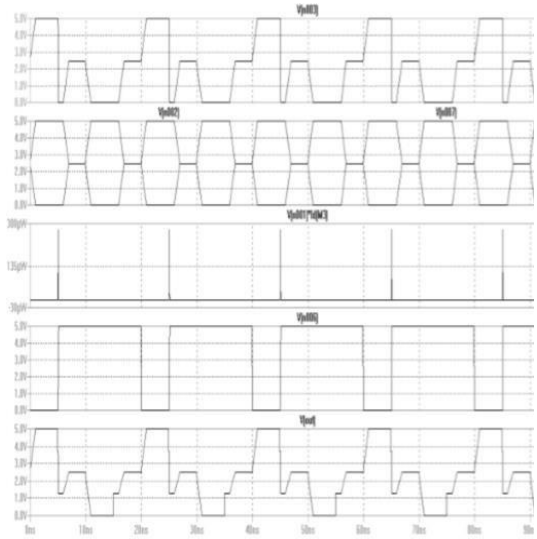

Fig.13 SCRL inverter simulation power, input, output in LTSPICE

TABLE I Comparison of power dissipation in SCRL, ECRL and PFAL inverters with conventional CMOS inverter

Technology	Power Dissipation
Conventional CMOS inverter	1.13mW
SCRL inverter	279.16uW
ECRL inverter	353.55uW
PFAL inverter	334.84uW

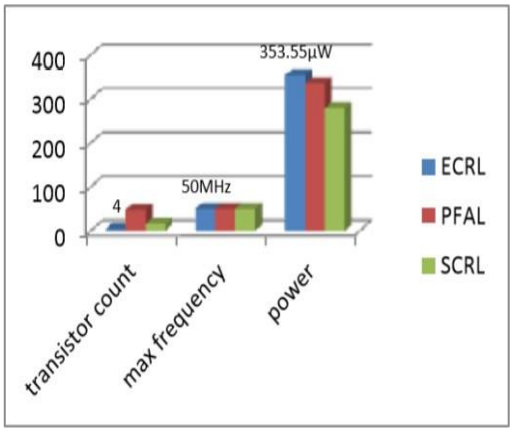

Fig.14 Graph for Transistor count, maximum frequency and power consumption by inverters

TABLE II

Power estimation with different load capacitances

	0.1fF	0.01fF	0.001fF
ECRL	119.03uW	236.13uW	233.71uW
PFAL	273.47uW	289.06uW	294.68uW
SCRL	243.39uW	275.68uW	280.63uW

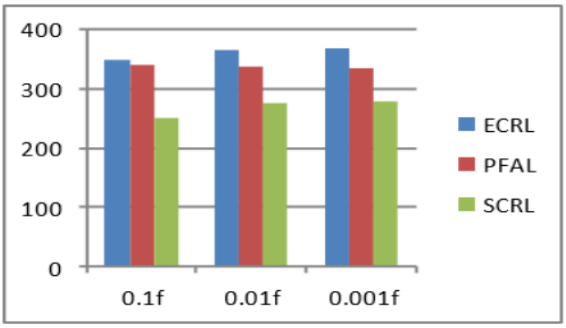

Fig.15Graph for energy for different load capacitances

V. CONCLUSIONS

From the above results, it can be concluded that circuits based on adiabatic techniques consumes very less power as compared to its conventional counterparts. The fully adiabatic technique recovers more charge and it has less power than partial adiabatic techniques. So SCRL has less power than ECRL and PFAL techniques, but this technique uses split level supply clocks. Thus, clock synchronization is more complex here. Partial adiabatic techniques ECRL and PFAL are power effective techniques but ECRL has less power than PFAL when connected with different load capacitances as depicted in Table II. PFAL has more transistor counts and so it consumes more area.

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