Comparative Analysis of Noise, Power and Area of 4 Bit Braun Multiplier and Baugh Wooley Multiplier with Minimum Number of Transistors in 45nm Technology

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***Abstract*— A central processing unit needs a considerable amount of processing time in performing logical operations, arithmetic operations, particularly multiplication operations. Multiplication is one of the arithmetic operations which require substantially more number of hardware resources and processing time than addition and subtraction. A multiplier is consist of mainly AND gates and Full Adders. Now a day's resources are an important factor in case of any design. Any design must have less number of resources as well as it must be power efficient, noise immune. This paper presents a new high speed and Power efficient 4-bit Braun Multiplier and 4 bit Baugh Wooley Multiplier with less number of CMOS transistors. The circuit diagram is tested in 0.045µm i.e. 45 nm Technology. All the designs have been designed in DSCH2. Also Noise, Power and Delay have been calculated in Tanner Spice-13 in 45nm Technology.**

Keywords*— Braun Multiplier Baugh Wooley Multiplier, T-Spice, DSCH2,

I. INTRODUCTION

Multiplication is one of the most important operations in digital computer systems because the performance of processors is significantly influenced by the speed of their multipliers and adders [1]. High performance multiplier is the important part of the CPU and DSP.

Multiplier is one of the most important parameter to determine the processor's speed. So, designing of multipliers are essential in Very Large Scale Integration (VLSI) systems and Digital Signal Processing (DSP) architectures applications. The continuing decrease in feature size of CMOS circuits and increase in chip density have made power consumption a major concern in VLSI design. Different types of multipliers have been proposed earlier like Array Multiplier, Tree Multiplier, and Braun Multiplier. In this paper we proposed a new Low Power 4-bit Braun Multiplier. To design a multiplier it is necessary to design an AND gate and Full Adder circuit. The proposed high speed and Low Power 4-bit Braun Multiplier was done using Tanner tools in 45nm technology. The basic arithmetic operation is addition of binary digits, i.e. *bits*. A full adder is one that adds three bits; the third input is produced from a previous addition operation. These Adders can be implemented by using different logic families. In this paper Baugh Wooley Multiplier and Braun Multiplier has been described by minimum number of transistors. 3 transistor AND gates and simulation results has been shown similarly 8 transistor Full Adder and simulation results has been shown also. Next the information about implementation of Braun Multiplier and Baugh Wooley Multiplier and the simulation results for Braun Multiplier Baugh Wooley Multiplier is shown. We have measured power, area and noise and made a comparison of power, area and noise for Braun Multiplier and Baugh Wooley Multiplier.

II. AND GATE

The AND gate is designed by 3 transistors (3T) where both the NMOS are connected in cross-coupled manner i.e. the gate of the first NMOS (A) is connected with the source of second NMOS and vice versa. The inputs are given to the gate of each NMOS. Both the drain of NMOS are sorted and connected with the drain of PMOS. The gate and source of the PMOS are connected to ground. When the input is 00 i.e. A=0 and B=0 the PMOS is ON but both the NMOS are off so the output becomes zero. When the input is 01 i.e. A=0 and B=1 the PMOS is ON so the output becomes zero and similarly for input10 the output becomes zero. In the case of input 11 i.e. A=1 and B=1 the PMOS is off but both the NMOS are ON and the output becomes high. Figure.1 shows the circuit arrangement and the output waveform of the 3T AND Gate.

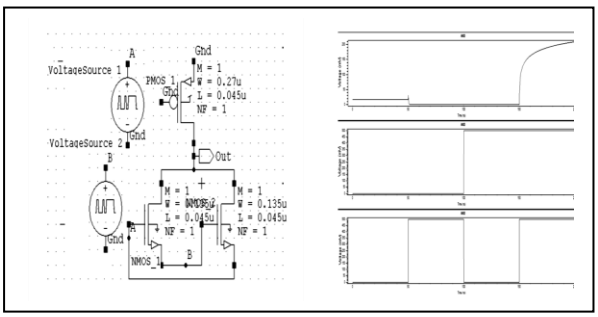

Figure 1: Circuit Diagram and Output waveform of 3T -AND gate

III. FULL ADDER

The design of an eight transistor (8T) full adder using XOR (3T) function and the waveform of Full Adder (8T) is shown in Figure.2. 8T full adder using centralizer output condition contains three modules—Two XOR (3T) gates and one multiplexer (2T). The MUX is controlled by the output of XOR of the first two inputs. The 3T XOR operation is as follows: When the input B is at logic high, the circuit functions like a normal inverter. When the input B is at logic low, the CMOS inverter output is at high impedance. However, the pass transistor M_3 is enabled and the output Y gets the same logic value as input A. However, when A=1 and B=0, voltage degradation due to threshold drop occurs across pass transistor and consequently the output Y is degraded with respect to the input.

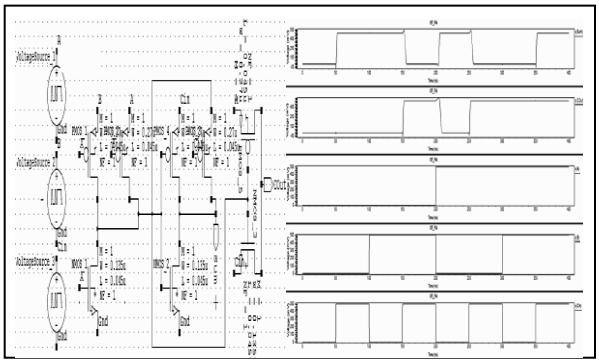

Figure 2: Circuit Diagram and Output waveform of 8T Full Adder

IV. BRAUN MULTIPLIER

Braun multipliers are regularly arranged arrays that have n (n-1) adders and n^2 AND gates, where n is the number of inputs. Each of the inputs A and B of the multiplier cell's product bits is generated in parallel with the AND gates. The partial products can be added to the previous sum of the partial product by using one row of an adder. The carry signals are shifted one bit to the left and then added to the sums of the first adder and the new partial product. They are then passed diagonally downward to the next adder stage. There is no horizontal carry propagation for the first rows. Instead, the carry bit is saved for the subsequent adder stage.

Consider the multiplication of two unsigned n-bit numbers, where

$A = a_{n-1}\ a_{n-2}.....a_0$ is the multiplicand and

$B = b_{n-1}\ b_{n-2}.....b_0$ is the multiplier.

The product $P = p_{n-1}\ p_{n-2}.....p_0$ can be written as follows: $P = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1}\left(a_i a_j\right)2^{i+j}$

The Circuit diagram of 4 bit Braun Multiplier is shown in Figure 3 where the lighter shade of grey denotes the AND gates and the darker shades denotes The Full Adder. Figure 4 shows the T-Spice diagram of the multiplier.

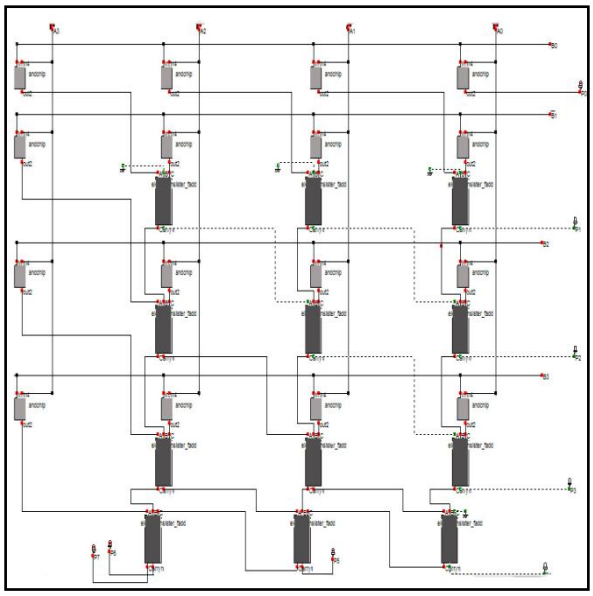

Figure 3: Circuit Diagram and of 4 bit Braun Multiplier

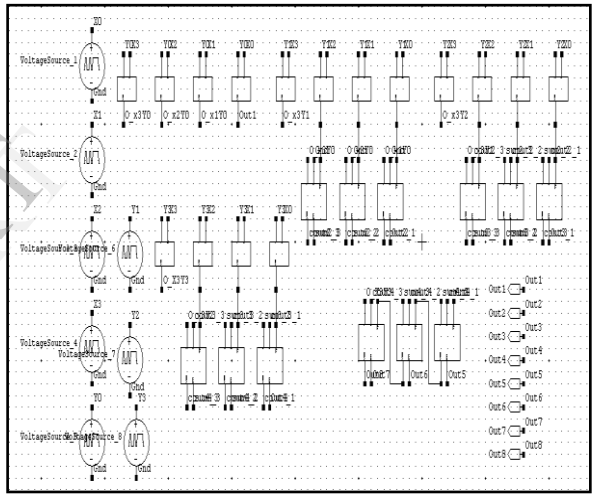

Figure 4: Tanner Spice Diagram and of 4 bit Braun Multiplier

V. BAUGH WOOLEY MULTIPLIER

Baugh Wooley Two's compliment Signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits. Baugh Wooley Multiplier is used for both unsigned and signed number multiplication. Signed Number operands which are represented in 2's complemented form. Partial Products are adjusted such that negative sign move to last step, which in turn maximize the regularity of the multiplication array. Baugh Wooley Multiplier operates on signed operands with 2's complement representation to make sure that the signs of all partial products are positive. The basic blocks are constructed by Grey Cell and White cell, which are given in Figure 5. In case of White Cell a AND gate and a Full Adder is used and in case of Grey Cell the AND gate is replaced by a NAND Gate. The Circuit diagram of 4 bit Braun Multiplier is shown in Figure 6 where the shade of grey denotes the Grey Cells and the similar cells are white coloured are White Cells.

The Full Adders are shown by lighter grey shade. Figure 7 shows the T-Spice diagram of the multiplier.

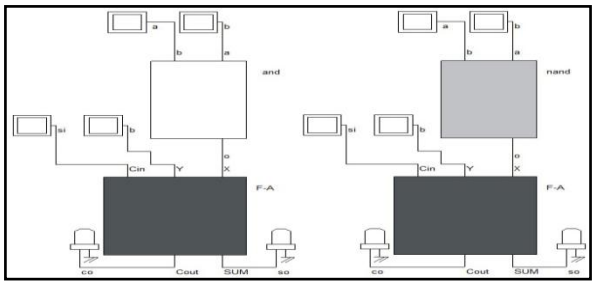

Figure 5: White Cell and Grey Cell

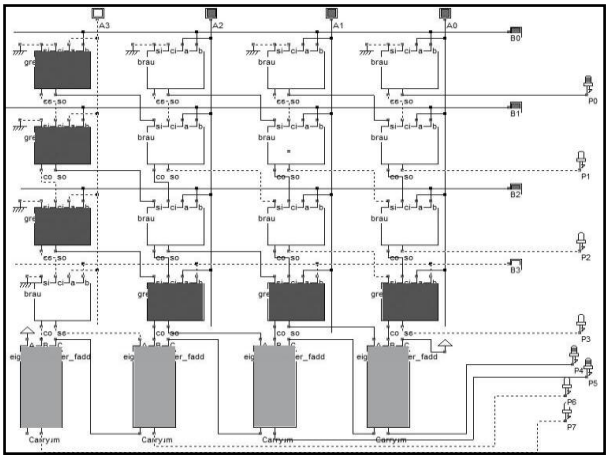

Figure 6: Circuit Diagram and of 4 bit Baugh Wooley Multiplier

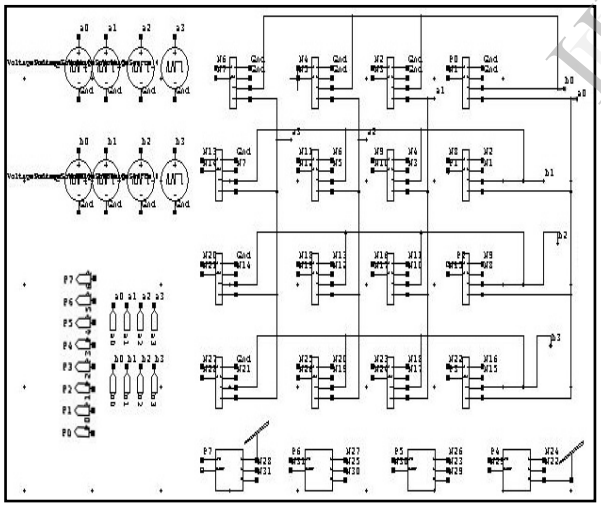

Figure 7: Tanner Spice Diagram and of 4 bit Baugh Wooley Multiplier

VI. RESULT ANALYSIS

The circuit of 4x4 Braun Multiplier and Baugh Wooley Multiplier has been tested in DSCH2. The Noise, Power has been simulated in Tanner Spice-13 in 45nm Technology. The input voltage is taken as 0.5V. The frequency of operation is taken as 1000MHz. The Comparison table of Noise, Power, Area and Transistor count of 4x4 Braun Multiplier and Baugh Wooley Multiplier is given in Table 1.

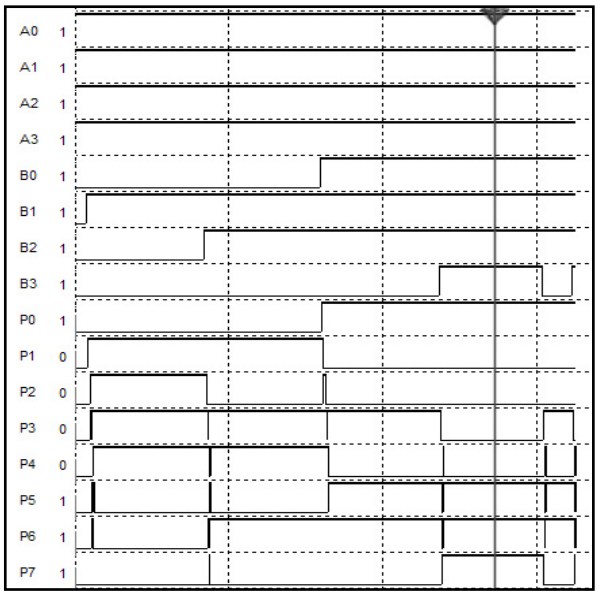

Figure 8: Output Waveform of 4 bit Braun Multiplier

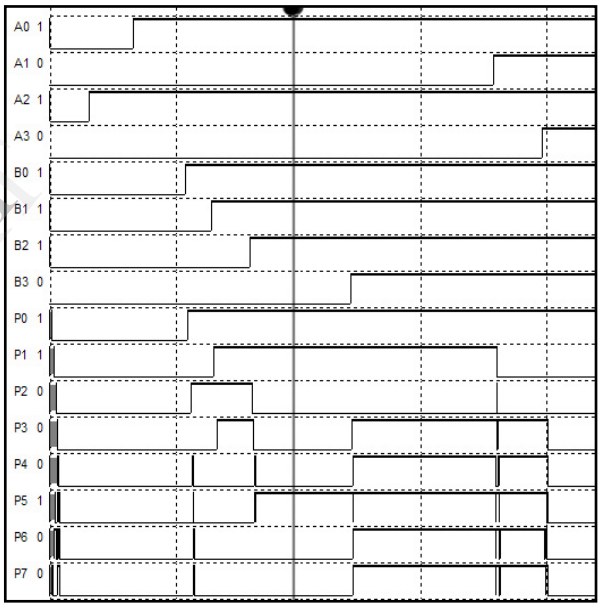

Figure 8: Output Waveform of 4 bit Baugh Wooley Multiplier

Table 1: Comparison between Different Multipliers

	Braun Multiplier	Baugh Wooley Multiplier
Noise (μV)	250	300
Power Consumption	1e-012	5.571e-012
Area	7.5mm^2	7.8mm^2
Transistor Count	144	214

VII. CONCLUSION

In modern technology, it is very necessary for any design, is low power consumption to make it more efficient and cost effective. Here we design the 4 bit Baugh Wooley and Braun multiplier with less number of transistors rather than existing type. Reduction in number of Transistor means minimizing the Power consumption and Area. Moreover in developing and DSP processor or embedded processor, if the blocks are designed with our design, the design may be more efficient. Al last here we also make a comparison between our two designs and the conventional multiplier design to reach the conclusion that our both design are more efficient than other conventional design.

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