Comparative Analysis of Different PWM Techniques in Multilevel Inverters

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***Abstract*: The multilevel inverter now days are very popular for medium voltage applications for different kind of electrical loads such as motor drives for traction load, Electrical Vehicles and Hybrid Electric Vehicles etc. As an improvement, the multilevel converter produces a staircase output waveform with low amplitude of voltage levels which in turns reduces the $\frac{dv}{dt}$ stress across the switch. With addition of levels, the output waveform is a good staircase waveform whose fundamental component is near to the actual stepped waveform, therefore, contains lesser harmonics.**

This work presents a comparative study of the multi-level PWM inverters. The study has been carried out for three different topologies of the multi-level inverter: Neutral Point-Clamped type, Flying Capacitor type and Cascaded H-Bridge inverter taking seven-level three-phase inverter into consideration. Different types of sinusoidal Pulse Width Modulation techniques named as Phase Disposition, Phase opposition disposition and alternate phase opposition disposition being applied to multilevel inverters and %THD have been compared. All these circuit configurations have been modelled in MATLAB/SIMULINK environment and the results are presented in tabular form.

Keywords : MLI, %THD, PD-PWM, POD-PWM, APOD-PWM.

I. INTRODUCTION

Power converter is the interface between the renewable energy source and the load. Multilevel inverter (MLI) is becoming the best choice in Power electronics converters[1]-[4]. The term multilevel power conversion was first introduced twenty years ago. It is not a good practice to connect a single semiconductor device in medium voltage application as it needs more protection and heating problem followed by thermal break away. Thus, the term multilevel comes in to picture with introduction of three level structures. The general concept involves utilization of large number of semiconductor switches in cascaded manner for converting power into small stepped voltage[5]. There are several advantages to multilevel topologies when compared to conventional two level power Conversions[6]. Recently trends towards the multi-level inverter. Researchers have been thinking over the various new and novel configurations along with different modulation strategies like SPWM (sinusoidal pulse width modulation), SVPWM (space vector pulse width modulation). Some application for these converters includes industrial drives, flexible AC transmission system (FACTS), and vehicle propulsion.

Amongst the three basic topologies Cascaded H-bridge, Diode-clamped and Flying capacitor, the cascaded H-bridge structure pulled the attention because of its some unique features that includes the requirement of least number of switches to produce same number of levels[9], [10]. Also, this inverter has the modularity structure for packaging purpose. The other features include the simplest structure and easy control algorithm.

Different PWM schemes have been developed for the inverters to improve the quality of output waveform. The fundamental and high frequency carrier PWM scheme such as the basic one Sine PWM (SPWM), Third harmonic injection, Phase shifted and level shifted, space vector modulation [11], [12] etc. Each PWM owes its benefits and harms. The high frequency PWM is adopted widely to improve the output waveform which in turns reduces the ripples

This paper work includes the comparison of seven level three-phase multilevel inverter configurations of various types from various aspects at different PWM techniques. However, study of different PWM such as APOD (Alternate Phase Opposition Disposition), POD (Phase Opposition Disposition), PD (Phase Disposition) technique for seven level inverter has been compared.

II. POWER CIRCUIT CONFIGURATION

The inverter being known as VSI (voltage source inverter) if the input DC is a voltage source or supply. The word ‘inverter’ in the context of power-electronics symbolizes a power circuits that converts a dc current source or a dc voltage source into ac current or ac voltage.

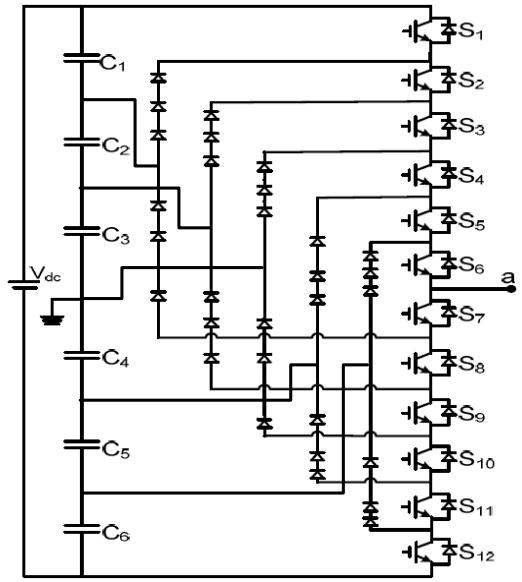


Fig. 1. Power circuit of per phase arrangement of seven level NPC inverter.

Per phase configuration of seven level NPC inverter is shown in Fig. 1 having six capacitors in a DC bus where voltage across each capacitor are distributed accordingly. This configuration named as neutral point clamped (NPC) because except the neutral, there are large number of clamping nodes. Input DC voltage is further being divided by the capacitors connected in series into a set of voltage levels. (N-1) capacitors are required to generate 'N' levels of output phase voltage. These inverters are highly efficient as they are operated at fundamental frequency. The number of output voltage level increases, harmonic content decreases thereby reduces the requirement of filter components.

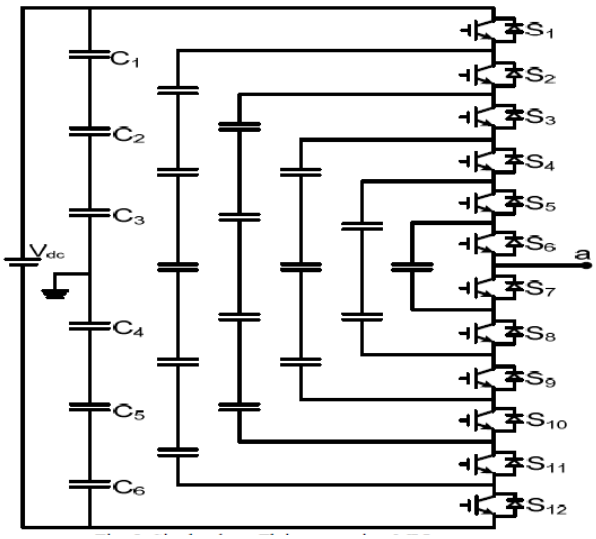


Fig. 2. Power circuit of per phase arrangement of seven level FC inverter.

Per phase configuration of seven level FC inverter is shown in Fig. 2 having twenty one capacitors forms a ladder like structure, the voltage on each capacitor differs from the other capacitors. The voltage levels in the output waveforms determined by increment in the voltage levels at the output where (N-1) capacitors are required. Flying capacitors replaces the clamping diode in this configuration. Zero level is obtained by connecting the load to both the positive and negative terminals through flying capacitor with opposite polarity and more voltage levels can be easily achieved.

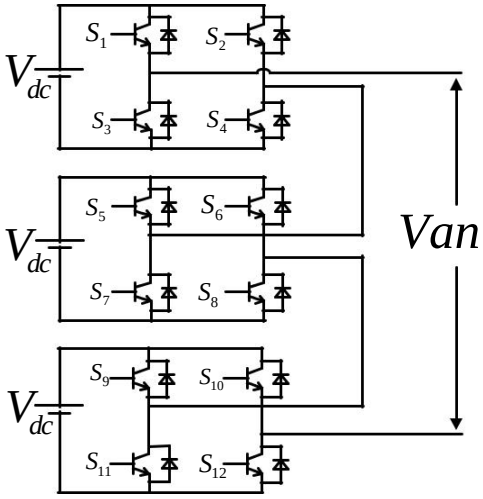


Fig. 3. Power circuit of per phase arrangement of seven level CHB inverter.

Per phase configuration of three-phase seven level CHB inverter is shown in Fig. 3 having one capacitors or voltage source in each H-bridge configuration. This configuration formed by cascading more than one single phase H-Bridge inverters in series. H-bridge inverter generates three different voltage levels. The CHB-MLI requires "M" number of independent voltage sources where N= (2*M + 1) being defined as the phase voltage levels at the output. Also, this inverter has the modularity structure for packaging purpose. The other features include the simplest structure and easy control algorithm.

Each structure has its own distinct advantages and disadvantages. Among the three structures, the cascaded H-bridge inverter is most popular in industries because of its modular structure. The series connection of single-phase H-bridge topology have voltage rating of 13.8kV, 30MVA but it uses a number of semiconductor switches. On the other hand, the Flying Capacitor and Diode Clamped multilevel inverter uses lesser number of semiconductor switches to produce the same number of output levels as produced by equally structured cascaded H-bridge but they use a number of components except power semiconductor devices. The NPC multilevel inverter uses a number of diodes to clamp the voltage and FC multilevel inverter uses a number of capacitor in each phase.

III. MULTI-CARRIER PWM STRATEGY

As the various structures of multilevel inverter are proposed, simultaneously, profuse modulation techniques and control paradigms have been developed for the same such as SPWM, SHE-PWM (selective harmonic elimination), SVM (space vector modulation), etc.

This sinusoidal PWM strategy basically deals in generating gate pulses for the semiconductor switches by comparing a sine wave as the reference signal or wave with the triangular wave as the carrier signal or wave. The arrangement of carrier signals can be different and thus named accordingly which are described as follows [13] - [16]:

(a) Alternate Phase Opposition Disposition (APOD): The method having the adjacent two triangular carrier signals as their mirror image. These adjacent two carrier waves being displaced by 180°.

(b) Phase Opposition Disposition (POD): The method having the carrier signals above zero level are in phase whereas carrier signal below zero level are in opposite phase to the triangular signals above the zero level. It looks like a mirror image if zero level being considered as the mirror.

(c) Phase Disposition (PD): The method having the triangular carrier signals above zero level and triangular carrier signals below zero level are in phase but only the level is changed.

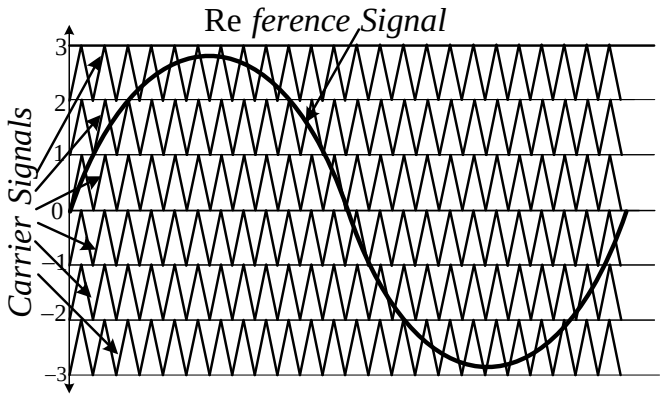


Fig. 4. PD-PWM topology arrangement for seven level inverter.

Single-phase 7-levels MLI require six triangular carriers wave and some rules that are applicable for all PWM strategy are: -

- Converter produces +3V, when the reference wave is higher than all three carriers above zero level.
- Converter produces +2V , when the reference wave is higher than second carrier above zero level.
- Converter produces +V, when the reference wave is higher than first carrier above zero level.
- Converter produces 0V, when the reference wave is higher than lower carrier and lower than higher carrier.
- Converter produces –V, when the reference wave is higher than first carrier below zero level.
- Converter produces -2V, when the reference wave is higher than second carrier below zero level.
- Converter produces -3V, when the reference wave is higher than all three carriers below zero level.

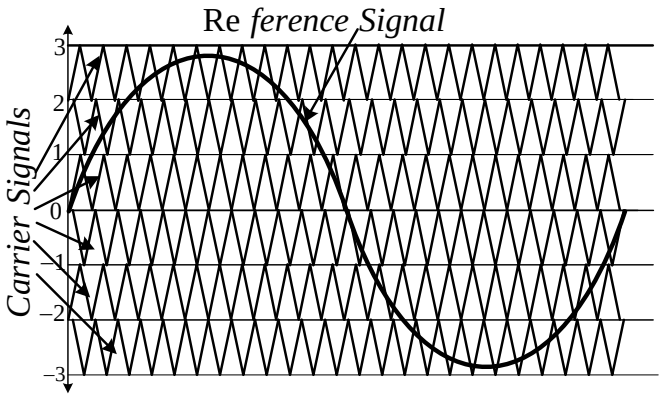


Fig. 5. APOD-PWM topology arrangement for seven level inverter.

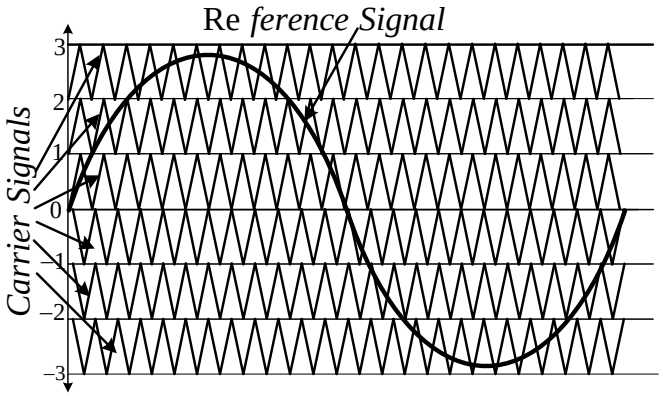


Fig. 6. POD-PWM topology arrangement for seven level inverter.

Seven level carrier arrangement of PD-PWM, POD-PWM, APOD-PWM topology have been shown in the Fig. 4, Fig. 5, Fig. 6 respectively. Similarly, all further more levels can be developed in same manner. Switching table for seven level inverter for NPC-MLI, FC-MLI, CHB-MLI is presented in Table.1, Table. 2, Table. 3 below respectively.

TABLE. 1. SWITCHING TABLE FOR SEVEN LEVEL NPC

V_{AN}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
3V	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
2V	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
V	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
0	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**
-V	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**
-2V	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
-3V	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**

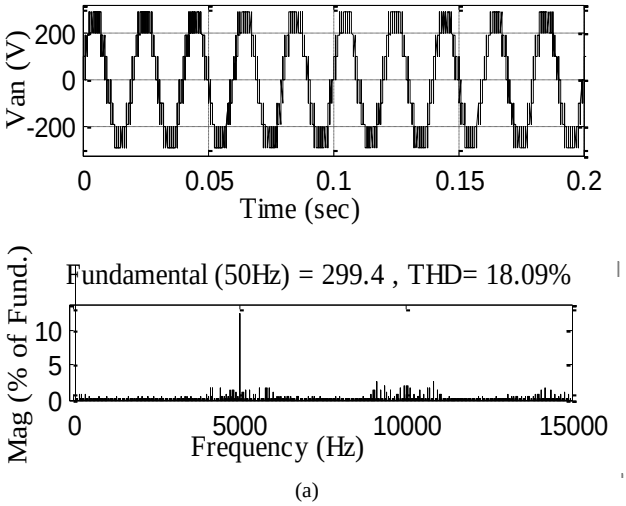
TABLE. 2. SWITCHING TABLE FOR SEVEN LEVEL FC

V_{AN}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
3V	1	1	1	1	1	1	0	0	0	0	0	0
2V	1	1	1	1	1	0	1	0	0	0	0	0
V	1	1	1	1	0	0	1	1	0	0	0	0
0	1	1	1	0	0	0	1	1	1	0	0	0
-V	1	1	0	0	0	0	1	1	1	1	0	0
-2V	1	0	0	0	0	0	1	1	1	1	1	0
-3V	0	0	0	0	0	0	1	1	1	1	1	1

TABLE. 3. SWITCHING TABLE FOR SEVEN LEVEL CHB

V_{AN}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
3V	1	0	0	1	1	0	0	1	1	0	0	1
2V	1	1	0	0	1	0	0	1	1	0	0	1
V	1	1	0	0	1	1	0	0	1	0	0	1
0	1	1	0	0	1	1	0	0	1	1	0	0
-V	0	1	1	0	1	1	0	0	1	1	0	0
-2V	0	1	1	0	0	1	1	0	1	1	0	0
-3V	0	1	1	0	0	1	1	0	0	1	1	0

IV. SIMULATION RESULTS



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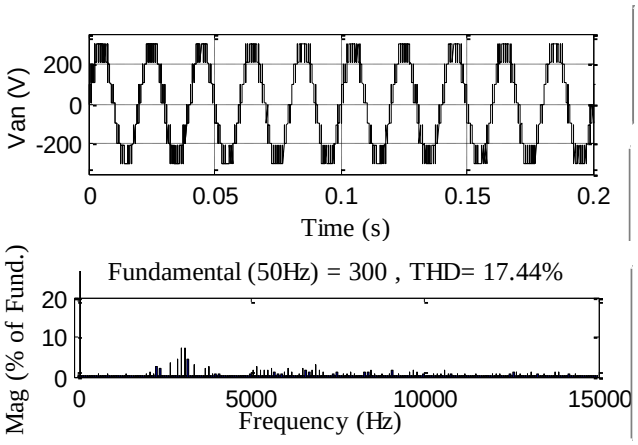

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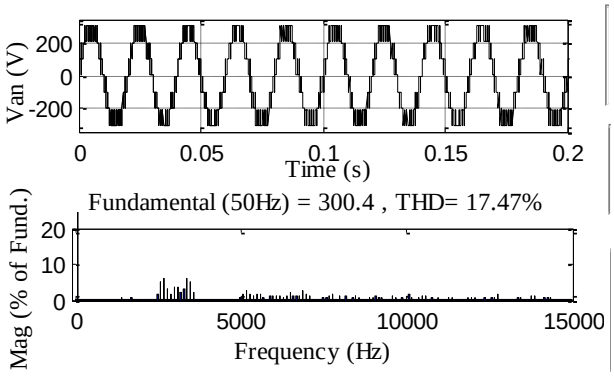
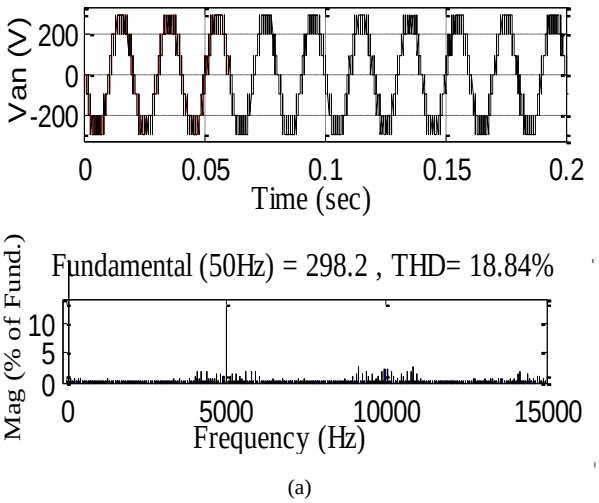


(c)

Fig. 7. Simulation results of phase output voltage with %THD for seven-level NPC-MLI (a) PD-PWM (b) POD-PWM (c) APOD-PWM.



(a)

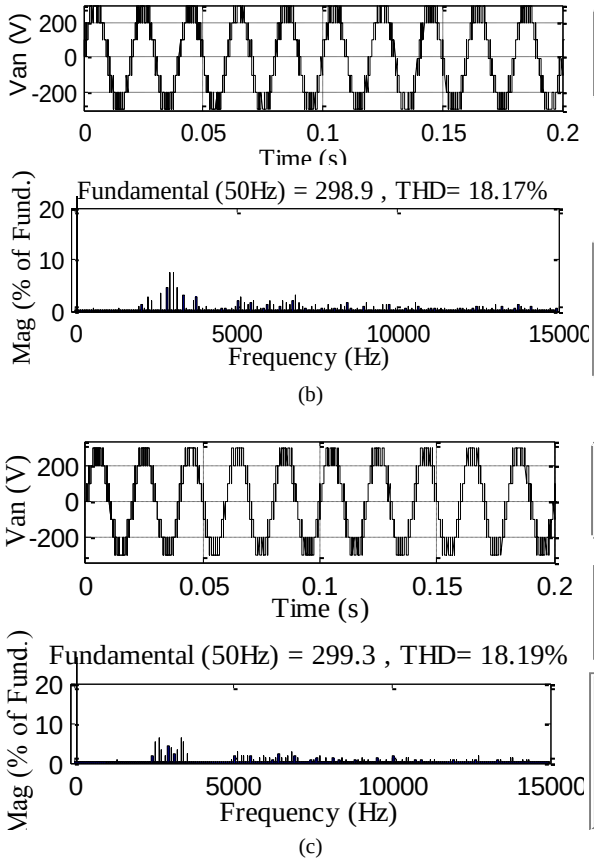
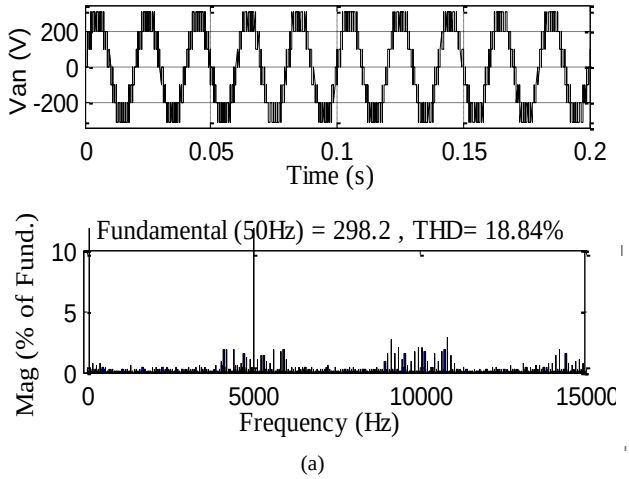


Fig. 8. Simulation results of phase output voltage with %THD for seven-level FC-MLI (a) PD-PWM (b) POD-PWM (c) APOD-PWM.



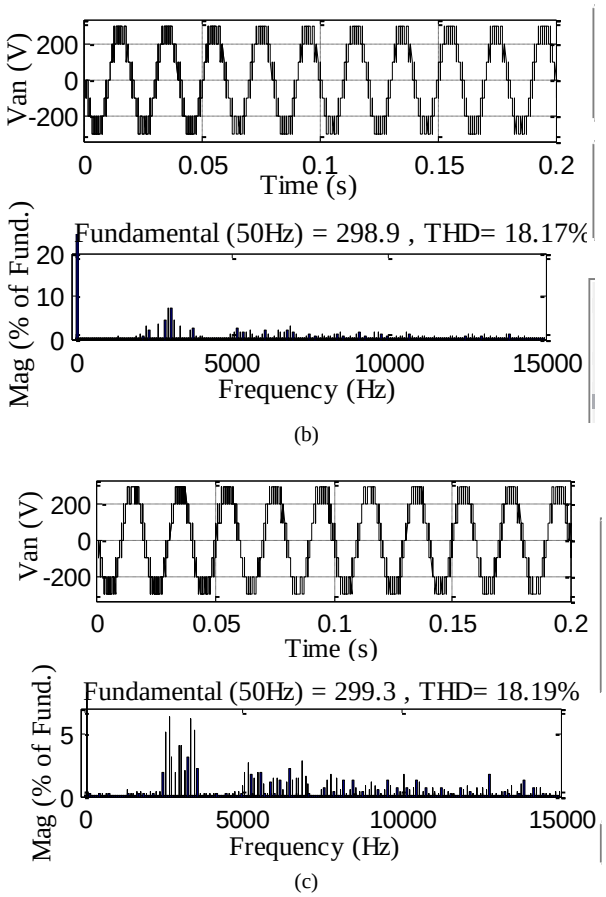


Fig. 9. Simulation results of phase output voltage with %THD for seven-level CHB-MLI (a) PD-PWM (b) POD-PWM (c) APOD-PWM.

Fig. 7 shows the simulation results of output voltage in per phase of seven level inverter neutral point clamped topology (NPC-MLI) for (a) PD-PWM (b) POD-PWM (c) APOD-PWM having total harmonic distortion in percent (%) of 18.09, 17.44, 17.47 respectively. Fig. 8 shows the simulation results of output voltage in per phase of seven level inverter Flying capacitor topology (FC-MLI) for (a) PD-PWM (b) POD-PWM (c) APOD-PWM having total harmonic distortion in percent (%) of 18.84, 18.17, 18.19 respectively. Fig. 9 shows the simulation results of output voltage in per phase basis of seven level cascaded H-bridge inverter (CHB-MLI) for (a) PD-PWM (b) POD-PWM (c) APOD-PWM having total harmonic distortion in percent (%) of 18.84, 18.17, 18.19 respectively. It has been noted that better %THD is noticed in all classical MLI topologies for POD-PWM technique compared to the PD-PWM and APOD-PWM techniques.

TABLE 4: COMPARISON TABLE FOR %THD IN SEVEN AND NINE LEVEL MLI FOR PD, POD, APOD PWM STRATEGIES

	%THD in Seven Level Inverter		
Topologies	NPC	FC	CHB
PD-PWM	18.09%	18.84%	18.84%
POD-PWM	17.44%	18.17%	18.17%
APOD-PWM	17.47%	18.19%	18.19%

TABLE 5: COMPARISON TABLE IN TERMS OF NO. OF SWITCHES, DC SOURCES AND DIODES IN SEVEN AND NINE LEVEL MLI FOR DIFFERENT TOPOLOGY.

	Seven Level Inverter		
Topologies	NPC	FC	CHB
No. Of Switches	36	36	36
DC Sources	6	51	9
Diodes	90	36	36

In Table. 4 comparison of % THD for seven level inverter on different PWM schemes have been presented. Table. 5 shows the comparison in terms of number of switches, number of DC sources, diodes for three classical configurations of multilevel inverters. It shows the data of 7^{th} level of phase output voltage and also can be generalized for n^{th} level. It has been noted that better %THD is noticed in all classical MLI topologies for POD-PWM technique compared to the PD-PWM and APOD-PWM techniques. Therefore, CHB-MLI found can be concluded as better topology for various applications like PV based grid applications, adjustable speed drive applications etc.

V. RESULTS AND DISCUSSION

This paper work includes the comparison of seven level three-phase multilevel inverter configurations of various types from various aspects at different PWM techniques. However, study of different PWM such as APOD (Alternate Phase Opposition Disposition), POD (Phase Opposition Disposition), PD (Phase Disposition) technique for seven level inverter has been done in MATLAB/SIMULINK environment. This study includes comparison of required least number of components to obtain same voltage levels and CHB-MLI is found to be appropriate among other configurations of MLI due to its modular structure, solution of voltage balancing, fault clearing ability for higher levels. Output voltage levels along with %THD has been shown and compared for seven level inverter with different PWM i.e. PD-PWM, POD-PWM, APOD-PWM.

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