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Comparative analysis of Cascaded H-Bridge Multilevel Inverters in Reducing Harmonic Distortion by EPPWM and PDPWM Techniques

Chaitra G D
Assistant Professor, Department of ECE,
Mysuru Royal Institute of Technology,
Mandya, Karnataka, India

Dr. Y L Chandrashekar
Professor, Department of ECE,
Mysuru Royal Institute of Technology,
Mandya, Karnataka, India

***Abstract*—Multilevel inverter (MLI) technologies are suitable for conversion in renewable sources and high-power industrial applications due to their many advantages such as low power dissipation on power switches, low harmonic contents, high power rating and high efficiency that can be achieved without using transformer. Multi-level inverter is a DC to AC power convertor which is implemented using power electronic semiconductor switches like IGBT or MOSFET. The proposed system uses Equal Phase (EP) and Sinusoidal pulse width modulation (SPWM) method for generating gating/firing signal in the multilevel inverter to convert DC voltage from battery storage to supply AC loads. In the EP method, the effectiveness of eliminating low-order harmonics in the inverter output voltage is studied and compared to that of the sinusoidal PWM method. In SPWM, Phase Disposition (PD) PWM method is used to control the output of multilevel inverter. The distortion of the output voltage decreases and rms output voltage increases as the number of level increases. This paper presents the simulation and comparative analysis of the single phase three, five, seven and eleven level inverters. All the topologies are modelled using MATLAB/Simulink and the results are validated and compared.**

Keywords—Multilevel inverter [MLI]; Equal Phase PWM [EPPWM]; Sinusoidal pulse width modulation [SPWM]; phase disposition PWM [PDPWM]; total harmonic distortion [THD].

I. INTRODUCTION

There have been major advancements in power electronics from the last few decades. Power electronics have moved along with these developments with such things as digital signal processors being used to control power systems. An Inverter is basically a converter that converts DC-AC power. Inverter circuits can be very complex, so the objective of this paper is to present some of the inner workings of inverters without getting lost in some of the fine details [1].

Inverters are power electronic circuits which can convert DC voltages to AC voltages. Inverters do not produce any power; they rather use power provided by DC source. The output waveforms are generally sine wave, square wave, or quasi square wave. Inverters are majorly classified as current source inverters (CSI) and voltage source inverters (VSI). Though both types of inverters can be used in every application where inverter is used but voltage source inverters are more widely used as compared to current source inverters.

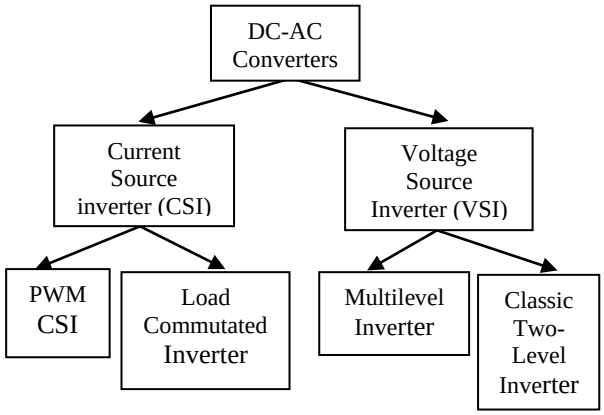

Fig. 1: Different Types of Inverters

VSI are further classified as two-level inverters and multilevel inverters (MLI). Classification of inverters is shown in fig 1.

Earlier conventional two-level inverters were used but these inverters suffered some serious disadvantage. To overcome these disadvantages multilevel inverters became more popular in industries than traditional two-level inverters.

The advantages of multilevel inverters over two level inverters are given as follows [2]

(i). Staircase Waveform in Output: A multilevel converter generates staircase waveform or quasi-square wave in the output. The total harmonic distortion (THD) generated by the staircase waveform is very low as compared to the THD present in the output of traditional two-level converters. Along with low THD, the staircase waveform can also reduce dv/dt stresses and as a result the problems of electromagnetic compatibility are also reduced.

(ii). Common Mode (CM) Voltage: The common mode voltages produced by multilevel converters is small and hence, stress on the bearing of the motor connected to a multilevel motor drive is also small. These common mode voltages can be eliminated by using advanced modulation strategies like, sinusoidal pulse width modulation (SPWM).

(iii). Input Current: The input current drawn by a multilevel converter has low distortion.

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(iv). Switching Frequency: The operation of a multilevel converter is possible for both fundamental switching frequency and high switching frequency PWM. Hence, by operating at lower switching frequency, the switching losses can be reduced, and the efficiency of the system can be increased.

II. TOPOLOGIES OF MULTILEVEL INVERTERS

In past few years a number of multilevel inverter topologies were introduced in industries but three of these topologies which are famously called classical topologies are more common in industry. These are:

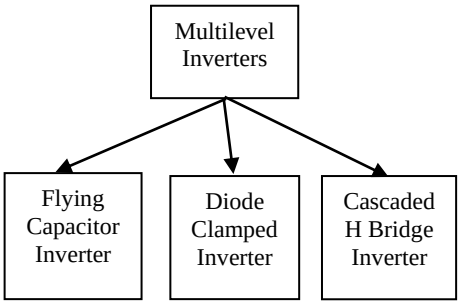

Fig. 2: Topologies of Multilevel Converters

The cascaded H-Bridge multilevel inverters are the most advanced and important method of power electronic converters that analyses output voltage with number of dc sources as inputs. As compared to diode clamped inverter and flying capacitor inverter, the cascaded H-Bridge multilevel inverters require less number of components and it reaches high quality output voltage which is close to sine wave. By increasing the number of output levels, the total harmonic distortion in output voltage can be reduced. In cascaded H-Bridge multilevel inverter required AC output voltage is obtain by synthesizing number of DC sources. The number of H-Bridge units with different DC sources is connected in series or cascade to produce cascaded H-Bridge multilevel inverter. In our work, we are using Cascaded H Bridge Inverter.

III. ADVANTAGES OF CASCADED H-BRIDGE MULTILEVEL CONVERTERS

1. The total number of output voltage levels is more than twice to that of number of DC sources available.
2. The use of separate DC sources provides isolation of between sources of each module.
3. Since the outputs of all the modules gets added so voltage rating of individual module is low and hence stress on individual devices also gets reduced.
4. The series of H-Bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.
5. The topology due to its modularized structure is highly flexible and hence more convenient to reconfigure in case of occurrence of fault.

IV. APPLICATION AREAS OF CASCADED H-BRIDGE MULTILEVEL CONVERTERS

1. Static VAR generation.
2. Interfacing renewable energy sources with grid.
3. They can be used in battery-based system.
4. They are also proposed to be used as main traction drive in electric vehicles where several batteries and ultra-capacitors are being used and are well suited to behave as SDCS.
5. Active filters
6. Back-to-Back frequency link systems.

V. DEVELOPMENT AND SIMULATION OF MLI

In this paper, MLI model is developed using multi-carrier PWM (PD method is used) and Equi-phase PWM.

A. Multi-Carrier PWM Strategy

As the various structures of multilevel inverter are proposed, simultaneously, profuse modulation techniques and control paradigms have been developed for the same such as SPWM, SHE-PWM (selective harmonic elimination), SVM (space vector modulation), etc.

This sinusoidal PWM strategy basically deals in generating gate pulses for the semiconductor switches by comparing a sine wave as the reference signal or wave with the triangular wave as the carrier signal or wave. The arrangement of carrier signals can be different and thus named accordingly which are described as follows [4]:

(a) Phase Disposition (PD): The method having the triangular carrier signals above zero level and triangular carrier signals below zero level are in phase but only the level is changed. In phase disposition strategy, all the carriers have the similar frequency and amplitude furthermore all the carriers are in phase with each other. Carrier disposition triangular signals are used in comparison with sinusoidal reference to generate Sine PWM switching sequence.

(b) Phase Opposition Disposition (POD): The method having the carrier signals above zero level are in phase whereas carrier signal below zero level are in opposite phase to the triangular signals above the zero level. It looks like a mirror image if zero level being considered as the mirror.

(c) Alternate Phase Opposition Disposition (APOD): The method having the adjacent two triangular carrier signals as their mirror image. These adjacent two carrier waves being displaced by 180°.

The SPWM technique to generate gate signal for switches in H bridge to work in Phase Disposition method and the corresponding waveforms for five level inverter shown in fig below.

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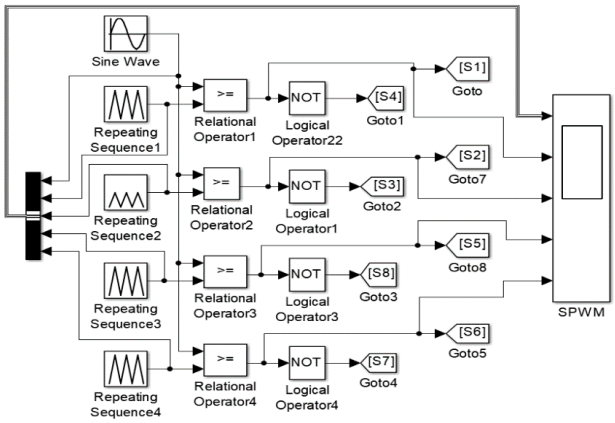

Fig 3: Generation of multi-carrier signal (SPWM) (Five level)

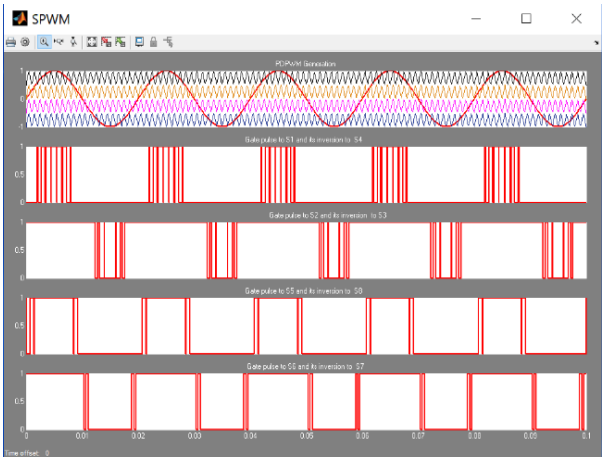

Fig 4: waveforms of SPWM (five level)

B. Equal Phase (EP) PWM Strategy

Methods to calculate switching angle for cascade H-bridge inverters. There are following four methods [5]:

1. Equal Phase (EP)
2. Half Equal Phase (HEP)
3. Half Height (HH)
4. Feed Forward (FF) Method.

We are discussing only Equal phase method in this paper.

In the equal phase method, the switching angles are distributed averagely in the range 0-Π. The main switching angles are obtained by the formula given below: α_i = (i * 180)/m where i=1, 2, 3, ……. (m-1) /2.

Switching Angle

Switching angle is the moment of the voltage level change at the output. For an m-level waveform, there are 2(m-1) switching angles are needed. We call them as α_1, α_2, α_3, ……. α_{m-2}, α_{m-1}. The number of bridges(n) in the inverter is calculated using, n = (m-1)/2, where m is the number of output voltage levels in the inverter and the number of switching elements (i.e., switches) are equal to (n x 4). The switching pattern of five level inverter is shown below.

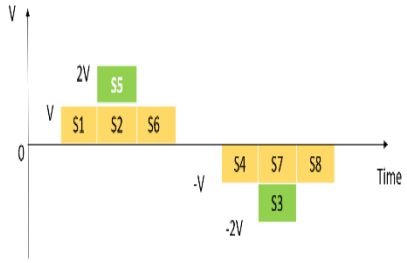

Fig 5: Switching pattern of five level Inverter using EP-PWM

VI. EXPERIMENTATION

The Simulation model of three, five, seven and eleven level inverters are explained below.

A. Three level inverter with EP and PD method

Figure 6 shows a three-level cascaded H-bridge multilevel inverter. The converter consists of single H-bridge cell which is fed by independent voltage source. There are three level of output voltage i.e +V, 0, -V. The circuit remains the same except the application of gate signal.

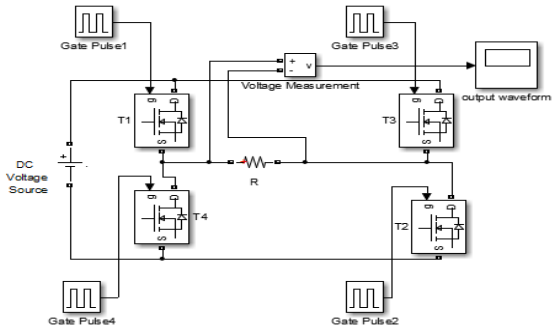

Fig 6: Simulation model of three level inverter

B. Five level inverter with EP and PD method

Figure 7 shows a five-level cascaded H-bridge multilevel inverter. The converter consists of two series connected H-bridge cells which are fed by independent voltage sources. The outputs of the H-bridge cells are connected in series such that the synthesized voltage waveform is the sum of all of the individual cell outputs. The output voltage is given by V=V1 +V2 Where the output voltage of the first cell is labelled V1 and the output voltage of the second cell is denoted by V2. There are five level of output voltage i.e 2V, V, 0, -V, -2V.

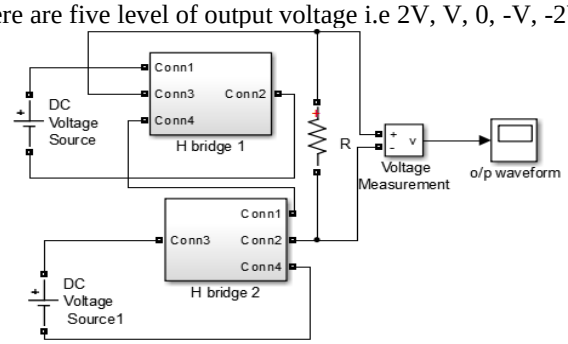

Fig 7: Simulation model of Five level inverter

C. Seven level inverter with EP and PD method

Figure 8 shows a seven-level cascaded H-bridge multilevel inverter. The converter consists of three series connected H-

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bridge cells which are fed by independent voltage sources. The outputs of the H-bridge cells are connected in series such that the synthesized voltage waveform is the sum of all of the individual cell outputs. The output voltage is given by V=V1 +V2+V3, Where the output voltage of the first cell, second cell and the third cell are labelled by V1, V2 and V3. There are Seven level of output voltage i.e 3V, 2V, V, 0, -V, -2V, -3V.

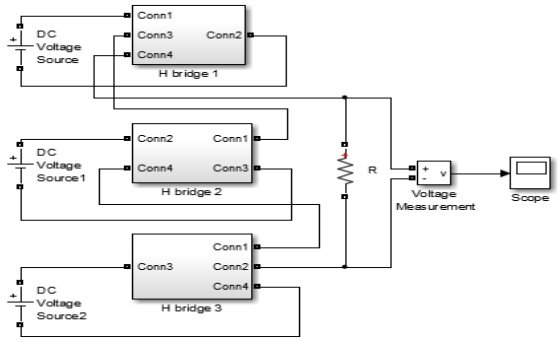

Fig 8: Simulation model of seven level inverter

D. Eleven level inverter with EP and PD method

Figure 9 shows a Eleven level cascaded H-bridge multilevel inverter. The converter consists of Five series connected H-bridge cells which are fed by independent voltage sources. The outputs of the H-bridge cells are connected in series such that the synthesized voltage waveform is the sum of all of the individual cell outputs. The output voltage is given by V=V1 +V2+V3+V4+V5, Where the output voltage of the first cell, second cell, third cell, fourth cell and fifth cell are labelled by V1, V2, V3, V4 and V5. There are eleven level of output voltage i.e 5V, 4V, 3V, 2V, V, 0, -V, -2V, -3V, -4V, -5V.

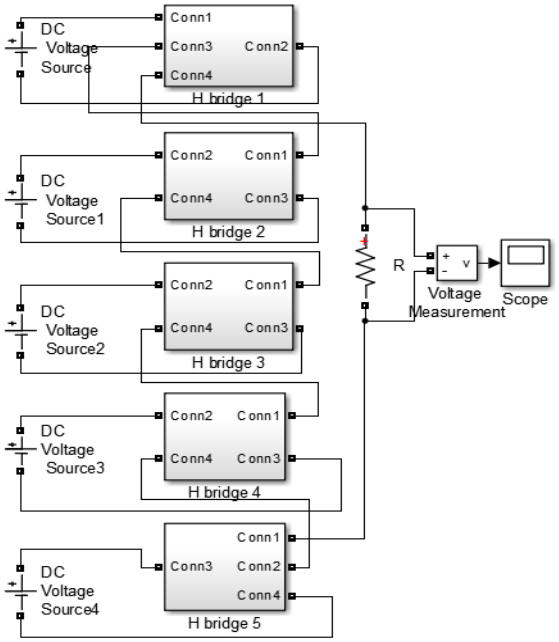

Fig 9: Simulation model of eleven level inverter

VII. RESULTS AND DISCUSSION

The multi-carrier (PD)PWM and EP PWM are applied to single phase three, five, seven and eleven level inverters. The respective gate pulses generated, THD waveforms and output voltage waveforms generated from both the methods for three, five, seven and eleven level inverters are shown in the figures below

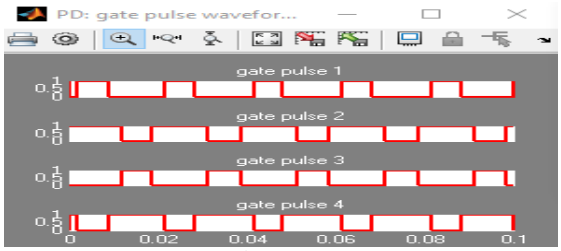

Fig 10(a1): Gate pulse for three level inverter: EPPWM

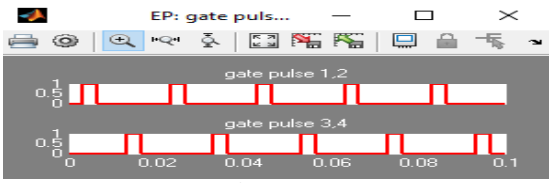

Fig 10(a2): Gate pulse for three level inverter: PDPWM

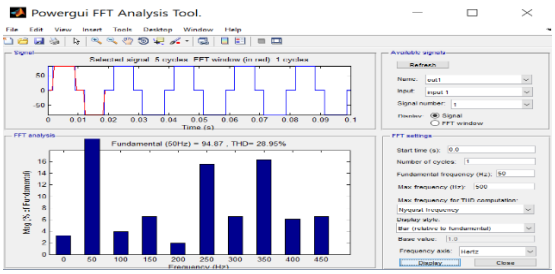

Fig 10(b1): THD waveforms of three level inverter: EPPWM

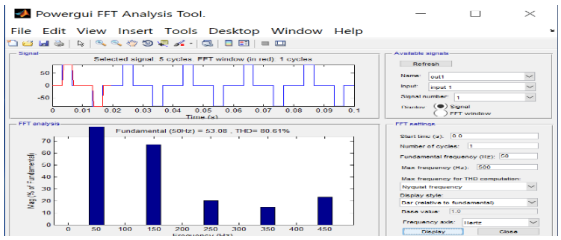

Fig 10(b2): THD waveforms of three level inverter: PDPWM

Fig 10(c): Three level Output waveform

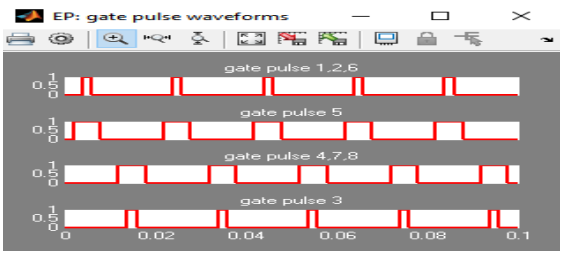

Fig 11(a1): Gate pulse for five level inverter: EPPWM

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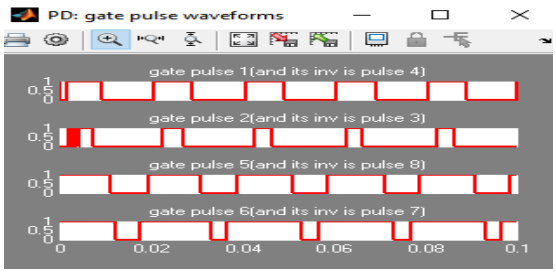

Fig 11(a2): Gate pulse for five level inverter: PDPWM

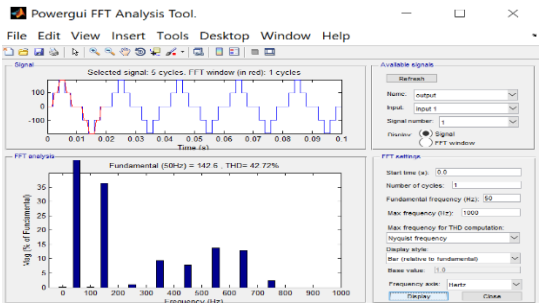

Fig 11(b1): THD waveforms of five level inverter: EPPWM

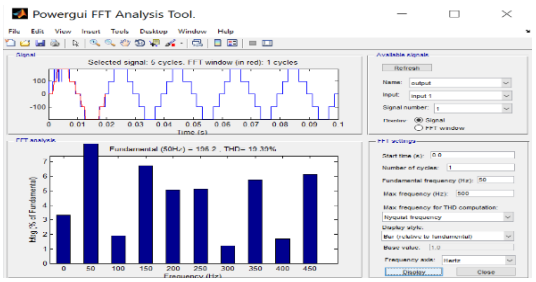

Fig 11(b2): THD waveforms of five level inverter: PDPWM

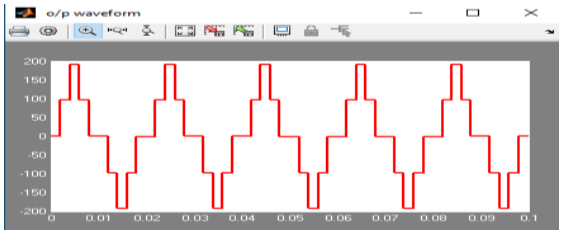

Fig 11(c): Five level Output waveform

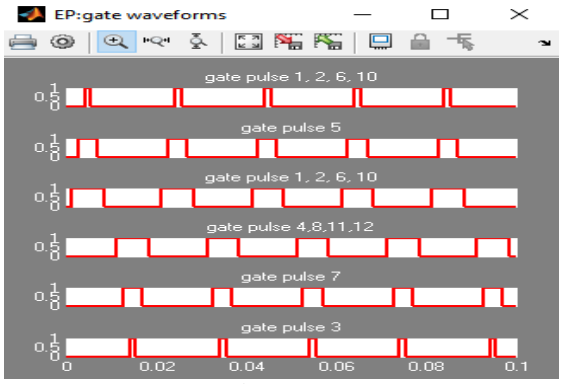

Fig 12(a1): Gate pulse for seven level inverter: EPPWM

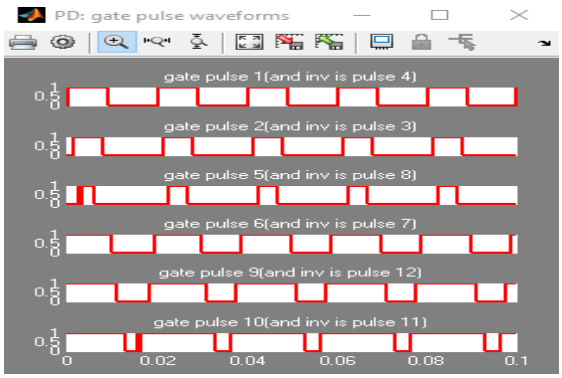

Fig 12(a2): Gate pulse for seven level inverter: PDPWM

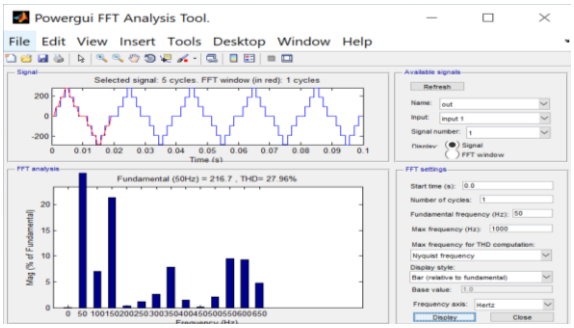

Fig 12(b1): THD waveforms of seven level inverter: EPPWM

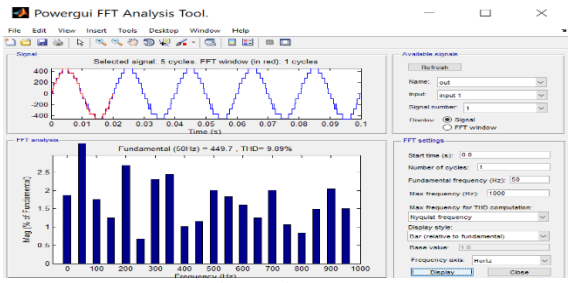

Fig 12(b2): THD waveforms of seven level inverter: PDPWM

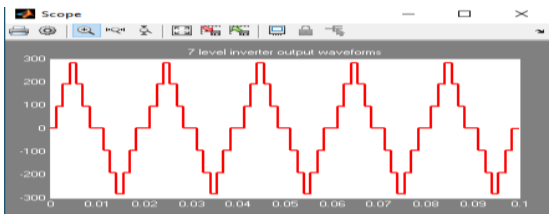

Fig 12(c): Seven level Output waveform

Fig 13(a1): Gate pulse for eleven level inverter: EPPWM

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Fig 13(a2): Gate pulse for eleven level inverter: PDPWM

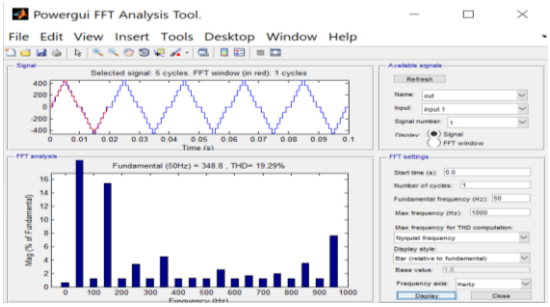

Fig 13(b1): THD waveforms of eleven level inverter: EPPWM

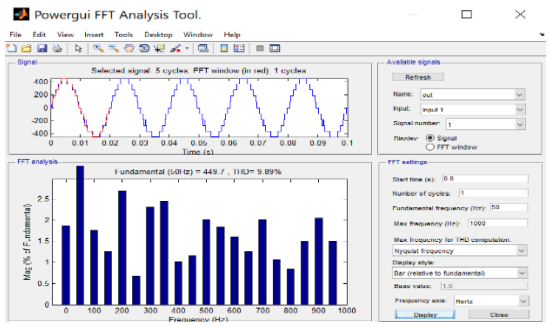

Fig 13(b2): THD waveforms of eleven level inverter: PDPWM

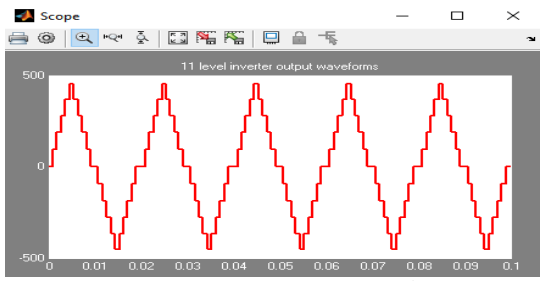

Fig 13(c): Eleven level Output waveform

Comparison table and graph for EP method

The comparison table for percentage of THD and RMS output voltage is shown below in table 1 for EPPWM and PDPWM.

Table1: Comparison of 3,5,7,11 level inverter of EPPWM and PDPWM methods for THD and RMS output voltage

Level of inverter	EPPWM		PDPWM	
	% of THD	RMS output Voltage	% of THD	RMS output Voltage
3	80.61	52.6	28.95	71.66
5	42.72	112.4	19.39	137.3
7	27.96	165.6	16.43	214.7
11	19.89	269.1	9.89	338.1

Also, the graph in figure 14 and 15 shows that for EPPWM MLI, as the number of levels of inverter output increases, the THD decreases, and RMS output voltage increases, respectively.

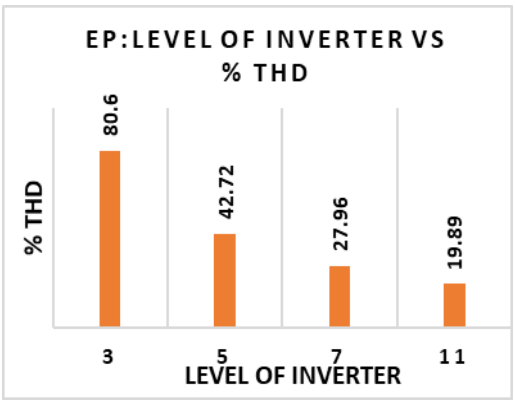

Fig 14: Graph of level of inverter vs %THD for EPPWM

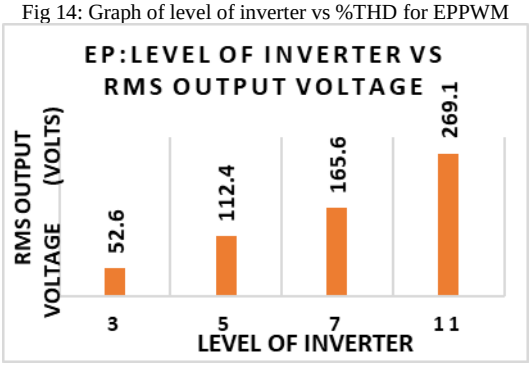

Fig 15: Graph of level of inverter vs RMS output voltage for EPPWM

Also, the graph in figure 16 and 17 shows that for PDPWM MLI, as the number of levels of inverter output increases, the THD decreases, and RMS output voltage increases, respectively and its greater than EPPWM inverters.

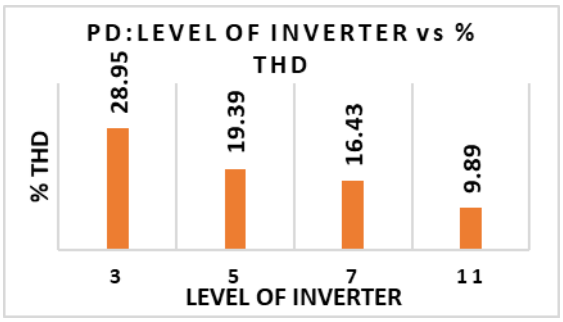

Fig 16: Graph of level of inverter vs %THD for PDPWM

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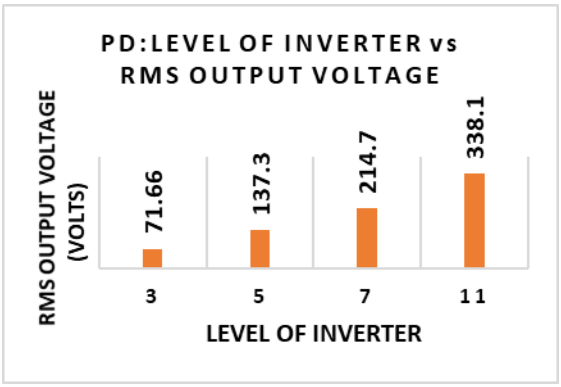

Fig 17: Graph of level of inverter vs RMS output voltage for PDPWM

From table 1, it has been observed that the % of THD obtained is less in Phase Disposition (PD) PWM compared to Equi-phase (EP) PWM. Also, the RMS output voltage is more in PDPWM compared to EPPWM.

VIII. CONCLUSION

The simulation of three, five, seven and eleven level inverters are carried out in MATLAB/SIMILINK where a simple control strategy is applied for switching the switches using EP-PWM and SPWM-PDPWM methods. The total harmonic distortion and rms output voltage for each level for both the methods are calculated and compared for resistive load. From the different levels of simulation, it is observed that THD can be decreased from 80.61 % to 19.89 % by increasing number of levels in EPPWM and THD is even lesser in eleven level of PDPWM method i e., 9.89 %. The rms output voltage is increased by increasing number of levels from 52.6V to 269.1V in EPPWM and it has been observed that it is highest in eleven level inverter with PDPWM i.e., 338.1V technique.

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