

Comparative Analysis of 8-bit Adders for Embedded Application

¹Kunjan D. Shinde

²nd Year, M.Tech. in Digital Electronics,
Dept. of Electronics & Communication Engineering
SDMCET, Dharwad - 02
Karnataka, INDIA
Kunjan18m@gmail.com

²Jayashree C. Nidagundi

Assistant Professor
Dept. of Electronics & Communication Engineering
SDMCET, Dharwad - 02
Karnataka, INDIA
jayaprajwal@rediffmail.com

Abstract— Digital computations and processing is involved in each and every embedded and non-embedded device, such applications and devices has arithmetic logic unit, adders are most important and essential block of these system, design and selection of adders plays a very important role, this paper presents a comparative study of five different adders like Ripple Carry Adder, Carry Skip Adder, Carry Lookahead Adder, Kogge Stone Adder, with performance metrics as delay and area. From the results it is clear that Kogge Stone Adder provides a less delay with a compromise in area.

Keywords— Ripple Carry Adder, Carry Skip Adder, Carry Lookahead Adder, Kogge Stone Adder, Delay, No. of slices, No. of LUTs.

I. INTRODUCTION

Adders are fundamental and most essential blocks in every digital system, design of effective and reliable adders plays a important role[1], as the technology is scaled down the complexity in the design increases with some reduction is the performance of the adders, in this paper a different set of adders like Ripple Carry Adder, Carry Skip Adder, Carry Lookahead Adder, Kogge Stone Adder are designed using Verilog coding and the performance of the adders are tabulated,

A simple adder performs the addition of given two numbers and the result is sum of those two numbers. Adders can be implemented in different ways using different technologies at different levels of architectures. [2] Design of high speed and reliable adders is the prime objective and requirement for embedded applications as the technology is scaled down. Binary addition is a fundamental operation in most digital circuits. There are a variety of adders, each has certain performance. Adder is selected depending on where the adder is to be used.

Ripple Carry Adder (RCA)

A combinational circuit that adds two bits is called a half adder, A combinational circuit that adds two bits along with the carry generated/ carry in bit is called as full adder. The ripple carry adder is constructed by cascading full adder blocks in series, Fig-1.a. and Fig. 1.b. shows the block

diagram and gate level schematic of 1-bit full adder. To obtain the 8-bit Ripple Carry Adder it requires 8 stages of 1-bit full adders, the carryout of one stage is fed directly to the carry-in of the next stage which is shown in Fig. 2. For an n-bit parallel adder, it requires n full adder[2][5].

Drawbacks of Ripple Carry Adder

- ✓ Not very efficient when large bit numbers are used
- ✓ Delay increases linearly with the bit length

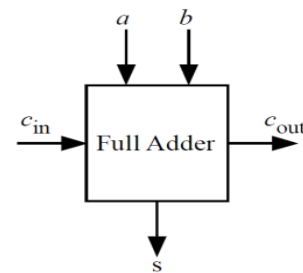


Figure 1.a. Block Diagram of 1-bit full adder

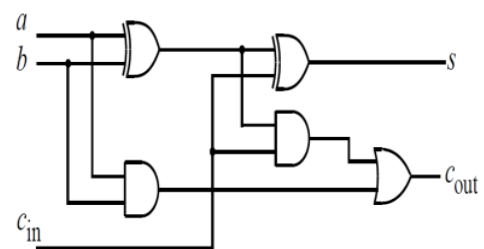


Figure 1.b. Schematic of 1-bit Full Adder

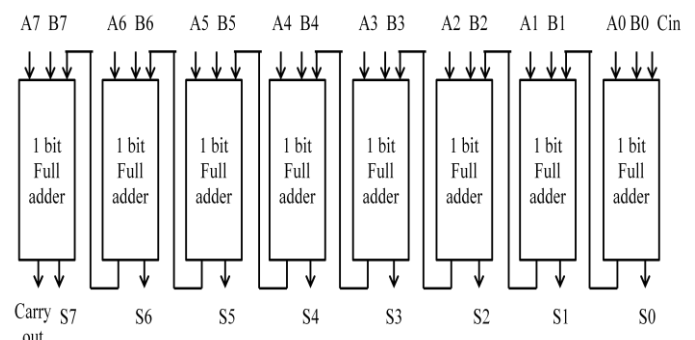


Figure 2. Block Diagram of Ripple Carry Adder

Equation of Ripple Carry Adder

$$S_i = A_i \text{ XOR } B_i \quad (1)$$

The worst case of delay might happen when the inputs at 1st stage are at logic '1' and/or any one of the input is at logic '1' and at this time the carry in is also at logic '1', at this state the carry propagated is carried out till the last stage and the delay in generating proper result is large and hence it the largest carry propagation path that can occur in the RCA.

CARRY SKIP ADDER (CSA)

The design of a carry-skip adder is based on the classical definition propagate signals as follows

$$P_i = A_i \text{ XOR } B_i \quad (2)$$

where P_i is the propagate signal and A_i and B_i are the input operands to the i th adder cell, C_i is the carry input to the i th cell. The carry out from the i th adder cell is expressed as

$$C_{i+1} = (A_i \text{ AND } B_i) \text{ OR } (P_i \text{ AND } C_i) \quad (3)$$

Figure 3 shows the block diagram of 8-bit Carry Skip Adder, the block diagram is obtained from the equations mentioned above

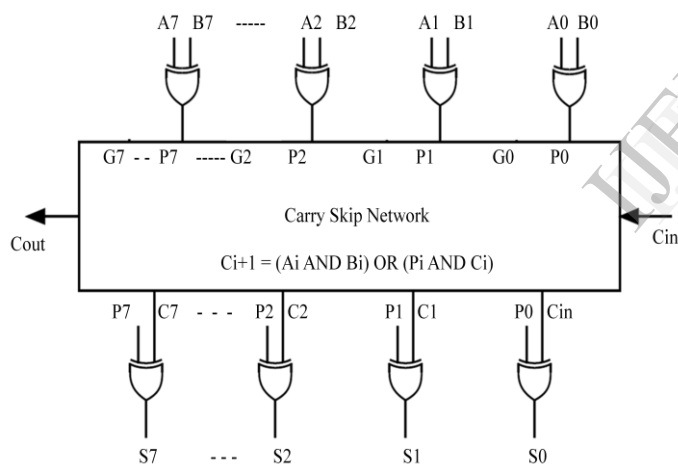


Figure 3. Block Diagram of Carry Skip Adder

It is stated that Carry Skip Adder provides better results in generating carryout signal when compared with Ripple Carry Adder, where as the area occupied is larger than that of Ripple Carry Adder.

CARRY LOOKAHEAD ADDER (CLA)

The carry lookahead adder (CLA) solves the carry delay problem by calculating the carry signals in advance based on the input signals. It is based on the fact that a carry signal will be generated in two cases: (1) when both bits are 1, or (2) when one of the two bits is high and the carry-in is high.[3][5]

Equations of Carry Lookahead Adder

$$P_i = A_i \text{ OR } B_i \quad (4)$$

$$G_i = A_i \text{ AND } B_i \quad (5)$$

$$S_i = A_i \text{ XOR } B_i \text{ XOR } C_i \quad (6)$$

$$C_{i+1} = G_i \text{ OR } (P_i \text{ AND } C_i) \quad (7)$$

Where P_i is propagate Signal and G_i is generate signal and S_i is the final sum output. The carry out of i th adder is obtained by equation (7). [3]

The above two equations can be written in terms of two new signals and which are shown in Figure 4:

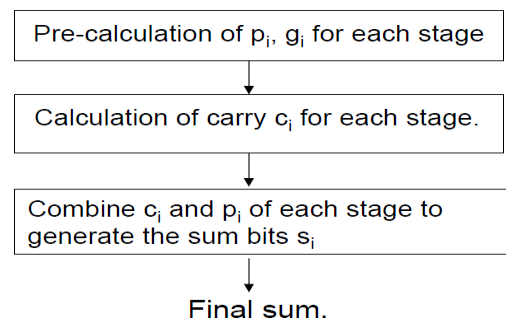


Figure 4. Processing Stages of Carry Lookahead Adder[5]

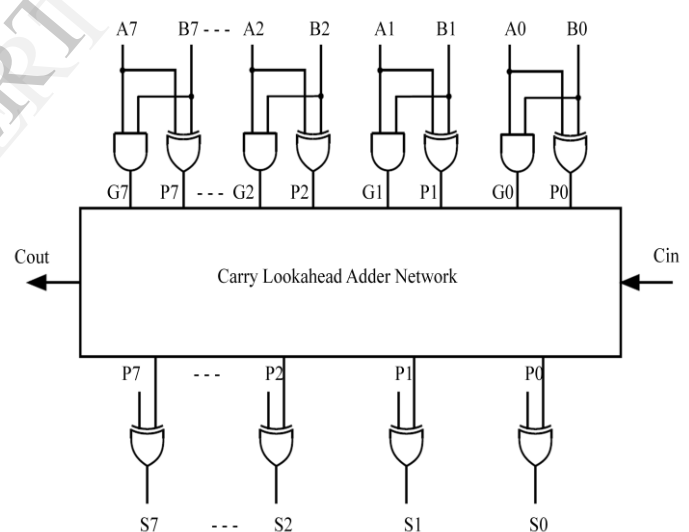


Figure 5. Block Diagram of Carry Lookahead Adder

KOGGE STONE ADDER

KSA is a parallel prefix form carry look ahead adder [1] It generates carry in $O(\log n)$ time and is widely considered as the fastest adder and is widely used in the industry for high performance arithmetic circuits. [1] In KSA, carries are computed fast by computing them in parallel at the cost of increased area. [1]

- ✓ Prefix: The outcome of the operation depends on the initial inputs.
- ✓ Parallel: Involves the execution of an operation in parallel. This is done by segmentation into smaller pieces that are computed in parallel

[5],[6]As mentioned earlier the Kogge Stone Adder is a parallel prefix form of Carry Look ahead Adder and the figure 4 shows the processing stages of Carry Look ahead adder and its equation for implementing/designing the same

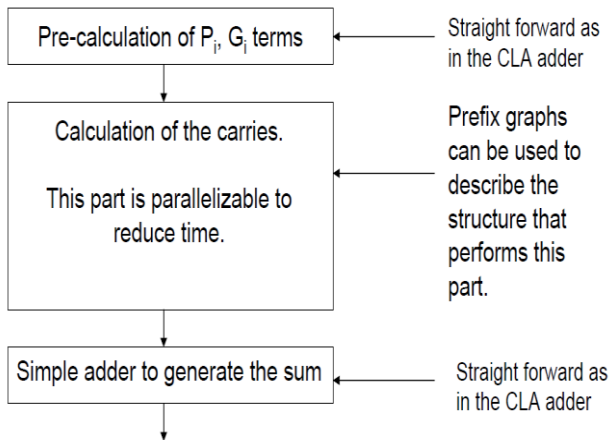


Figure 6. Parallel Prefix Adder stages[4]

The complete functioning of KSA can be easily comprehended by analyzing it in terms of three distinct parts [4][7][8]:

1. Pre processing

$$P_i = A_i \text{ XOR } B_i \quad (8)$$

$$G_i = A_i \text{ AND } B_i \quad (9)$$

2. Carry look ahead network

$$P_{i:j} = P_{i:k+1} \text{ AND } P_{k:j} \quad (10)$$

$$G_{i:j} = G_{i:k+1} \text{ OR } (P_{i:k+1} \text{ AND } G_{k:j}) \quad (11)$$

3. Post processing

$$S_i = p_i \text{ XOR } C_{i-1} \quad (12)$$

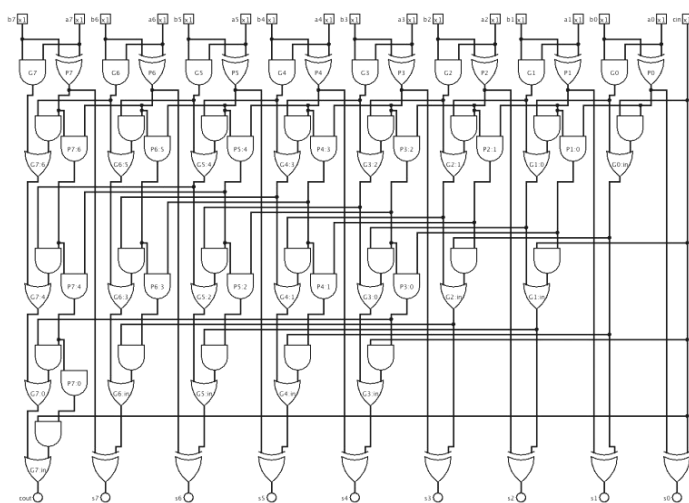


Figure 7. Schematic of 8 bit Kogge Stone Adder

RESULTS AND DISCUSSIONS.

Figure 8. shows the simulation results for all the adders give same inputs to every adder & the result of which is also the same and hence verifying the functionality of the adders mentioned above in this paper.

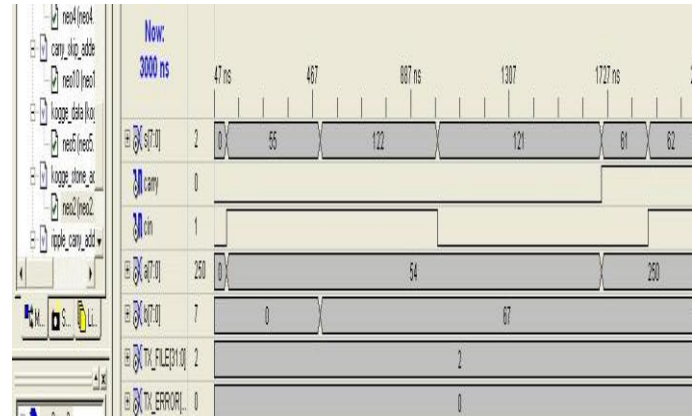


Figure 8. Simulation results of all the Adders for a common set of inputs.

Table 1 and 2 gives the comparative performance analysis of various adders mentioned above and speed is one of the criteria for the selection of embedded product for which Kogge Stone Adder provides the better results compared to other adders with compromise in the area. (KSA has a bit more area compared to other adders)

Table 1. Comparative Performance Analysis of Different Adders

Performance Metrics	No. of Slices	No. of 4 input LUTs	No. of Bounded IOBs	Delay	Macro statistics
Ripple Carry Adder (Data flow)	10/768	17/1536	26/98	17.102ns	1-bit Xor3-08
Ripple Carry Adder (structural)	10/768	17/1536	26/98	17.102ns	1-bit Xor3-08
Carry Skip Adder (Data flow)	10/768	17/1536	26/98	16.941ns	1-bit Xor - 13
Carry Skip Adder (Structural)	10/768	17/1536	26/98	16.941ns	1-bit Xor - 16
Carry Lookahead Adder(Data flow)	09/768	15/1536	26/98	15.858ns	1-bit Xor2-15
Kogge Stone Adder (Data flow)	20/768	34/1536	26/98	17.065ns	1-bit Xor2-16
Kogge Stone Adder (Structural)	20/768	34/1536	26/98	15.776ns	1-bit Xor2-16

Table 2. Comparative analysis of different adders with performance measure as delay

	Delay		
	Logic Delay	Route Delay	Total Delay
Ripple Carry Adder (Data flow)	09.456 ns	07.424 ns	16.880 ns
Ripple Carry Adder(structural)	09.456 ns	07.646 ns	17.102 ns
Carry Skip Adder(Data flow)	09.456 ns	07.485 ns	16.941 ns
Carry Skip Adder(Structural)	09.456 ns	07.485 ns	16.941 ns
Carry Lookahead Adder(Data flow)	08.977 ns	06.881 ns	15.858ns
Kogge Stone Adder(Data flow)	09.456 ns	07.609 ns	17.065 ns
Kogge Stone Adder(Structural)	08.977ns	06.799 ns	15.776 ns

Figures from Fig. 9 to Fig. 15 give the Top Level Schematic Implementation result of various adders mentioned above.

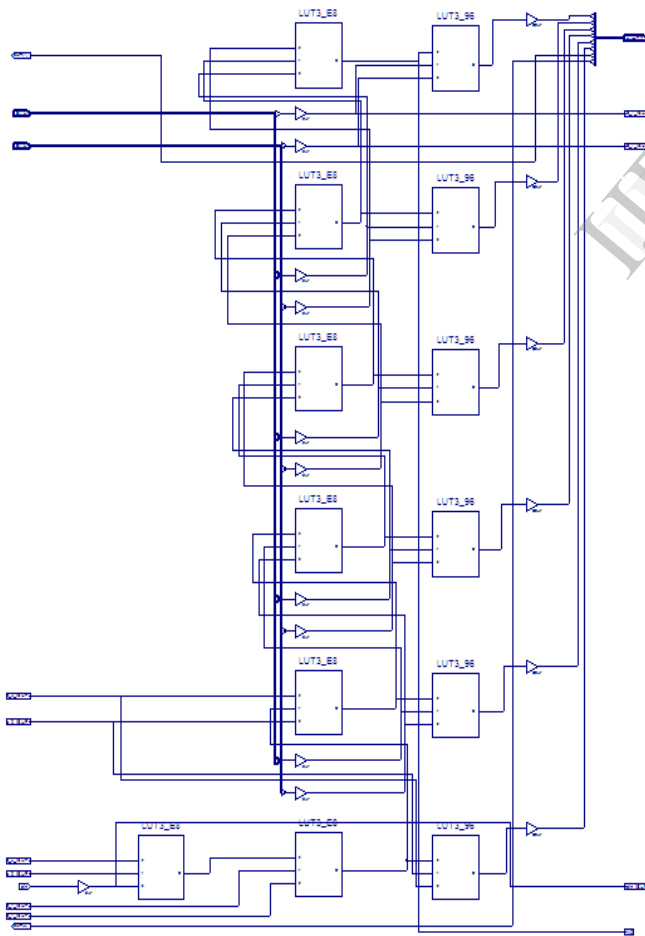


Figure 9. Technology Schematic of Ripple Carry Adder (Data Flow Modeling)

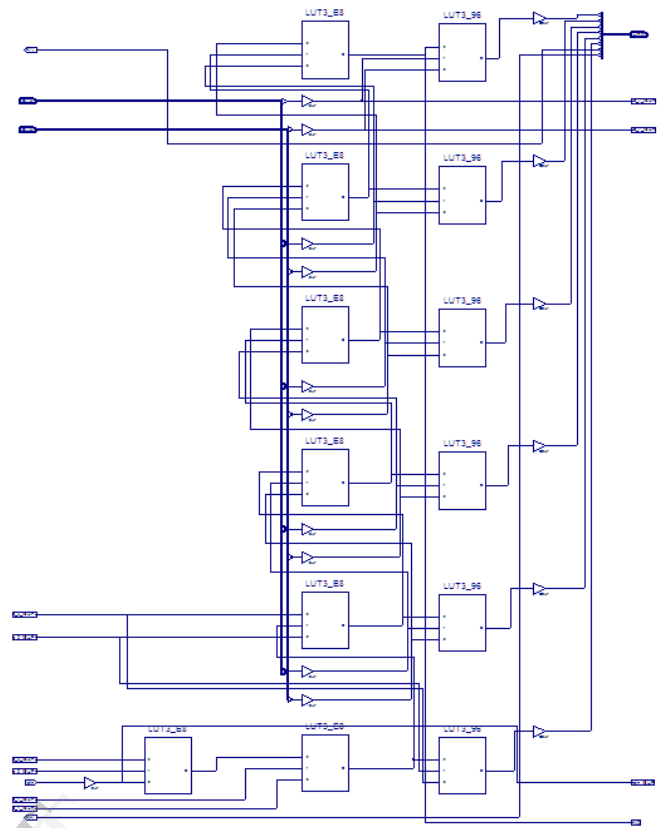


Figure 10. Technology Schematic of Ripple Carry Adder (Structural Modeling)

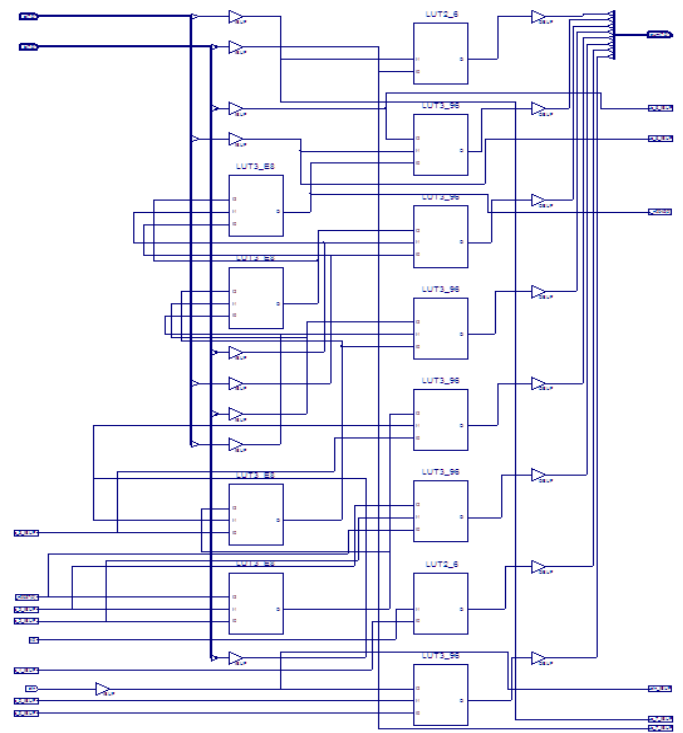


Figure 11. Technology Schematic of Carry Skip Adder (Data Flow Modeling)

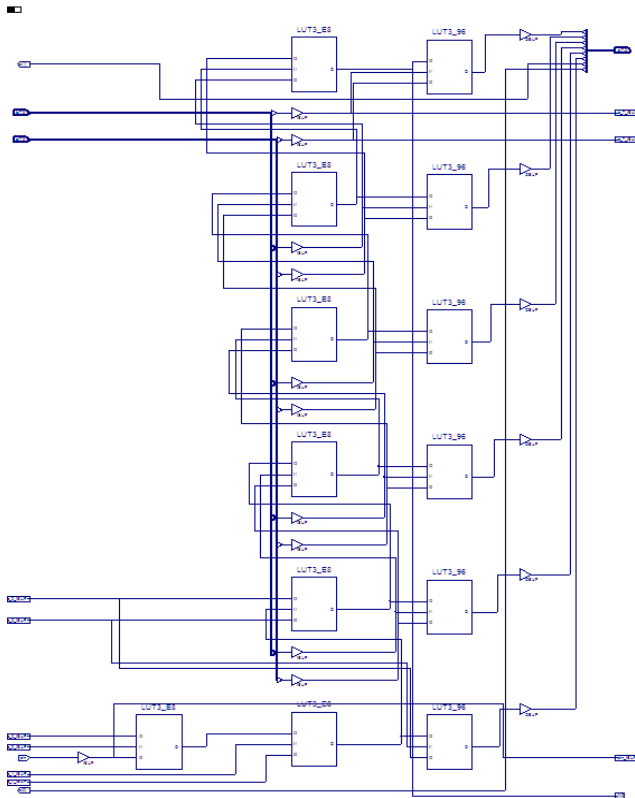


Figure 12. Technology Schematic of Carry Skip Adder (Structural Modeling)

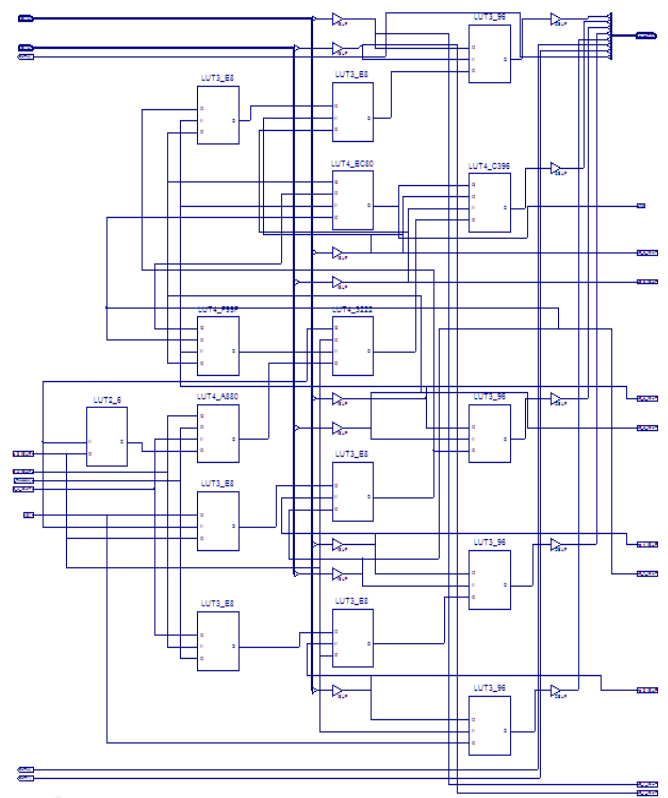


Figure 14. Technology Schematic of Kogge Stone Adder
(Data Flow Modeling)

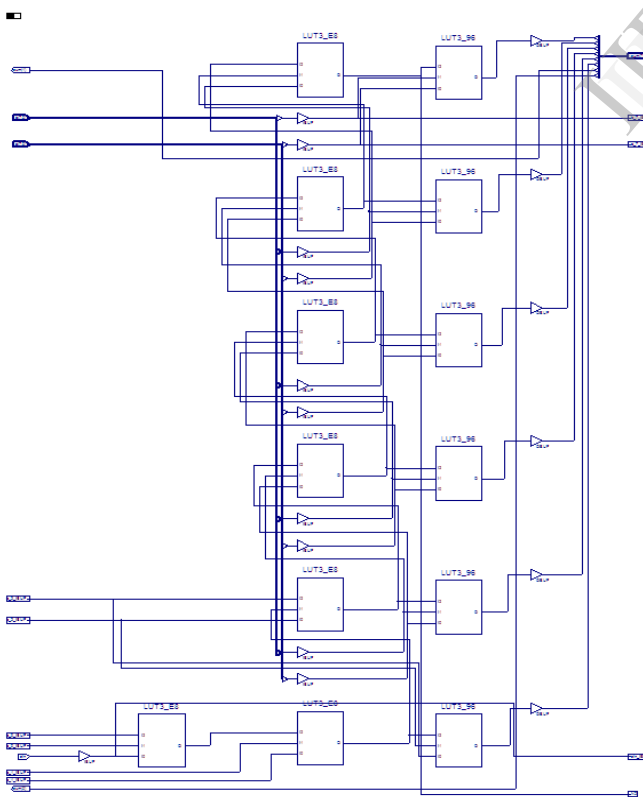


Figure13.Technology Schematic of Carry Lookahead Adder (Data Flow Modeling)

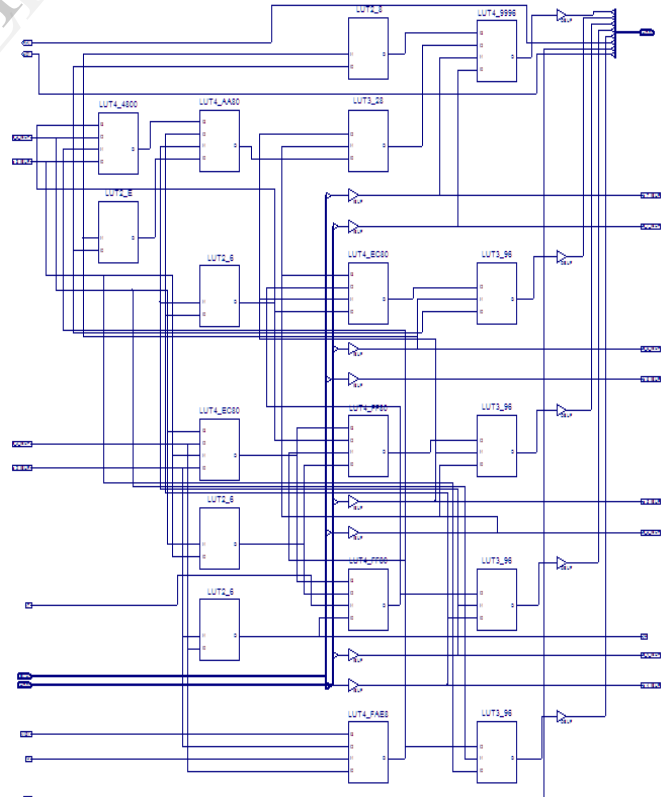


Figure 15. Technology Schematic of Kogge Stone Adder (Structural Modeling)

CONCLUSION

From the simulation results the functional verification of the adders is done and from the synthesis report it is observed that, the Kogge Stone Adder gives better results compared to the other adders implemented in this paper, the area for the KSA is larger than RCA, CSA and CLA, from the top level schematic of all the above adders it is clear that the area for RCA, CSA and CLA the device utilization is same but the way they are implemented is different and the same is observed KSA adder design.

ACKNOWLEDGMENT

The Authors would like to thank the management and the Principal of SDMCET Dharwad for providing all the support and we would also like to thank Dept. of Electronics and Communication Engineering, SDMCET, for all the resources & support provided.

REFERENCES

- [1] http://en.wikipedia.org/wiki/Kogge%E2%80%93Stone_adder
- [2] Donald D. Givone, "Digital Principles and Design", Tata McGraw-Hill Edition 2002, chapter 5 – pp 231- 240
- [3] Douglas A. Pucknell, Kamran Eshraghian "Basic VLSI Design" third edition, chapter 8 – pp 192-220.
- [4] Anurag Sindhu, Ashish Bhatia, "8-bit Kogge Stone Adder" Course project.
- [5] R.Kathiresan, M.Thangavel, K.Rathinakumar, S.Maragadharaj "Analysis Of Different Bit Carry Look Ahead Adder Using Verilog Code" International Journal of Electronics and Communication Engineering & Technology (IJECE), ISSN 0976 – 6464(Print), ISSN 0976 – 6472(Online) Volume 4, Issue 4, July-August (2013), © IAEME
- [6] Lakshmi Phani, Deepthi Bollepalli, "Design And Implementation Of Fault Tolerant Adders On Field Programmable Gate Arrays" A thesis report , The University of Texas at Tyler May 2012.
- [7] Mr. Pakkiraiah Chakali, Mr. Madhu Kumar Patnala, "Design of High Speed Kogge-Stone Based Carry Select Adder", International Journal of Emerging Science and Engineering (IJESE) ISSN: 2319–6378, Volume-1, Issue-4, February 2013 34
- [8] Ms. Madhu Thakur, Prof. Javed Ashraf, "Design of Braun Multiplier with Kogge Stone Adder & It's Implementation on FPGA" ,International Journal of Scientific & Engineering Research, Volume 3, Issue 10, October-2012 1 ISSN 2229-5518
- [9] <http://www.goddard.net.nz/files/jsksadddergen/ksadddergen.html>
- [10] <http://www.minecraftforum.net/topic/394747-4-bit-kogge-stone-adder/>
- [11] http://venividiwiki.ee.virginia.edu/mediawiki/index.php/Group_name:_NAND
- [12] Adilakshmi Siliveru, M.Bharathi, "Design of Kogge-Stone and Brent-Kung adders using Degenerate Pass Transistor Logic" International Journal of Emerging Science and Engineering (IJESE) ISSN: 2319–6378, Volume-1, Issue-4, February 2013

AUTHORS



Mr. Kunjan D. Shinde received B E degree in Electronics & Communications Engineering from university of Visveswaraya Technology, Belgaum and pursuing M.Tech. in Digital Electronics from University of Visveswaraya, Belgaum. His research interests include VLSI design, Error Control Coding, Robotics and Digital system design.



Design.

Mrs. Jayashree C. Nidagundi is with SDMCET, Dharwad, Karnataka, India. She is serving as Assistant Professor in the Department of Electronics & Communications Engineering. Her research interests include VLSI design, Error Control Coding and Digital Circuit