Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 7 Issue 04, April-2018

Common Mode Feedback for Fully Differential Amplifier in ami06 micron CMOS process

Ravi Teja Bojanapally
Department of Electrical and Computer Engineering,
Texas Tech University, Lubbock, Texas, USA.

***Abstract*— This paper is about the design of the schematic of a common mode feedback for fully differential amplifier. The circuit is designed using CMOS ami06 technology in Cadence. The circuit is optimized to provide a Figure of Merit of 100.74*10^{9}Hz/A and phase margin more than 60 degrees. The layout of the design is done and the LVS match is obtained.**

Index Terms*— Common-mode feedback, Extracted file, Fully differential amplifier, CMOS ami06 technology, DC analysis, LVS match, STB simulation

I. INTRODUCTION

AFully differential amplifier is a DC-coupled high-gain voltage amplifier which has differential inputs and differential outputs. A common-mode feedback circuit senses the common mode voltage and compares it with a reference and feeds it back to the correcting common mode signal as to cancel the output common mode current component and to fix the dc outputs to the desired level.

Common mode feedback network consists of a simple feedback which stabilizes the common mode voltage without affecting the differential mode operation of the circuit. Referring to Fig1, if the common mode voltage at node Vout1 increases, the current through transistor M10 increases thereby reducing the current though M13 transistor. Since the gate voltages of M13 and M3 transistors are the same, the gate voltage of M3 increases thereby decreasing the voltage at the drain of M3 due to inversion. Thus, the Vout1 value is decreased to the desired level.

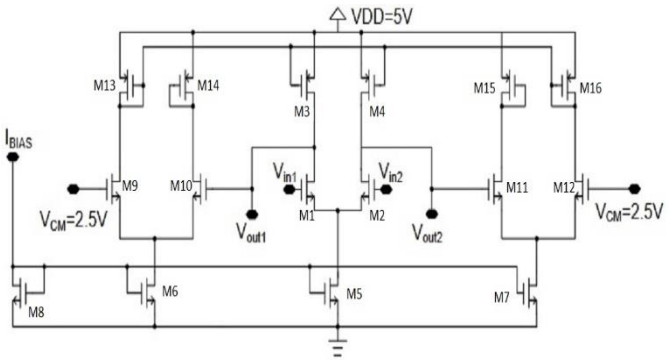

Fig1: Common mode feedback for fully differential amplifier

II. DESIGN AND CIRCUIT ANALYSIS

A. *Transistor Sizing*

The size of a transistor is determined by its W/L ratio. The ratio of size of transistor M5 to size of transistor M8 should be large to allow more current flow through the differential pair to obtain high gain. The current through M5 is equally divided between transistors M1 and M2. Size of transistors M1 and M2 should be more to achieve high gain. The sizes of other transistors should be chosen to ensure that sufficient current flows through them to operate in active region.

Transistors	Width	Length
M1, M2	4*12µm	1.95µm
M3, M4	8*4.05µm	1.95µm
M5	8*7.95µm	1.95µm
M6, M7	4*7.95µm	1.95µm
M8	1*7.95µm	1.95µm
M9, M10, M11,M12	4*6µm	1.95µm
M13,M14,M15,M16	4*4.05µm	1.95µm

Table1: Transistor sizes

B. *Bias Current*

A bias current is provided at the drain of transistor M8 which is then mirrored to transistors M5, M6, M7 depending on the ratio of their sizes. The value of the bias current chosen is 5µA. This value is chosen to mirror sufficient current so that all the transistors are in active region and the total DC current consumption is less to optimize the Figure of Merit(FOM).

III. CIRCUIT SIMULATION

Circuit is simulated using Cadence software. The schematic of the common mode feedback for fully differential amplifier circuit is setup with desired transistor sizes and bias current as shown below.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 7 Issue 04, April-2018

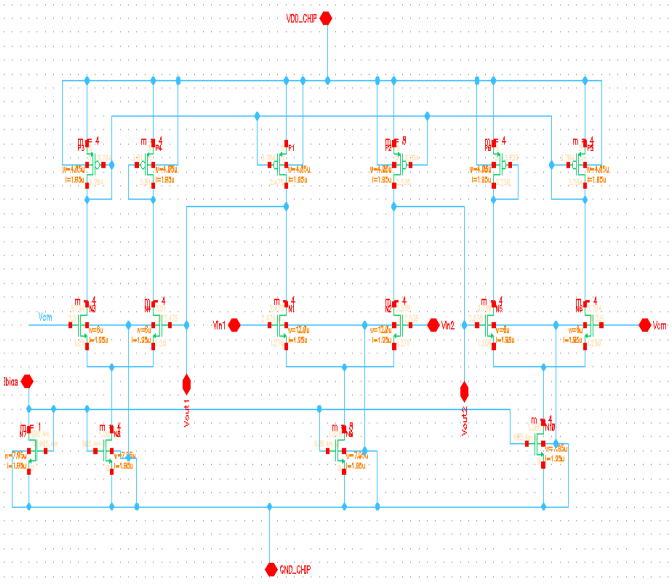

Fig2: Schematic with transistor sizes

DC simulation is performed using spectre simulator. The DC operating points and DC node voltages are annotated.

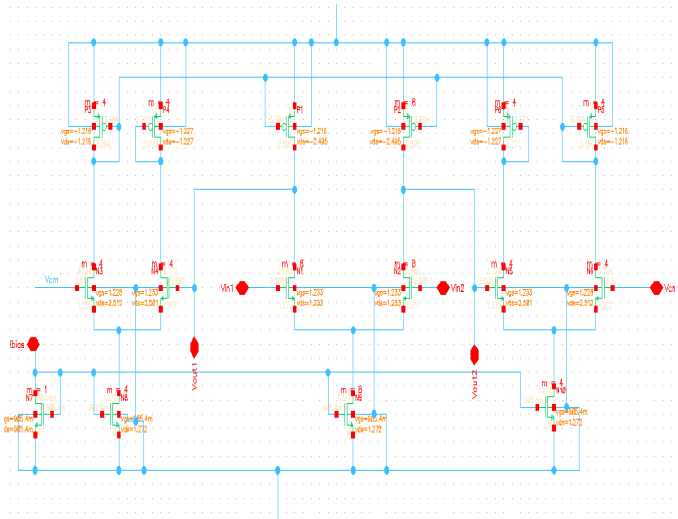

Fig3: Schematic with DC node voltages

Transistors	Current
M1 M2 M3 M4 M6 M7	20.32µA
M9 M12 M13 M16	9.747µA
M10 M11 M14 M15	10.57µA
M5	40.63µA
M8	5µA

Table2: Currents flowing through transistors

IV. GAIN AND PHASE MARGIN OF DIFFERENTIAL AND COMMON MODE FEEDBACK LOOPS

The figure below is used as a test bench to simulate differential and common mode loop gains.

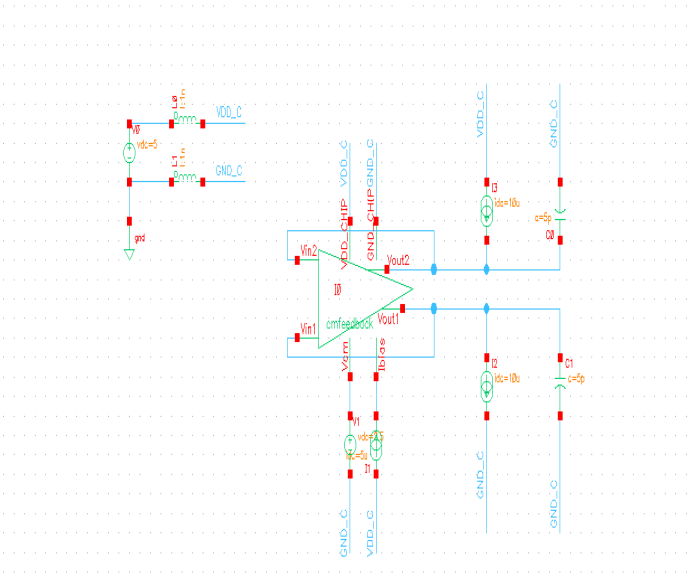

Fig4: Test bench

Transistors	Current(µA)
M1	10.34µA
M2	30.3µA
M3	20.34µA
M4	20.3µA
M5	40.64µA
M6	20.31µA
M7	20.33µA
M8	5µA
M9 M12 M16	9.747µA
M10 M11 M14 M15	10.57µA

Table3: Currents through transistors after introducing test bench

A. Differential mode feedback loop

To obtain the gain and phase plots of differential mode feedback loop, we introduce a CMDM probe in the schematic such that both the common mode and differential mode loops are broken. STB analysis is performed using spectre simulator to obtain the gain and phase plots.

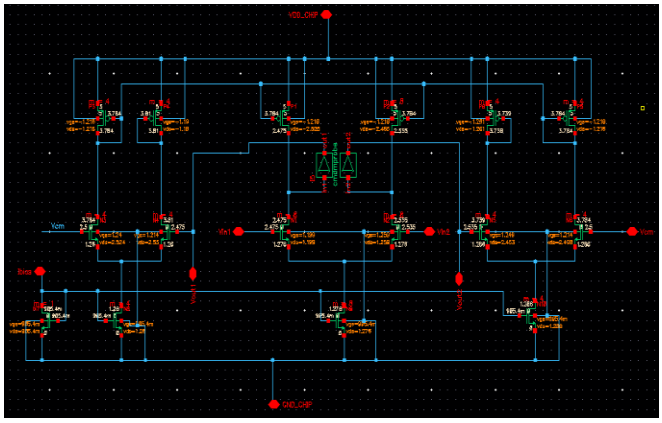

Fig5: Schematic with CMDM probe

To calculate phase margin and gain of differential mode feedback loop, the CDF parameter value in CMDM probe is set to -1.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 7 Issue 04, April-2018

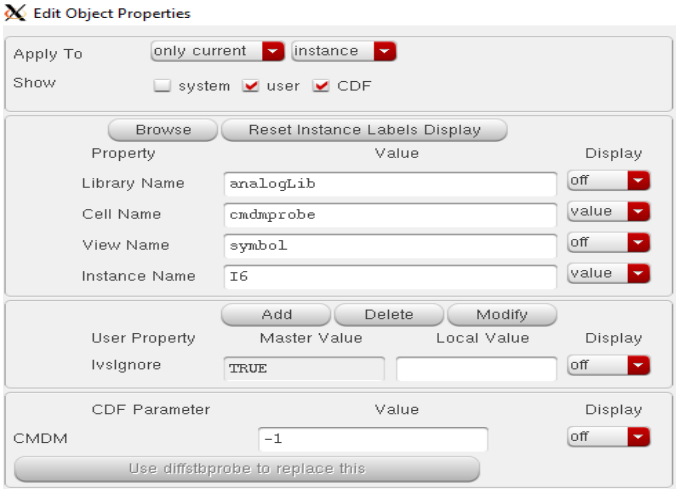

Fig6: CMDM probe Edit Object Properties window

For differential mode, a Gain of 46.946db and a Phase Margin of 88.6425deg is obtained.

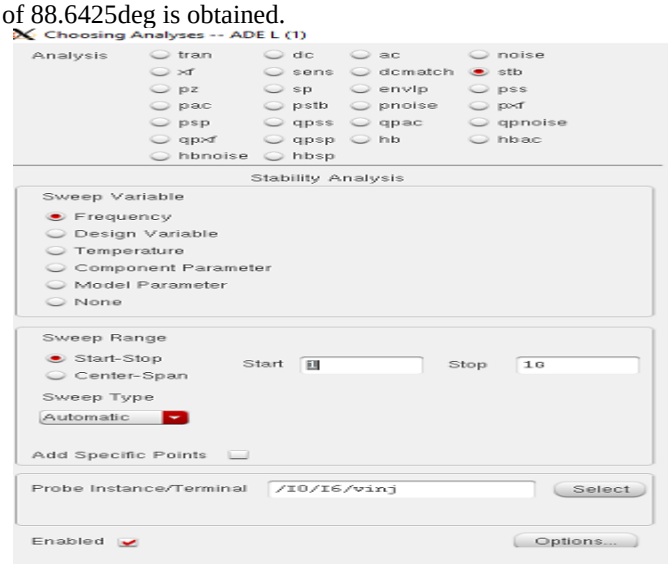

Fig7: STB simulation window

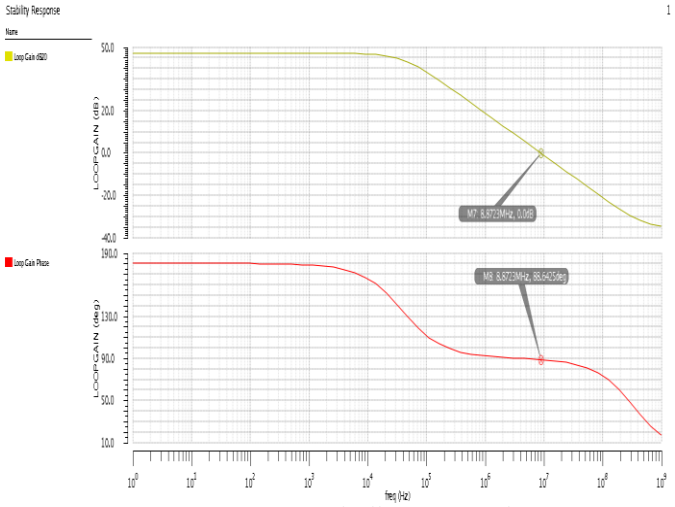

Fig8: Gain and Phase plot of differential mode feedback

B. Common mode feedback loop

To measure the gain and phase margin of common mode feedback loop, the CDF parameter value of CMDM probe is set to 1. A gain of 49.8712db and a Phase Margin of 83.3384deg is obtained.

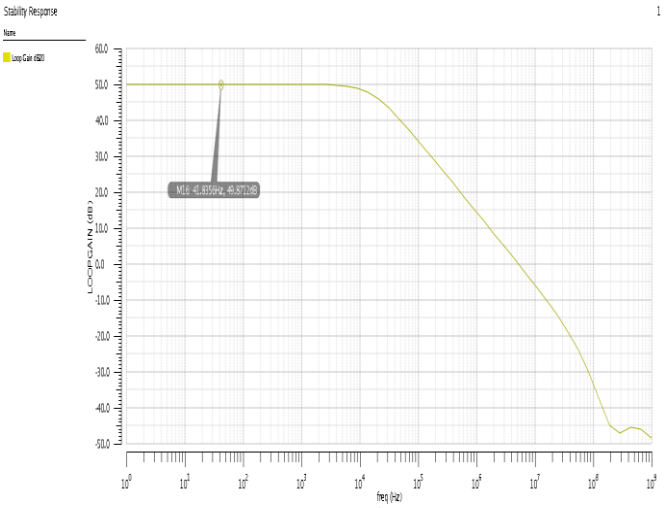

Fig9: Common mode feedback Gain

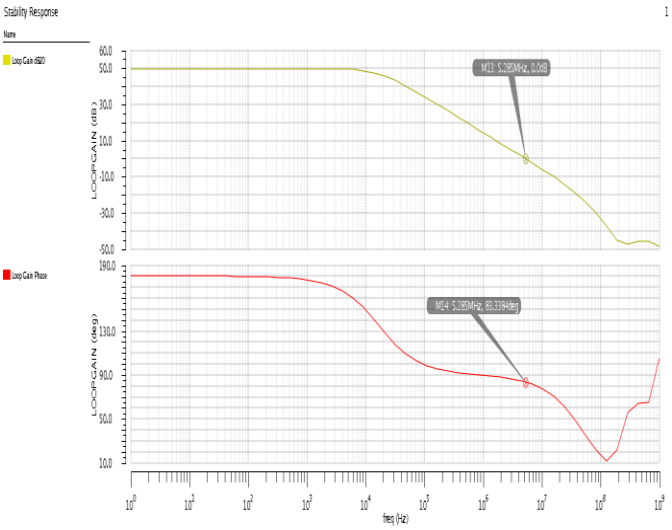

Fig10: Common mode feedback Phase Margin

Loop	Gain	Phase Margin
Differential mode	46.946db	88.6425deg
Common mode	49.8712db	83.3384deg

Table4: Values of gain and phase margin

C. Figure of Merit

Figure of Merit (FOM) is defined as the ratio of Gain Bandwidth product to the total DC current. Figure of merit of differential mode gain is calculated. The total DC current is measured as 86.27µA. The obtained bandwidth is 39.0634KHz. The Gain Bandwidth is 8691MHz.The Figure of Merit is $100.74*10^9$Hz/A.

Parameter	Value Obtained
DC current	86.27µA
Gain	46.946db
Bandwidth	39.0634KHz
Gain Bandwidth	8691MHz
Figure of Merit	$100.74*10^9$Hz/A

Table5: FOM parameter values

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 7 Issue 04, April-2018

V. LAYOUT, DRC AND LVS

A. *Layout*

Layout is designed using common centroid technique with multi fingered gates. The advantages of common centroid layout are immunity from cross-chip gradients, best-matching performance possible and reduced area by sharing the sources. Multi fingered gates are used to reduced series resistance in gate and minimize drain-to-bulk parasitic capacitance.

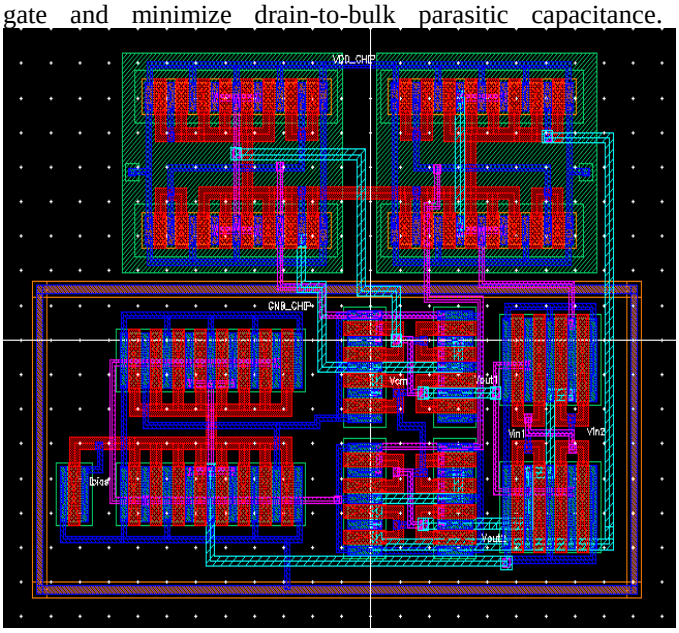

Fig11: Layout

B. *DRC*

DRC stands for Design Rule Check. It is used to determine whether the layout satisfies the recommended design rules.

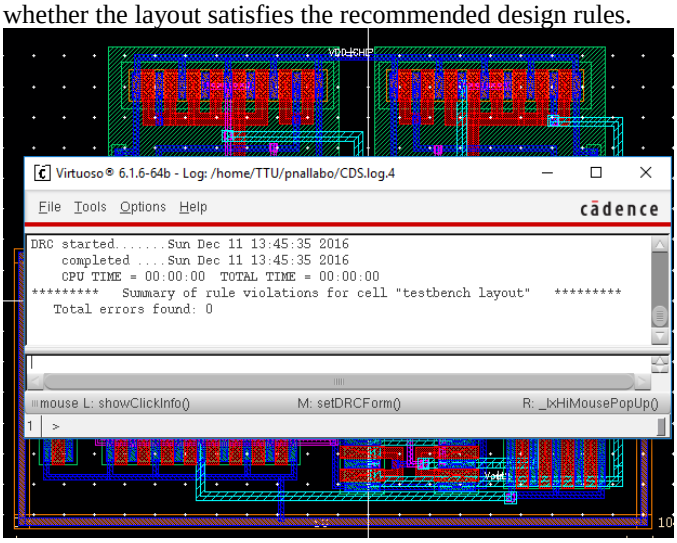

Fig12: CDS.log window showing 0 DRC errors

C. *LVS*

LVS stands for Layout Versus Schematic. LVS match is performed to check if the layout designed matches with the schematic. The extracted layout file is compared with the schematic.

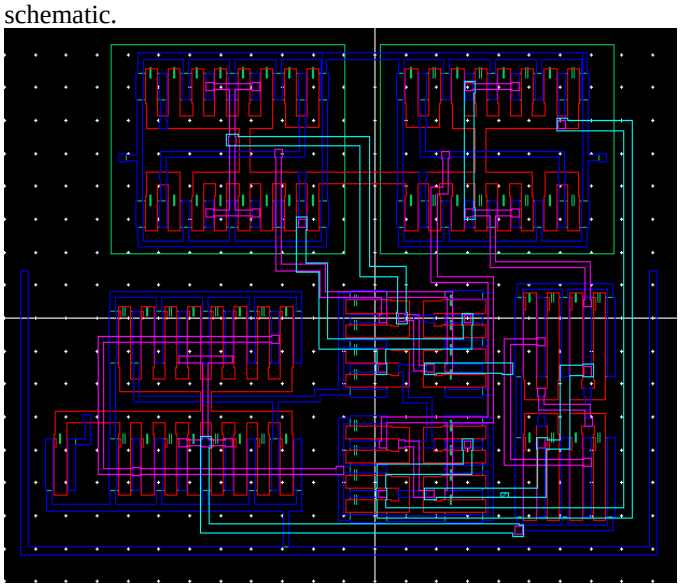

Fig13: Extracted Layout

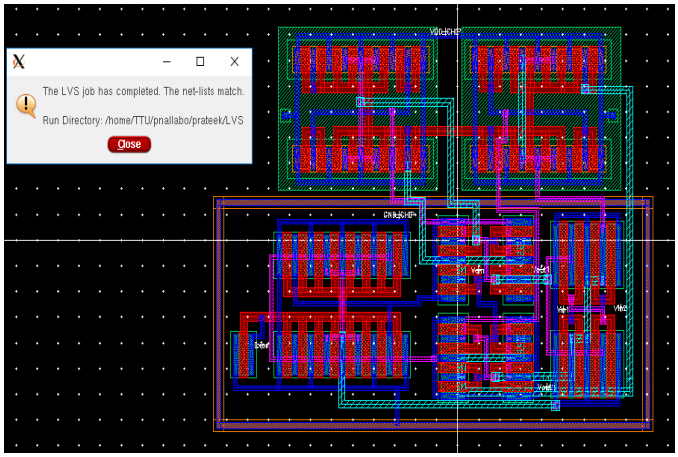

Fig14: Window showing LVS match

```
Net-list summary for /home/TTU/pnallabo/prateek/LVS/layout/netlist
   count
      14              nets
       8              terminals
      32              pmos
      41              nmos

Net-list summary for /home/TTU/pnallabo/prateek/LVS/schematic/netlist
   count
      14              nets
       8              terminals
       6              pmos
      10              nmos


   Terminal correspondence points
   N7          N4          GND_CHIP
   N11         N1          Ibias
   N8          N3          VDD_CHIP
   N6          N8          Vcm
   N13         N10         Vin1
   N12         N13         Vin2
   N10         N12         Vout1
   N9          N7          Vout2

Devices in the rules but not in the netlist:
       cap nfet pfet nmos4 pmos4

The net-lists match.
```

Fig14: LVS file

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 7 Issue 04, April-2018

VI. RESULTS

A. *Differential mode STB analysis:*

Gain= 46.946db
Phase Margin= 88.6425deg
Bandwidth= 39.0634KHz
Gain Bandwidth= 8691MHz
Total DC Current= 86.27µA
Figure of Merit(FOM)= $100.74*10^{9}$Hz/A

B. *Common mode STB analysis*

Gain= 49.8712db
Phase Margin=83.3384deg

VII. CONCLUSION

A fully differential amplifier with common mode feedback is designed. Simulations have been performed and Phase Margin better than 60degrees is obtained. The layout is designed and LVS net-lists match.

VIII. REFERENCES

[1] Behzad Razavi's Design of Analog CMOS Integrated Circuits.
[2] Dr. Changzhi Li's handout on Design of Analog IC, Texas Tech University.
[3] P.M. VanPeteghem; J.F. Duque-Carrillo. "A general description of common-mode feedback in fully-differentialamplifiers", IEEE International Symposium on Circuits and Systems, 1990, 312 – 320, vol.4.
[4] Lida Kouhalvandi; Sercan Aygün; Ece Olcay Güneş; Mürvet Kırcı. "Design of a fully-differential double folded cascode class AB opamp with continuous time common mode feedback network for 12-bit pipeline ADC applications", 2017 International Conference on Computer Science and Engineering (UMBK), 393 -396.
[5] M. Das, Improved Design Criteria of Gain-Boosted CMOS OTA with High-Speed Optimizations, IEEE Trans. on Circuits and Systems II Vol. 49, No. 3, 2002, 204-207.
[6] Shubhara Yewale, R. S. Gamad, "Analysis and Design of High gain Low Power Fully Differential GainBoosted Folded-Cascode Op-amp with Settling time optimization", International Journal of Engineering Research and Applications (IJERA), Vol. 1, Issue 3, 666-670.