Commercially Available Fpgas And Its Architecture- Survey

Mr. Sandip Yergude
M.Tech II Year
VITS, Karim Nagar (A.P)

Miss. Monica Nagdive
M.Tech I Year
WCEM,Nagpur

ABSTRACT

This paper will provide a survey of commercially available FPGAs and its architecture which is a part of commercially available high capacity field programmable devices i.e. FPDs. In this paper we first describe the recent evolution of FPDs which is having three types: simple PLD (SPLDs), Complex PLDs (CPLDs) and field programmable Gate Arrays (FPGA). Then we give details of commercially available and most important field programmable gate arrays with its architecture and also the example of applications of all two devices. This will focus entirely on commercially available field programmable Gate arrays (FPGAs).

1. INTRODUCTION TO FPDS

Field- programmable Device(FPD) is a general term that refers to any of the type of integrated circuit which is used for implementing digital hardware where the chip can be configure by end user to realize the different specific design for programming of such device, there will be need of special programmable unit but some chips are in system configured programmable logic device(PLDs) is the another name of FPDs although it is same but we prefer term FPD because the word PLD has referred to relatively simple type of devices.

The market of FPDs has grown dramatically over past decade where new and wide applications are needed. Designers need to think and understand the requirement of chips for special function choose a particular product, learn the vendor specific software and then design the hardware. The emphasis of this paper is an devices with relativelyhigh capacity, field programmable GateArrays (FPGAs).Before starting, we describe about the three main categories of FPDs. These are as follows:

Simple PLD (SPLD)

It refers to any type of simple PLD usually either a PLA or PAC.

CPCD-It is a more complex type of PLD that consist of arrangement of multiples SPLD on a single chip. The alternative name for this type of CPLD are enhanced PLD (EPLD), super PAC mega PAL.

IPGAs- It is a field programmable Gate Arrays which featuring a general structure with very high logic capacity. It offers more narrow logic resources whereas CPLDs features logic resources with wide number of inputs. FPGA also offer a higher ratio of flip-flops to logic resources than do CPLDs.

2. EVALUATION OF FPDS

Programmable Read only memory (PROM) is the first type of user programmable chip that could implement the logic circuit. A PROM contains a full decoder for its address inputs also the PROMs are inefficient to realize logic circuit, and so are rarely used in practice. Then the first device developed specifically for implementing logic circuit was field programmable Logic Array (FPLA). The FPLA consist of two levels of logic gates a programmable ‘wires’ and plane followed by programmable ‘wired’ or plane. FPLA is also called as simple PLA. So a PLA is structured to any of its inputs can be AND’ed together in AND plane. Thus, AND plane output can correspond to the any product term of the inputs. Thus AND plane outputs can correspond to any product of inputs.Thus each OR plane output can be configured to produce the logical sum of AND plane outputs. Thus the PLAs with

structure are well suited for implementing the logic function in sum-of-products (SOP) form.

The main drawbacks of PLAs when they were introduced in the early 1970s by Philips were that they were expensive to manufacture and offered poor speed performance. These disadvantages were due to the two levels of configurable logic, because programmable logic planes were difficult to manufacture and introduced significant propagation delays. To overcome these drawbacks, Programmable Array Logic (PAL) devices were developed. PACs have a single level of programmability consisting of programmable 'wired' AND plane that feeds fixed OR gates in figure 1. PAL usually contains Flip-Flop which was connected to the OR gate output so that sequential circuits gets realized. These devices are important because they had preferred effect on digital hardware design and also they are thebasis for newer, more sophisticated architectures. All small PLDs, like PALs, PLAs and PAC like devices are grouped into single category called SPLD, which is having low cost and very high pin-to-pin speed performance.

As new advancement in technology taken place it has become possible to produce devices with higher capacity than SPLDs. The large capacity devices can be design by integrating multiple SPLDs onto a single chip and provide interconnect to programmable connect the SPLD blocks together. The most commercial FPD product which areexisting in market are referred to as complexPLDs (CPLDs). CPLDs were pioneered by Altera which called as classic EPLDs and then developed the Max series MAX5000, MAX 700 and MAX 9000. CPLDs provide large capacity up to 50 typical SPLDs devices but it is somewhat difficult to extend thisarchitecture to higher densities. In this paper we are focusing on FPGA.

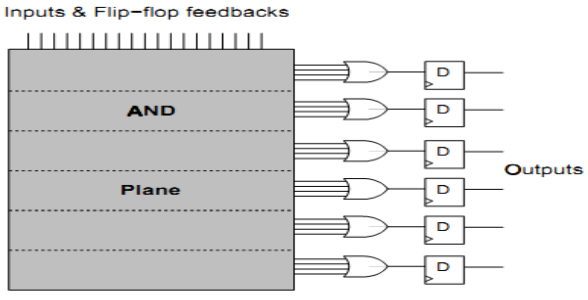

Figure 1- PAL structure

3. GENERAL ARCHITECTURE OF FPGA

Today, the highest capacity general purpose logic chips available are the traditional gate arrays which is sometimes referred as mask programmable Gate Arrays (MPGAs). It consists of an array of pre-fabricated transistors customized into use logic circuit by connecting the transistors with custom wires. The customization is preferred during chip fabrication by specifying the metal interconnect and this means that in order for user to employ MPGA a large set up cost is involved and time required for manufacturing is long, although it is not clear FPDs. Thus the MPGAs motivated the design of the user programmable equivalent called Field Programmable Gate Arrays (FPGA) like that of MPGAs, FPGAs comprise an array of circuit elements called logic blocks, and interconnected resources. But the FPGA configuration is performed through programming by end user. The structure of typical FPGA architecture appears in figure 2. As the only type of FPD that supports very high logic capacity, FPGAs have been responsible for a major shift in the way by which digital circuits are designed.

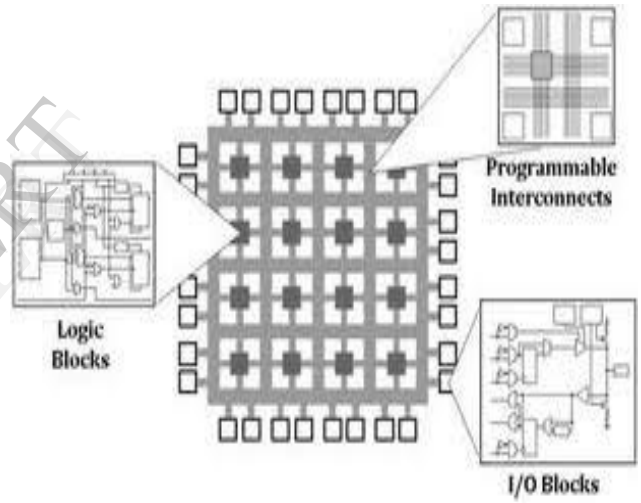

Figure 2- Structure of an FPGA

4. COMMERCIALLY AVAILABLE FPGAS

As it is one of the largest growing segments of semiconductor industry, the market place of FPGA is volatile considering this fact the pool of companies involved changes rapidly and it is difficult to say which products will be suitable significantly when industry reaches stable state. For this reason we will not focused to mentions all of the FPGA manufactures that are currently exist but we focus on those companies whose products are widely used. While describing each device we give its capacity it is vendor specific two input NAND gates. The gate count is an especially continuous issue in the FPGA industry and no need to take seriously the number given in this paper. There are two basic categories of FPGAs in market i) SRAM-

based FPGAs and ii) Antifuse-based FPGAs. Xilinx and Altera are the leading manufacturers in terms of number of user in first category. With the major competitor being AT & T. Actel, Quick logic and cypress and Xilinx offer antifused based product.

4.1 Xilinx SRAM-based FPGA's:

Xilinx FPGAs is having array based structure that means each chip comprises a two dimensional array of logic blocks which can be interconnected via horizontal and vertical routing channels. Figure shows the architecture of Xilinx SRAM based FPGAs. Xilinx introduced first FPGA family called XC 2000 series about 1985 and now provides three more generation: XC3000, XC4000, and XC5000. Though the XC3000 are still widely used we will focus on most recent XC4000. XC5000 is similar to XC4000, but has been developed to offer similar features at a more attractive price, with some penalty in speed; Also Xilinx recently introduced an FPGA family on antifuses called the XC8100.

The Xc4000 features a logic block called a configurable Logic block (CLB) that is based on Look up table(LUT). It is a small one bit wide memory array, where the address lines for the memory are inputs of the logic block and the one bit output from the memory is the LUT output. The XC4000 CLB contains three separate LUTs in the configuration shown in figure. There are two 4-input LUTs that are field by CLB inputs and the third LUT can be used in combination with other two. This allows the CLB to implement a wide range of logic function of up to nine inputs, two separate functions of four inputs or other possibilities. Each CLB contains two flip-flops.

With logic the other key features that characterizes an FPGA is its interconnect structure. The XC4000 interconnect is arranged in horizontal and vertical channels. Each channel contains some number of short wire segments that span a single CLB (the number of segments in each channel depends on the specific part number),longer segments that span two CLBs and very long segments that span the entire length or width of the chip. Programmable switches are available to connect the inputs and outputs of CLBs to the wire segments, or to connect one wire segment to another. A small section of a routing channel representative of an XC4000 device appears in figure. The figure shows only the wire segments in a horizontal channel, and does not show the vertical routing channels, the CLB inputs and outputs, or the routing switches. An important point worth nothing about the Xilinx interconnect is that signals must pass through switches to reach one CLB from another, and the total number of switches traversed depends on the particular set of wire segments used. Thus, Speed-performance of an implemented circuit depends in part on how the wire segments are allocated to individual signals by CAD tools.

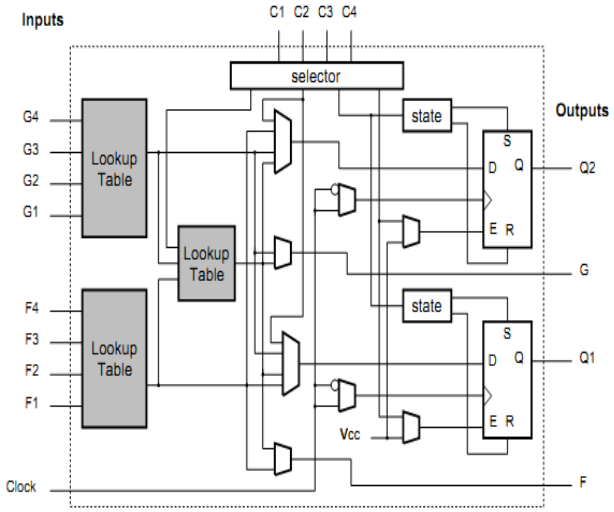

Figure 3- Xilinx XC4000 Configurable Logic block

4.2 Altera FLEX 8000 and FLEX 10000 FPGAs

Altera's FLEX 8000 series consist of a three-level hierarchy much like that found in CPLDs. However, the lowest level of the hierarchy consist of a set of lookup tables, rather than an SPLD like block, and so the FLEX 8000 is categorized here as an FPGA. It should be noted, however that FLEX 8000 is a combination of FPGA and CPLD technologies. FLEX 8000 is SRAM-based and features a four-input LUT as its basic logic block. Logic capacity ranges from about 4000 gates to more than 15,000 for the 8000 series.

The overall architecture of FLEX 8000 is illustrated in figure. The basic logic block, called a Logic Element (LE) contains a four-input LUT, a flip-flop, and special purpose carries circuitry for arithmetic circuits (similar to Xilinx XC4000). The LE also includes cascade circuitry that allows for efficient implementation of wide AND functions. Details of the LE are illustrated in figure.

In the FLEX 8000, Les are grouped into sets of 8, called Logic Array Blocks (LABs, a term borrowed from Altera's CPLDs). As shown in figure, each LAB contains local interconnect and each local wire can connect any LE to any other LE within the same LAB.

Local interconnect also connects to the FLEX 8000's global interconnect, called Fast Track. Fast Track is similar to Xilinx long lines in that each Fast track wire extends the full width or height of the device. However, a major difference between FLEX 8000 and Xilinx chips is that Fast Track consist of only long lines. This makes the FLEX 8000 easy for CAD tools to automatically configure. All Fast Track wires horizontal wires are identical, and so interconnect delays in the FLEX 8000 are more predictable than FPGAs that employ many smaller length segments because there are programmable switches in the longer paths. Predictability is furthered aided by the fact that connections between horizontal and vertical lines pass through active buffers.

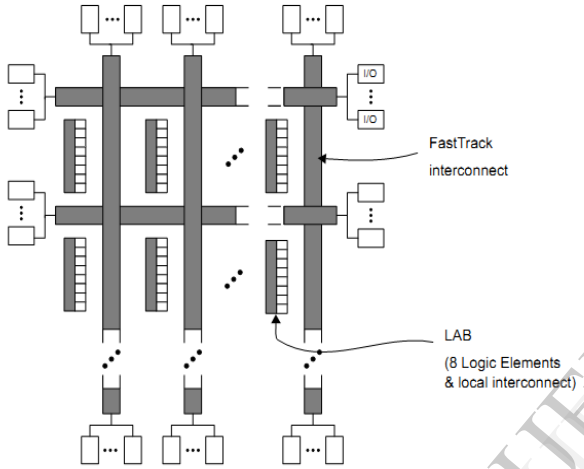

Figure 4- Structure of Altera Flex 8000FPGAs

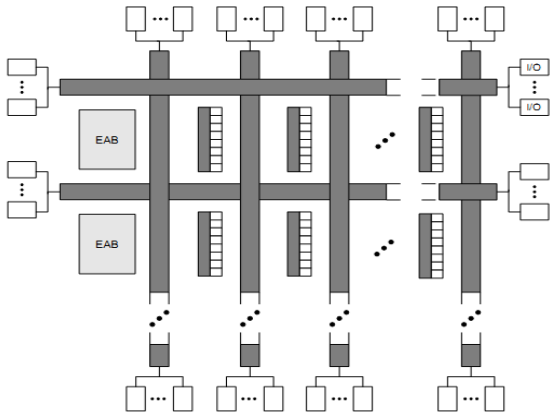

Figure 5- Structure of Altera Flex 10000 FPGAs

4.3 AT & T ORCA FPGAs

AT and T's SRAM-based FPGAs feature an overall structure similar to that in Xilinx FPGAs and is called optimized Reconfigurable Cell Array(ORCA). The ORCA logic block is based on LUTs, containing an array of Programmable Function Units (PFUs). The structure of a PFU is shown in figure. A PFU possesses a unique kind of configurability among LUT-based logic blocks, in that it can be configured in the following ways: as four $-inputs LUTs, as two 5-input LUTs, and as one 6-input LUT. A key element of this architecture is that when used as four 4-input LUTs inputs must come from the same PFU input. While this reduces the apparent functionality of the PFU, it also significantly reduces the cost of the wiring associated with the chip. The PFU also includes arithmetic circuitry, like Xilinx XC4000 and Altera FLEX 8000, and like Xilinx XC4000 a PFU can be configured as a RAM block. A recently announced version of the ORCA chip also allows dual-port and synchronous RAM.

ORCAs interconnect is also different from those in other SRAM-based FPGAs. Each PFU connects to interconnect that is configured in four-bit buses. This provides for more efficient support for "system-level" designs, since buses are common in such applications. The ORCA family has been extended in the ORCA 2 series, and offers very high logic capacity up to 40,000 logic gates. ORCA 2 features a two-level hierarchy of PFUs based on the original ORCA architecture.

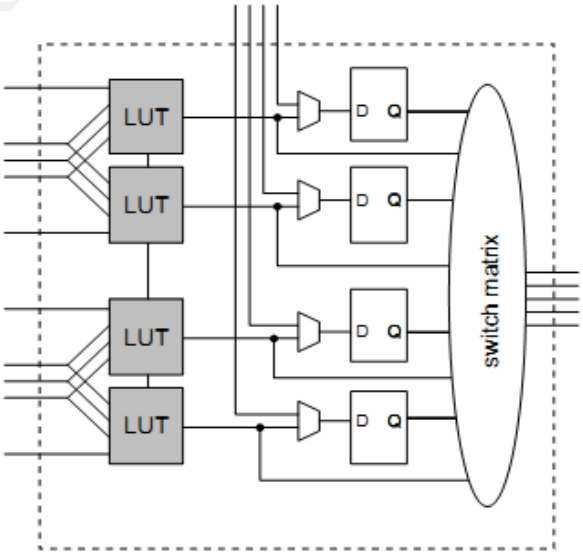

Figure 6- AT & T Programmable Function unit

4.4 Actel FPGAs

In contrast to FPGAs described above, the devices manufactured by Actel are based on antifuse technology.Actel offers three main families: Act 1, Act 2, and Act 3. Although all three generations have similar features, this paper will focus on the most recent devices, since they are apt to be more widely used in the longer term. Unlike the FPGAs described above,

Acteldevices are based on a structure similar to traditional gate arrays; the logic blocks are arranged in rows and there are horizontal routing channels between adjacent rows. This is architecture is illustrated in figure. The logic blocks in the Actel devices are relatively small in comparison to the LUT-based ones describes above, and are based on multiplexers. Figure illustrates the logic block in the Act 3 and shows that it comprises an AND and OR gate that are connected to a multiplexer based circuit block. The multiplexer circuit is arranged such that, in combination with the two logic gates, a very wide range of functions can be realized in a single logic block. About half of the logic blocks in an Act 3 device also contain a flip-flop. However, Actel provides a rich selection of wire segments of different length in each channel and has developed algorithms that guarantee strict limits on the number of antifuses traversed by any two-point connection in a circuit which improves speed performance significantly.

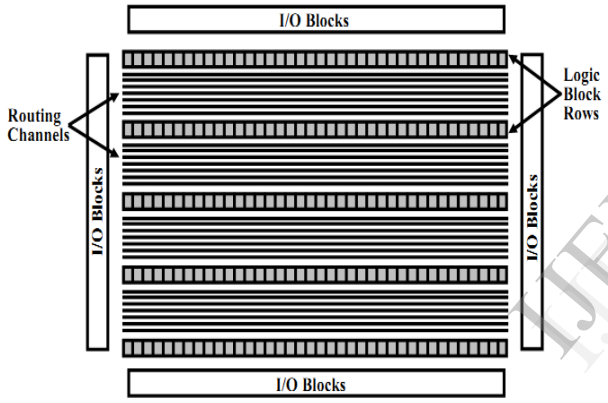

Figure7- Structure of Actel FPGAs

4.5 Quicklogic pASIC FPGAs

The main competitor for Actel in antifuse-based FPGAs is Quick logic, whose has two families of devices, called pASIC and pASIC-2. The pASIC-2 is an enhanced version that has only recently been introduced, and will not discussed here. The pASIC, as illustrated in figure, has similarities to several other FPGAs: the overall structure is array-based like Xilinx FPGAs, its logic blocks use multiplexers similar to Actel FPGAs, and the interconnect consist of only long-lines like in Altera FLEX 8000. We note that the pASIC architecture is now independently developed by cypress as well but this discussion will focus only on Quick logic's version of their parts.

Quicklogic's antifuse structure, called ViaLink ,is illustrated on the left-hand side of figure. It consists of a top layer of metal, an insulating layer of amorphous silicon, and a bottom layer of metal. When compared to Actel's PLICE antifuse, ViaLink offers a very low on-resistance of about 50 ohms (PLICE is about 300 ohms) and a low parasite capacitance. Figure shows that Via Link antifuses are present at every crossing of logic block pins and interconnect wires, providing generous connectivity. pASIC's multiplexer-based logic block is depicted in figure. It is more complex than Actel's Logic Module, with more inputs and wide(6-input) AND-gates on the multiplexer selectlines. Every logic block also contains a flip-flops.

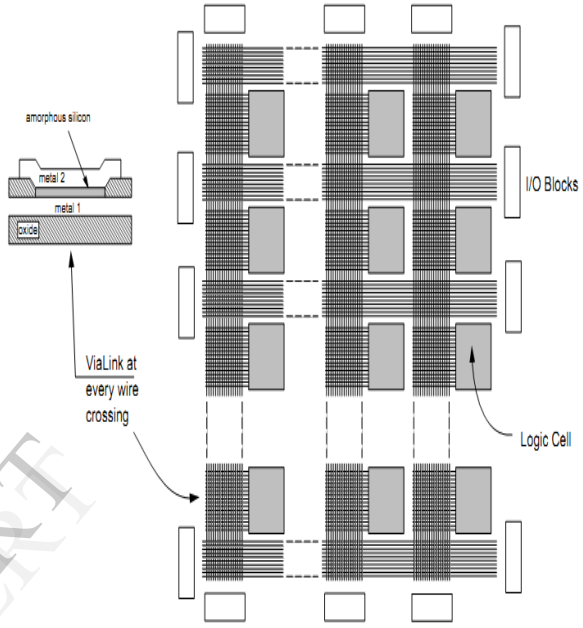

Figure 8- Structure of Quicklogic pASIC FPGA

5. APPLICATIONS OF FPGAS

FPGAs have gained rapid acceptance and growth over the past decade because they can be applied to a very wide range of applications. A list of typical applications includes: random logic, integrating multiple SPLDs, device controllers, communication encoding and filtering, small to medium sized systems with SRAM blocks, and many more.

Other interesting applications of FPGAs are prototyping of designs later to be implemented in gate arrays, and also emulation of entire large hardware systems. The former of these applications might be possible using only a single large FPGA(which corresponds to a small Gate Array in terms of capacity),and the latter would entail many FPGAs connected by some sort of interconnect; for emulation of hardware, Quick Turn has developed products that comprise many FPGAs and the necessary software to partition and map circuits.

Another promising area for FPGA application, which is only beginning to be developed, is the usage of FPGAs

as custom computing machines. This involves using the programmable parts to "execute" software, rather than compiling the software for execution on a regular CPU. The reader to the FPGA-Based custom Computing Workshop (FCCM) held for the last four years and published by the IEEE.

6. CONCLUSION

We have presented a survey on gate array describing the basic technology that provides the programmability and a description of many of the architectures in the current marketplace. We believe that overtime programmable logic will become the dominant form of digital logic design and implementation. Their ease of access, principally through the low cost of the devices, makes them attractive to small firms and small parts of large companies. As architecture improves the FPGA will used instead of mask-programmed Gate Arrays.

.

REFERENCES

[1] E. Hamdy et al, "Dielectric-based antifuse for logic and memory ICs" IEEE International Electron Devices Technical Digest,pp. 786-789,1988.

[2] Altera corporation, "MAX+plusII CAD Design System, Version 5.0", 1994.

[3] S. Trimberger, Field Programmable Gate Array Technology, Kluwer Academic Publishers,1994.

[4] J. Oldfield, R.Dorf, Field Programmable Gate Arrays, John Wiley and sons, Newyork,1995.

[5] Eric Monmasson, Morcian N. Cirstea, FPGA Design Methodology For Industrial Control System-A Review, IEEE Transaction In Industrial Electronics,Vol.54,No.4,August 2007.

[6] Chun Hok Ho,Chi Wai Yu, Wayne Luk, Steven J.E.Wilton, Floating Point FPGA: Architecture and Modeling ,IEEE Transaction on Very Large Scale Integration(VLSI) Systems, Vol.17,No.12, December 2009.