International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 2 Issue 4, April - 2013

Combined Operation Of DSTATCOM With Distributed Generation To Improve Power Quality

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Abstract— **This paper proposes a combined operation of the distribution static compensator (DSTATCOM) with distributed generation systems to improve power quality in low voltage grid systems. A distributed generation unit is connected to the dc-link of the DSTATCOM through suitable converter. The dc-link capacitor voltage of the DSTATCOM and the magnitude of three-phase grid voltages are used as feedback signals for two proportional integral controllers. The DSTATCOM controls the active power of the distribution generation system while compensating harmonics, reactive and neutral currents and provides load balancing in the gird currents. Apart from these the DSTATCOM is also capable for voltage regulation at the point of common coupling. In unity power factor mode of operation of DSTATCOM the reactive power supplied by grid is remains zero. But in zero voltage regulation modes sliding leading power factor is maintained. The simulation of the proposed system is carried out in the MATLAB environment using simulink and power system toolboxes.**

***Index Terms*—Distribution generation, distribution static compensator, harmonics, neutral current, reactive power.**

I. INTRODUCTION

THE rapid industrialization and dependence of mankind growths on electricity, the world energy demand has been increasing exponentially. However, the conventional energy resources are exhaustible and limited in use nowadays. Therefore, there is an urgent need to conserve what we have in hand. This has diverted a lot of research and attention of mankind towards alternate energy sources and wider use of energy efficient devices [1]. Also the present generating units and transmission lines are already loaded up to their rated maximum and it is not possible to load them further. As a result, the focus has shifted to generation of electric power locally using alternate source of energy. This has led to use of distributed generation (DG) [2]. Distributed generation encompasses a wide range of prime mover technologies, such as internal combustion (IC) engines, gas turbines, microturbines, photovoltaic cells, fuel cells and wind-power [3-5].

Moreover, the increasingly use of energy efficient devices results in continuous increment in the size and numbers of power electronics converters, adjustable speed drives, etc. for commercials, residential and industrial applications [6]. These power electronics devices operate on the sinusoidal supply voltages but at the same time they inject significant harmonics and draw reactive power from grids [7]. The loads responsible for injection of harmonics in the system are termed as nonlinear loads. Nowadays, the ac distribution systems are suffering from severe power quality problems due to continuous increment of nonlinear type of loads. In addition to harmonics and reactive current the large 1-phase nonlinear loads such as computers, lighting ballasts, small rating adjustable speed drives(ASDs), refrigerators and other commercial appliances etc. further complicate the issue by causing excessive neutral current in the three-phase and four-wire (3P4W) distribution supply systems [8]. The neutral conductor will carry a large percentage of each of the three-phase conductors' current even under balanced load conditions. The excessive neutral current may cause many adverse effects such as overloading power feeders, overloading distribution transformers, voltage distortion, and common mode noise [9-12].

It is obvious that DG interconnection should not disturb normal operation of loads and the network itself and the power quality indices should remain in the range required by standards viz. IEEE-519-1992/IEC-61000-3-12, etc. should not interrupt the sources operation. Therefore, DG integration may need some control devices to be applied in the network which will facilitate the integration process and assure the required power quality. The basic objective of the distribution generation system connected with grid is to control the power that the inverter injects into the grid. According to the grid demands, injected power does not only include the control of the reactive power, but also the control of the injected active power [13]. Fig.1 shows a general purpose block diagram of DG-grid with power electronics system for injecting DG power into the grid while improving the system power quality.

Many compensation methods are developed to mitigate these power quality problems in distribution systems are reported in literature [5]-[10], [13]-[16]. A group of controllers together called custom power devices (CPD), which include active power filters(APF) or more appropriately distribution static compensator (DSTATCOM), dynamic voltage restorer (DVR) and unified power quality conditioners(UPQC) are used for compensating power quality problems in current, voltage and both current and voltage, respectively. The DSTATCOM is a shunt connected device, which take care of the power quality problems in the currents. There are many DSTATCOM topologies reported in the literatures for 3P4W distribution systems such as four-leg voltage source inverter (VSI) [14], a three single-phase VSI

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[15], three-leg VSI with split capacitors [16], three-leg VSI with zigzag transformer [16]. Several studies proposed an interconnection system for DG with the power system through the DSTATCOM and APF because they give versatile solutions for improving the performance of DG [4, 11].

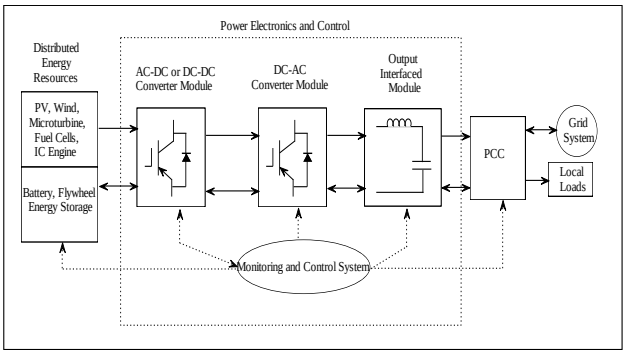


Fig.1. General purpose block diagram of DG-grid system with power electronic interfaced.

This paper proposed a simple control algorithm for combined operation four-leg VSI based DSTATCOM with distributed generation. The proposed controller is capable to control the active power of the distributed generated system while compensating load power factor, harmonics, neutral current, and load balancing under unbalanced and distorted grid voltages.

II. System Description and Design of DSTATCOM

A four-leg, PWM controlled voltage source converter (VSC) is used as a DSTATCOM and it has eight insulated-gate bipolar transistors (IGBTs), three interface inductors, and one dc-link capacitor. The single line diagram of the proposed DG-grid system interfaced with DSTATCOM is shown in Fig. 2(a) and the complete schematic of the proposed system is shown in Fig. 3 (a). A Three-phase grid of source resistance R_s, and inductance L_s per phase is supplying power to nonlinear load. A current controlled three-phase DSTATCOM with energy storage capacitor C_{dc} is connected in parallel with load and grid. The DSTATCOM consists of an inductor L_c and a resistance R_c (equivalent resistance of the inverter circuit) per phase and a three-phase IGBT bridge type current-controlled voltage source inverter (CC-VSI). A variable speed/power distributed generation unit is connected to the dc-link of DSTATCOM through AC-DC converter. A smoothing inductor of resistance R_{sm} and inductance L_{sm} per phase is also connected in series with nonlinear load.

For designing various parameters of the DSTATCOM the line voltage and the rating of the voltage source inverter are considered as 400 V and 10 kVA, respectively. The ac inductor, dc-link capacitor and the ripple filter selection are as below.

a. DC-Link Capacitor Voltage

The reference value of dc-link capacitor voltage of DSTATCOM is mainly depends upon the reactive power compensation capability [14]. For reactive power compensation the primary condition is that the magnitude of reference dc-link capacitor voltage should be higher than the PCC voltage V_L[13]. During reactive power compensation the operation of switches generate a voltage having fundamental component V_c towards AC side of the DC-AC converter (inverter). For proper reactive current compensation (to maintain source fundamental current I_{sp} in-phase with the V_L) the DSTATCOM generate a current I_{cq} of equal magnitude and 180^0 out of phase with load reactive current as shown in Fig. 2 (b).

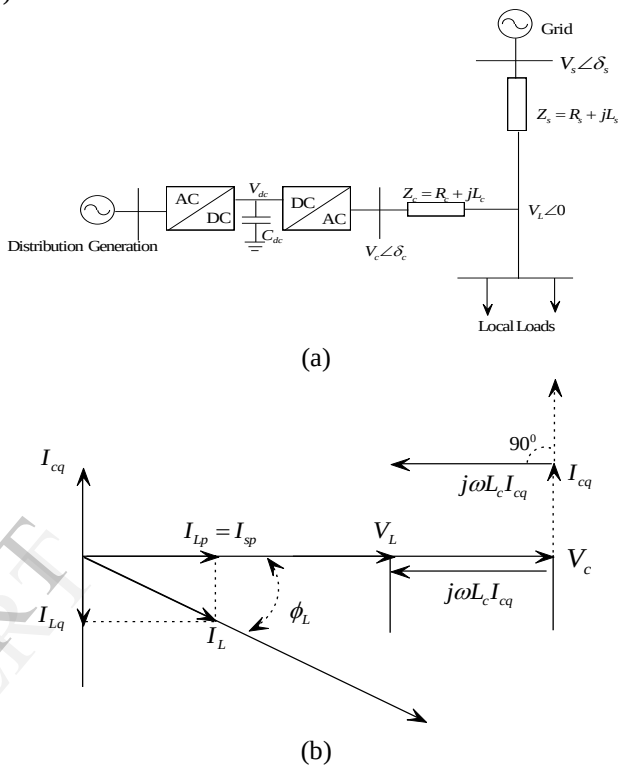


Fig.2 (a) Single line diagram of DG-grid interfaced system, (b) Phasor diagram of basic operation of DSTATCOM.

The vector diagram represents the reactive power flow in which source fundamental current I_{sp} is in-phase with PCC fundamental voltage V_L and the reactive component of filter current I_{cq} orthogonal to V_L. From this phasor diagram of DSTATCOM it is evident that,

$$V_c = V_L + j\omega L_c I_{cq} \tag{1}$$

From (1) I_{cq} is calculated as:

$$I_{cq} = \frac{V_c - V_L}{j\omega L_c} = \frac{V_c}{\omega L_c}\left(1 - \frac{V_L}{V_c}\right) \tag{2}$$

Three-phase reactive power delivered by the DSTATCOM is equal to the three-phase reactive power requirement of the nonlinear load, hence from vector diagram.

$$Q_{cq} = Q_L = 3V_L I_{cq} = 3V_L\left(\frac{V_c}{\omega L_c}\right)\left(1 - \frac{V_L}{V_c}\right) \tag{3}$$

From (4) it is evident that the DSTATCOM can compensate the load reactive current only when $V_c > V_L$ and for this case value Q_{cq} is positive. For the case when $V_c < V_L$, the Q_{cq} is negative and DSTATCOM will draw the reactive power from the utility. The upper limit of V_c is calculated on the basis of maximum compensation capacity of the DSTATCOM, calculated as follows:

$$\frac{dQ_{c1}}{dV_L} = 0$$

$$\frac{d}{dV_L}\left(\frac{3V_L V_c}{\omega L_c} - \frac{3V_L^2}{\omega L_c}\right) = 0\ ;\ V_c = 2V_L \tag{4}$$

Thus the maximum capacity of DSTATCOM can be obtained as,

$$Q_{cq\max} = \frac{3V_L^2}{\omega L_c}$$

Hence, the value of reference dc-link capacitor voltage of the DSTATCOM must be according to the reactive power requirement of the system. From above relations the range of V_{c1} will be,

$$V_L < V_c \le 2V_L$$

If it is assumed that the PWM converter operates in the linear modulation mode $0 \le m_a \le 1$ [10] then,

$$m_a = \frac{\sqrt{2}V_c}{V_{dc}} = \frac{2\sqrt{2}\,V_L}{\sqrt{3}V_{dc}},\quad \text{for } m_a = 1,\ V_{dc} = \frac{2\sqrt{2}V_L}{\sqrt{3}} \tag{5}$$

Thus V_{dcref} is obtained as 655.88 V for V_{L} of 400V (line voltage) and it is selected as 650 V.

b. DC-Link Capacitor

The energy E_{dc} required by the dc-link capacitor to charge the capacitor from actual V_{dc} to the reference voltage V_{dcref} can be expressed as:

$$E_{dc} = \frac{1}{2}C_{dc}(V_{dcref}^2 - V_{dc}^2) \tag{6}$$

On the other hand, the total energy E_{ac} delivered by the source will be as:

$$E_{ac} = 3K_L \frac{V_L}{\sqrt{3}}\frac{I_{sp}}{\sqrt{3}}.t \tag{7}$$

where, V_{L} is the line value of source voltage, I_{sp} is the line value of active component of source current, t is the time for which source supplies power and K_{L} is the over loading factor. The principle of energy conservation is applied as:

$$\left[\frac{1}{2}C_{dc}(V_{dcref}^2 - V_{dc}^2)\right] = (V_L)(K_L I_{sp}).t \tag{8}$$

Considering, a 5% (32.50 V) reduction in dc-link capacitor voltage during transients, V_{dcref} = 650 V, V_{dc}= 617.5 V, V_{L}= 400 V, I_{sp}= $\sqrt{3}$ *48.5 A, t= 1000 μs, K_{L}= 1.2, the calculated value of C_{dc} is 1957 μF and it is selected as 2000 μF.

c. Filter Inductor

The selection of the filter inductance (L_c) per phase depends on the current ripple $i_{\text{crp-p}}$, switching frequency f_{s} and dc-link capacitor voltage (V_{dc}) as [14]:

$$L_c = \frac{(\sqrt{3}m_a V_{dcref})}{(12K_L f_s i_{crp-p})} \tag{9}$$

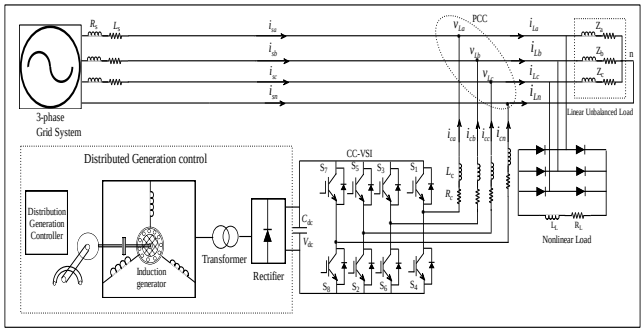
where, m_a is the modulation index and K_L is the over-load factor. Considering, $i_{\text{crp-p}}$ = 5%, f_{s}= 10 kHz, m_{a} = 1, V_{dcref} = 650 V, K_L = 1.2, the L_c value is calculated to be 1.86 mH. The round off value of L_c of 2.0 mH is selected in this investigation.

d. Voltage Ripple Filter

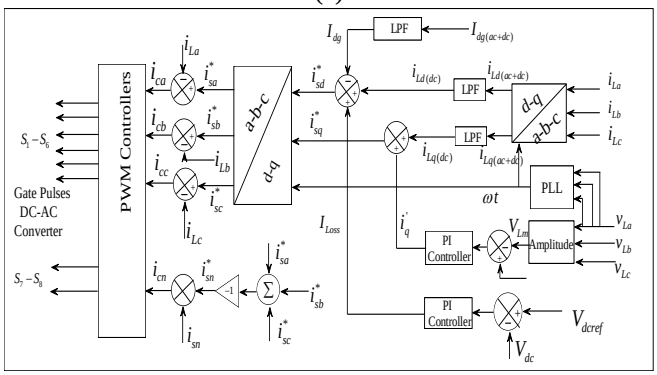
A first order low-pass filter tuned at half the switching frequency is used to filter the high frequency noise of the PCC voltages. For considering a low impedance of 10 Ω for the harmonic voltage at a frequency of 5 kHz, the ripple filter capacitor is designed as C_f = 3.6 μF when a series resistance R_f of 5 Ω is included in series with the capacitor C_{f}. The impedance at fundamental frequency is found to be 884 Ω, which is sufficiently large and hence the ripple filter draws negligible fundamental current.

III. OPERATION PRINCIPLE OF PROPOSED DSTATCOM

The Power as well as control circuit diagrams of the proposed DG-grid interconnected system with DSTATCOM are shown in Fig. 3 (a) and (b), respectively. The system works in interconnected mode when both the DG as well as the grid supplies power to the load. But it works in islanding mode when the voltage interruption on grid occurs. The control of DSTATCOM involved the control of active power supplied by DG and reactive power requirement of load. The ac-side voltages of the DSTATCOM interfaced inverter are controlled both in magnitude and phase to control the active and reactive power. The load currents, PCC voltages, and dc-link capacitor voltage of the DSTATCOM are sensed as feedback signals for the controller. The load currents are converted into the d-q-0 frame using park's transformation. The three-phase source voltages are applied to three-phase Phase Locked Loops (PLL) to synchronize the three-phase voltages with the voltages at PCC. The d-q components of load currents are then passed through low pass filters to extract the dc components.



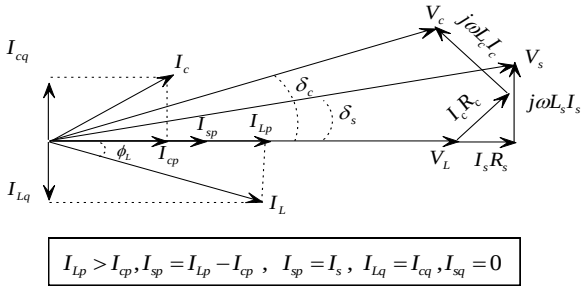
(a)



(b)

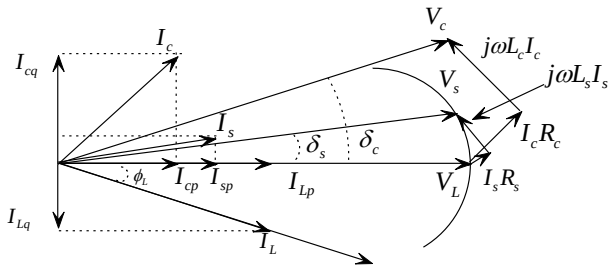
Fig. 3. Proposed DG-Grid interfaced system with DSTATCOM (a) Power circuit (b) Control circuit.

The error between the actual dc capacitor voltage and reference capacitor voltage of the DSTATCOM is sensed and is given to dc-bus proportional-integral (PI) controller whose output is added with the direct axis component i_{Ld} of the load currents. The active current supplied by the DG unit is now subtracted from the direct axis component of load currents to obtain the direct axis component of source current. Similarly, another PI controller is used to regulate the PCC voltages. The amplitude of the PCC voltages and their reference value are fed to another PI controller and whose output is added with the quadrature axis component i_{Lq} of the load currents. The resultant direct and quadrature axis currents are converted into the reference currents using Reverse Park's transformation. The desired source currents are now compared with the actual load currents to obtain the compensating currents which include both active current supplied by the DG unit and reactive current requirement of the load. The compensating currents are now applied to the hysteresis controller to obtain the switching pulses to switch the devices used in DSTATCOM configuration.



$I_{Lp} > I_{cp}, I_{sp} = I_{Lp} - I_{cp}\ ,\ \ I_{sp} = I_s\ ,\ I_{Lq} = I_{cq}, I_{sq} = 0$

(a)



$I_{Lp} > I_{cp}, I_{sp} = I_{Lp} - I_{cp}\ ,\ \ I_{sp} \neq I_s\ ,\ I_{cq} > I_{Lq}, I_{sq} \neq 0$

(b)

Fig. 4.Phasor diagram for forward interconnected mode (a) at unity power factor (b) at zero voltage regulation

Fig. 4 shows the vector diagrams of active power flow at unity power factor and zero voltage regulation for forward interconnected mode of operation. In which I_{sp}, I_{Lp}, and I_{cp} are the active fundamental currents of the grid (source), load and DG (ac-side of the inverter) respectively. And V_s, V_L, and V_c are the voltages at grid (source), load (PCC), and ac side of the DC-AC converter. The Φ_L is the load power factor angle and δ_s is the power angle between grid and load voltage and δ_c is the power angle between inverter and load voltage. I_{Lq} and I_{cq} are the reactive current component of load and DSTATCOM, respectively. Fig. 4 (b) shows the phasor diagrams of active power flow with zero voltage regulation in forward interconnected modes. Similar diagrams at unity power factor and zero voltage regulation can be drawn from reverse mode of operations.

IV. Proposed Control Algorithm

In order to examine the compensation mechanism let's assume that distribution generation uses a variable power generation system. The grid voltages at PCC of vector $[v_L(t)]$ and load currents of vector $[i_L(t)]$ consists a set of harmonic components H for $h \in H$ are expressed in (10) and (11) respectively, where h is the order of harmonics.

$$[v_L(t)] = \begin{bmatrix} v_{La}(t) \\ v_{Lb}(t) \\ v_{Lc}(t) \end{bmatrix} = \begin{bmatrix} \sum_{h\in H}^{H} V_{Lah} \sin(h\omega t + \alpha_{ah}) \\ \sum_{h\in H}^{H} V_{Lbh} \sin(h(\omega t - 2\pi/3) + \alpha_{bh}) \\ \sum_{h\in H}^{H} V_{Lch} \sin(h(\omega t + 2\pi/3) + \alpha_{ch}) \end{bmatrix} \quad (10)$$

$$[i_L(t)] = \begin{bmatrix} i_{La}(t) \\ i_{Lb}(t) \\ i_{Lc}(t) \end{bmatrix} = \begin{bmatrix} \sum_{h\in H}^{H} I_{Lah} \sin(h\omega t + \alpha_{ah} - \phi_{ah}) \\ \sum_{h\in H}^{H} I_{Lbh} \sin(h(\omega t - 2\pi/3) + \alpha_{bh} - \phi_{bh}) \\ \sum_{h\in H}^{H} I_{Lch} \sin(h(\omega t + 2\pi/3) + \alpha_{ch} - \phi_{ch}) \end{bmatrix} \quad (11)$$

where,

$(V_{Lah}, V_{Lbh}, V_{Lch})$ = Peak values of the voltages at PCC corresponding to h^{th} order harmonics for phase-*a*, *b* and *c*.

$(I_{Lah}, I_{Lbh}, I_{Lch})$ = Peak values of the load currents corresponding to h^{th} order harmonics for phase-*a*, *b* and *c*.

$(\alpha_{ah}, \alpha_{bh}, \alpha_{ch})$ = Arbitrary angles of the PCC voltages and load currents corresponding to h^{th} order harmonics.

$(\phi_{ah}, \phi_{bh}, \phi_{ch})$ = Phase angles of the load currents corresponding to h^{th} order harmonics.

The load currents are converted into the d-q-0 frame using park's transformation as:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (12)$$

The three-phase PCC voltages are applied to three-phase phase locked loops (PLL) for obtaining the unit vectors and synchronizing the current signals with the voltages at PCC. The d-q component of load current consists with fundamental and harmonic components. The d-q components of load currents are then passed through a 5^{th} order low pass filters (LPF) to extract the dc components and block the harmonic component of load currents. The loss component of source current is calculated using dc-bus voltage PI controller. Actual dc-link and reference dc-link capacitor voltages are compared and difference is given to PI controller as shown in Fig. 3(b). The output of PI controller is considered as loss components of source current which is added with the direct axis

component i_{Ld} of the load currents. The output of PI controller is represented mathematically as:

$$i_{Loss(n)} = i_{Loss(n-1)} + K_{pd}(V_{dce(n)} - V_{dce(n-1)}) + K_{id}V_{dc(n)} \quad (13)$$

where, $V_{dce(n)} = V_{dcref} - V_{dc(n)}$ and $V_{dce(n-1)} = V_{dcref} - V_{dc(n-1)}$ are the error between reference dc-link capacitor voltage and actual voltage at n^{th} and $(n\text{-}1)^{th}$ sampling instant and K_{pd} and K_{id} are the proportional and integral constant for dc-bus PI controller. The output of this dc-bus PI controller is added with the dc component of load currents. Finally the fundamental value of DG current is subtracted to obtain the dc reference value of source currents as:

$$i_{sd}^{*} = i_{Ld(dc)} + i_{loss} - i_{cp} \quad (14)$$

Similarly, another PI controller is used to regulate the PCC voltages as shown in Fig.3 (b). The amplitude of the PCC voltages and their reference value are fed to a second PI controller whose output is represented mathematically as:

$$i_{q(n)}^{'} = i_{Loss(n-1)} + K_{pq}(V_{sme(n)} - V_{sme(n-1)}) + K_{iq}V_{sme(n)} \quad (15)$$

where, $V_{sme(n)} = V_{smref} - V_{sm(n)}$ and $V_{sme(n-1)} = V_{smref} - V_{sm(n-1)}$ are the error between peak value of reference grid voltage and actual grid voltage at n^{th} and $(n\text{-}1)^{th}$ sampling instant and K_{pq} and K_{iq} are the proportional and integral constant for the grid PI controller. The output of this PI controller is added with the quadrature axis component i_{Lq} of the load currents to obtain the reference quadrature component of the source currents as:

$$i_{sq}^{*} = i_{Lq(dc)} + i_{q}^{'} \quad (16)$$

The resultant current components (i_{sd}^{*}, i_{sq}^{*}) are converted into the reference currents using the reverse park's transformation as:

$$\begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) & 1 \\ \sin\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{2\pi}{3}\right) & 1 \\ \sin\left(\omega t + \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} i_{sd}^{*} \\ i_{sq}^{*} \\ i_{s0}^{*} \end{bmatrix} \quad (17)$$

The desired source currents are now compared with the actual load currents to obtain the compensating currents which include both active current supplied by the DG unit and reactive current requirement of the load.

$$[i_c(t)] = \begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} = \begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} - \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (18)$$

The compensating currents are now applied to the hysteresis controllers to obtain the switching pulses to switch the devices used in DSTATCOM inverter (DC-AC converter) configuration.

V. RESULTS AND DISCUSSION

The proposed controller of the DSTATCOM for DG-Grid interfaced system as shown in Fig. 3(a) is simulated under MATLAB/Simulink environment to show the performance characterestics of the controller. The performance of the DSTATCOM is simulated for forward and reverse interconnected mode of operation with variable load and DG power. Three single-phase uncontrolled rectifires with common neutral wire and R-L on there dc-side are used for unbalanced nonlinear loads. To fullfil the basic objectives of the study (DG active power transfer, load harmonics, reactive and neutral current compensation and PCC voltage regulation) the DSTATCOM is switched on at t = 0.1 s for all cases. Various simulation parameters used for this study are given in Table1.

Table:1 Simulation parameters used for the proposed DSTATCOM controller

Parameters	Values	Parameters	Values
V_s (Line) RMS	400 V, 50Hz	L_{sm} : R_{sm} per phase	0.5 mH : 0.05 Ω
$R_s : L_s$ per phase	0.01 Ω: 0.1 mH	K_{pq} : K_{iq} for voltage controller	0.3 : 0.75
R_c : L_c per phase	0.1 Ω: 2.0 mH	K_{pd} : K_{id} for dc-bus controller	0.15 : 0.5
C_{dc}	2000 µF	V_{dcref}	650 V

The discussion on the perofrmance of the DSTATCOM for different mode of operation are as:

a. *Forward Interconnected Mode with Variable Load and DG Power at Unity Power Factor*

In this case, the total active power requirement of the load P_L is more than DG active power capacity P_{dg} thus, the grid also supplies the active power of difference (P_L - P_{dg}) to the load. The DSTATCOM is switched on at t = 0.1 s and the load is changed from 17.72 kW to 23.98 kW at t = 0.25 s. The DG power is changed from 10 kW to 18.94 kW at t = 0.4 s and from 18.94 kW to 10 kW at t = 0.6 s. During t < 0.1s the total active power requirement of the loads P_L is supplied by the grid. Hence, the active power demand of the load is same as the active power supplied by the grid during t < 0.1 s. The three-phase grid voltage, load current, grid current and the DSATCOM currents are shown in Fig. 5. After t < 0.1 s the grid currents are in-phase with the respective grid voltages ensures the unity power factor compensation capabilities of the proposed DSTATCOM controller. Fig. 6 shows the phase-wise grid voltages (scaled by a factor of 0.2) and grid currents wherein the gird currents are in-phase with the respective phase voltages proves that reactive power is compensated completely. Also proves that the grid is supported to meet out the load active power demand. Apart from these the grid currents are balanced after t < 0.1 s. The values of the load, grid, and DG active powers for t < 0.1 s, 0.1 s < t < 0.25 s, 0.25 s < t < 0.4 s, 0.4 s < t < 0.6 s and t > 0.6 s are given in Table2 and the variations are shown in Fig. 7. The DSTATCOM energy storage dc-link capacitor supplies extra power during transient. The load and grid neutral currents are shown in Fig. 8 wherein, the grid neutral current is almost zero after t = 0.1 s. The FFT of the load and grid currents of all the phases for all durations are also carried out and the results are given in Table 2. A sample of load and grid currents waveform with harmonic spectrum for phase-*a* are shown in Fig. 9. The total harmonic distortion (THD) of the grid currents after compensation is well within the recommended limits shows the harmonic compensation capabilities of the controller.

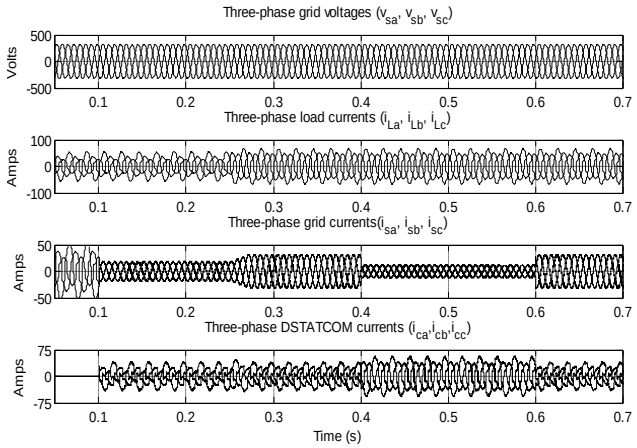


Fig. 5. Three-phase grid voltages, load currents, grid currents, and DSTATCOM currents in forward interconnected mode.

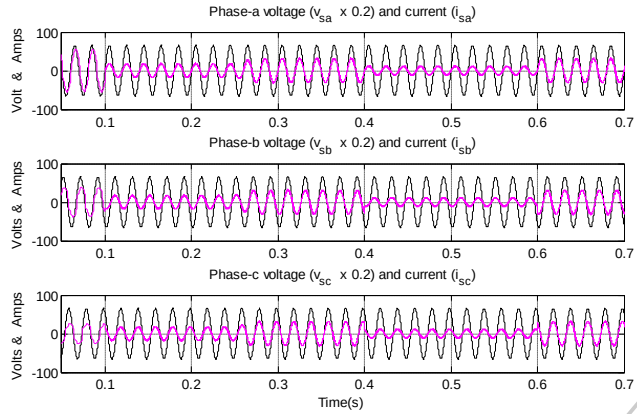


Fig.6. Phase-wise grid voltages (scaled by a factor of 0.2) and currents in forward interconnected mode.

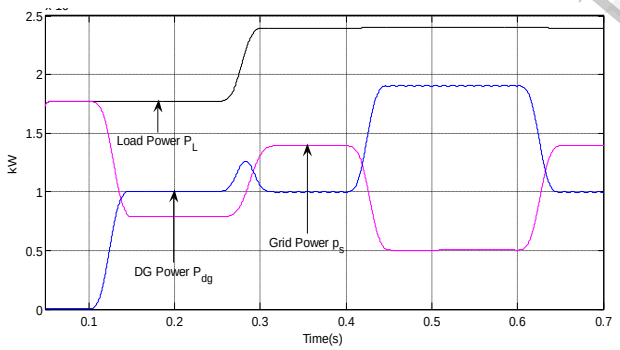


Fig. 7. Grid, load, and DG active powers

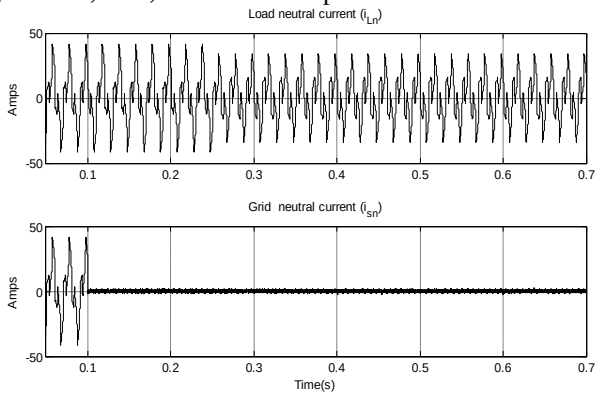


Fig.8. Load and grid neutral currents, in forward interconnected mode.

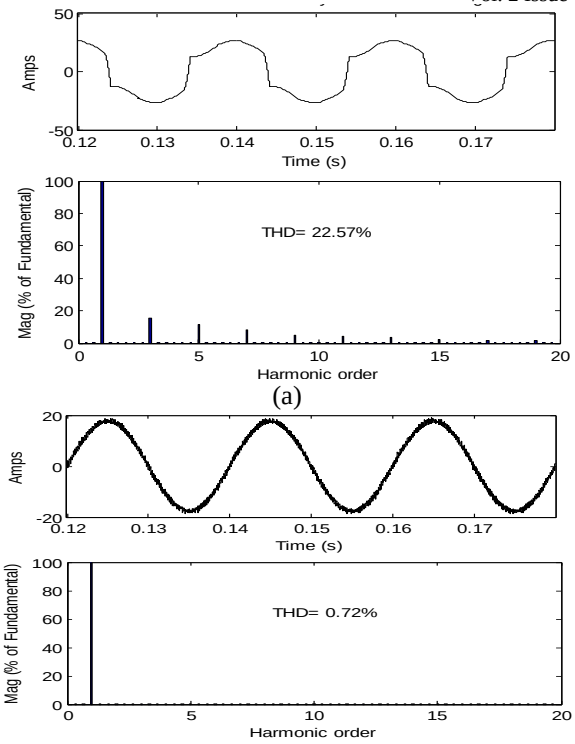


Fig. 9. THD of current waveforms for phase-*a* in forward interconnected mode. (a) Load current (b) Grid current.

5.3 Zero *Voltage Regulation Mode of Operation*

Fig.10 shows the voltage compensation capabilities of the proposed DSTATCOM controller. When a three-phase heavy load is connected at PCC without compensation the PCC voltage will reduced. A case of connecting such a load on PCC during 0.2 s to 0.4 s, results in reduction (sag) in magnitude of PCC voltages as shown in Fig. 10 (a). The DSTATCOM voltage PI controller senses the reduced voltage and accordingly generates extra reactive power $i_q^{'}$ to compensate the voltages at PCC. The compensated PCC voltages are shown in Fig. 10 (b). The other parameters are kept same as the previous case.

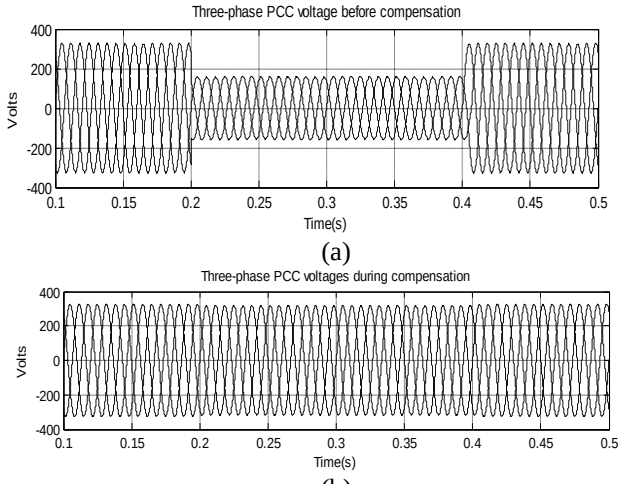


Fig.10. PCC voltages during application of heavy load (a) Without compensation (b) With compensation.

Table2: Simulated response for forward interconnected mode of operation with varying load and DG power

Parameters	Phase	$t < 0.1$s	0.1s$<t<$0.25s	0.25s$<t<$0.4 s	0.4s$<t<$0.6s	$t > 0.6$ s
RMS Load Currents(Amps)	A	40.68	40.68	48.49	48.49	48.49
	B	28.57	28.57	37.48	37.48	37.48
	C	20.17	20.17	34.17	34.17	34.17
	N	04.02	04.02	03.29	03.29	03.29
RMS Grid Currents(Amps)	A	40.68	12.46	22.10	7.984	22.10
	B	28.57	12.46	22.05	7.975	22.05
	C	20.17	12.45	22.05	7.975	22.05
	N	04.02	0.005	0.003	0.003	0.003
Load Current % THD	A	16.08	16.08	13.58	13.58	13.58
	B	19.76	19.76	15.46	15.46	15.46
	C	22.57	22.57	17.82	17.82	17.82
Grid Current % THD	A	16.08	00.70	0.44	0.88	0.44
	B	19.76	00.74	0.47	0.83	0.47
	C	22.57	00.72	0.47	0.86	0.47
Three-phase Load Power (kW)		17.72	17.72	23.98	23.98	23.98
Three-phase DG Power (kW)		10.00	10.00	10.00	18.94	10.00
Three-phase Grid Power (kW)		17.72	07.71	13.95	05.00	13.95

VI. CONCLUSION

This paper proposed the application of DSTATCOM as in interface between distributed generation and utilities three-phase four-wired distribution system. The proposed DSTATCOM system is capable for injecting energy to electric grid while compensating load power factor, harmonics and neutral currents, load balancing and provide voltage regulation at PCC. The grid system currents are sinusoidal and in-phase with their respective voltages. The grid current THD after compensation are well within the IEEE 519-1992 recommended limits. The proposed controller is suitable for islanding as well as integrated connected (both forward and reverse) mode of operation under unbalanced and distorted grid voltages conditions. The regulation in PCC voltages during any change is also quite satisfactory. The simulation results show that the proposed DSTATCOM control system is suitable for islanding as well as integrated mode of operation to improve power quality.

REFERENCES

[1]T. Ackerman, G. Anderson and L. Soder, "Distributed generation: a definition," *Electric Power System Research*, vol. 57, pp. 195-204, 4/20, 2001.

[2] G. Venkataramanan, M. Illindala, "Microgrids and sensitive loads," *IEEE Power Engineering Society Winter Meeting*, vol. 1, pp. 315-322, 2002.

[3] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398-1409, October 2006.

[4] W. Kramer, S. Chakraborty, B. Kroposki, and H. Thomas, "Advanced power electronic interfaces for distributed energy systems, Part 1: systems and topologies," *Technical Report NREL*/TP-581-42672, March 2008.

[5] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems." *IEEE Transactions on Power Electronics*, vol. 19, no.5, pp. 1184-1194, September 2004.

[6] C. C. Chen, Y. Y. Hsu, "A novel approach to the design of a shunt active filter for an unbalanced three-phase four-wire system under nonsinusoidal conditions," *IEEE Transactions on Power Delivery*, vol. 15 no. 4, pp. 1258–1264, 2000.

[7] G. W. Chang, "A new approach for optimal shunt active power filter control considering alternative performance indices," *IEEE Transactions on Power Delivery*, vol. 21, no. 1, pp. 406-413, January 2006.

[8] M. C. Benhabib and S. Saadate, "New control approach for four-wire active power filter based on the use of synchronous reference frame," *Electric Power Systems Research*, vol. 73, no. 3, pp. 353-362, March 2005.

[9] M. I. Milanes, E. R. Cadaval and F. B. González, "Comparison of Control Strategies for shunt active power filters in three-phase four-wire Systems," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 229-236, January 2007.

[10] B. Singh, S. Gairola, B. N. Singh, A. Chandra and K. Al-Haddad, "Multipulse AC-DC converters for improving power quality: a review," *IEEE Trans. on Power Electronics*, vol. 23, no. 1, pp. 260-281, January 2008.

[11] P. S. Sensarma, K. R. Padiyar, V. Ramanarayanan, "Analysis and performance evaluation of a distribution STATCOM for compensating voltage fluctuations," *IEEE Transaction on Power Delivery*, vol. 16, no. 2, pp. 259-264, 2001.

[12] Electromagnetic compatibility part 3:2: Limits – Limits of harmonic current produced by equipment to public low voltage systems with input current >16A and ≤ 75A per-phase, IEC 61000-3-12, April 2005.

[13] H. Fugita and H. Akagi, "Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system," *IEEE Trans. on Power Electronics*, vol. 22, no. 1, pp. 1046-1053, May 2007.

[14] B. N. Singh, P. Rastgoufard, B. Singh, A. Chandra and K. Al. Haddad, "Design, simulation and implementation of three pole/ four pole topologies for active filters," *IEE Electric Power Appl*ications, vol. 151, no. 4, pp. 467-476, July 2004.

[15] E. Acha, V. G. Agelids, O. Anaya-Lara, T. J. E. Miller, "Power electronic control in electric systems," *Newness Power engineering series, 1st Edition*, Oxford, 2002.

[16] S. Choi and M. Jang, "Analysis and control of a single-phase- inverter-zigzag transformer hybrid neutral-current suppressor in three-phase four wire systems," *IEEE Transactions on Industrials Electronics*, vol. 54, no. 4, pp. 2201- 2208, August 2007.