CMOS SRAM Circuit Design and Layout using Parametric Analysis

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***Abstract*—Memories are widely used as an embedded element rather than an individual component. Design of memory needs to address all the issues such as speed, power consumption, area etc. In this paper, optimization of the layout area is the main objective. A 64x32 SRAM is designed with indestructible read and write and reduced layout area in a 45nm node. A 6T-SRAM with a tall cell configuration is used as the basic building block of the memory. A 32 bit wide data is read from and written into the memory.**

Keywords—64x32 SRAM; reduced layout area; indestructible read and write ; 6T-SRAM.

I. INTRODUCTION

In the past few decades, we have witnessed a rapid development in CMOS technology in which memory has been a driving force. In any digital system, memories are an essential building block. Therefore the key considerations in designing a memory are more vital. Majority of the die area is occupied by the microprocessors and application specific integrated circuits which consist of large arrays of SRAM. Maintaining the balance between the performance and cost of such chips is a challenging task for the designers. System performance is boosted by faster and larger arrays of SRAM. But this has negative impact on layout area which in turn increases the chip cost. Hence a large number of SRAM cells are packed tightly which makes it one of the densest circuit on the chip.

II. 6T-SRAM

A. β-ratio

β-ratio is defined as the ratio of width of PMOS to width of NMOS. On the basis of parametric analysis a β-ratio of 1 is obtained as shown in Fig 1. Therefore a minimum width of NMOS and PMOS of 120nm is maintained throughout the SRAM layout in a 45nm node.

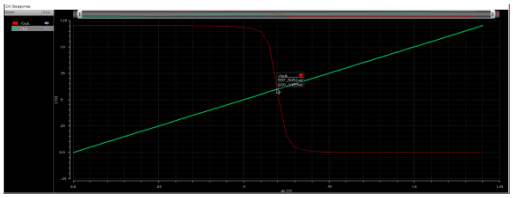


Fig. 1. βratio using Parametric Analysis

B. 6T-SRAM bit cell

Two cross coupled inverters are used as a memory storage element along with two NMOS access transistors to provide access to read and write into the memory as shown in the Fig 2 These access transistors are activated by the word line.

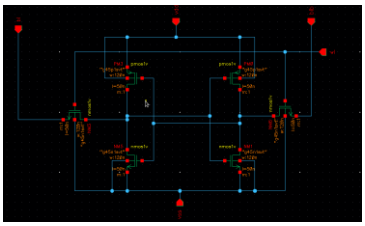


Fig. 2. 6T SRAM Schematic

32 such bit cells are abutted in a single row to read or write a 32 bit wide data. Similarly 64 such rows are abutted with shared VDD and VSS to obtain a 2K bit SRAM array with reduced area. The height and width of one bit cell is 1.275µm and 1.17µm respectively. The layout of a 6T SRAM bit cell is as shown in the Fig 3

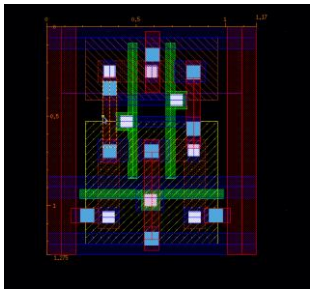


Fig. 3. 6T SRAM Layout

III. DECODER

A 6:64 decoder is used to address 64 rows with 6 address lines. The decoder leaf cell consists of two 3 input NAND gates and one 3 input NOR gate in order to reduce the fan in as shown in the Fig 4. 64 such decoder leaf cells are used which activate one particular word line depending upon the combination of address lines.

The output of the decoder aligns with the word line of the bit cell. The height of the leaf cell is maintained same as that of the bit cell to share the supply voltages with the respective bit array row. The decoder leaf cell layout is as shown in the Fig 5.

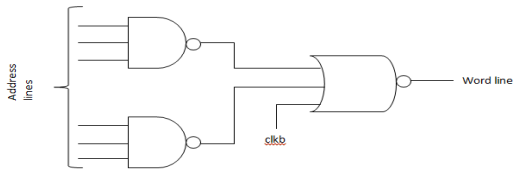


Fig. 4. Decoder Leaf Cell Logic Diagram

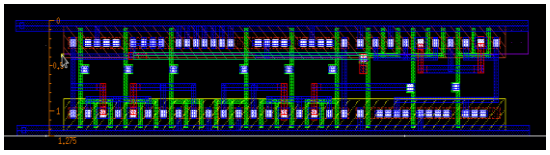


Fig. 5. Decoder Leaf Cell Layout

IV. IO SECTION

The input output section of a SRAM consist of a write amplifier and a sense amplifier to write and read respectively. The sense and write amplifiers are designed in the width of 1 bit cell to reduce area.

A. *Write amplifier*

Write amplifier is activated when a write operation has to be performed. It consists of 2 NMOS pass transistors which are activated by a wsel control signal as shown in the Fig 6. The input and its inverted form is written into the bit and bit bar of the bit cell through write drivers having equal delay. 32 such write amplifiers are abutted to write 32 bit data at a time. The layout of a write amplifier leaf cell is as shown in the Fig 7

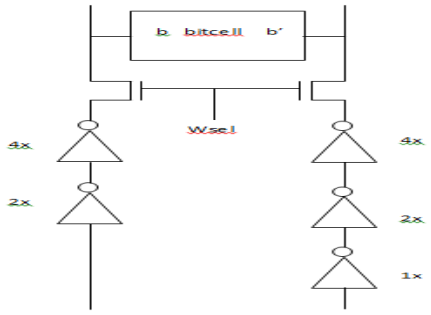


Fig. 6. Write Amplifier Logic Diagram

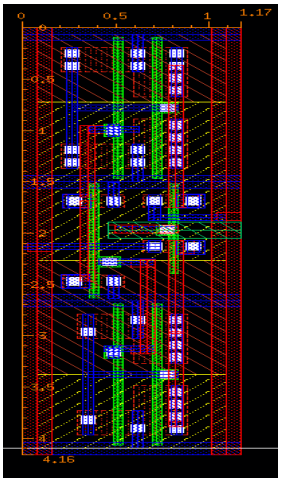


Fig. 7. Write Amplifier Leaf Cell Layout

B. *Sense amplifier*

Sense amplifier is activated when a read operation has to be performed. The primary function is to amplify a small voltage difference developed on the bit lines by read accessed cell. It consists of a NAND latch whose output is ANDed with wen control signal as shown in the Fig 8.32 such sense amplifiers are abutted to read 32 bit data at time. The layout of a sense amplifier leaf cell is as shown in the Fig 9.

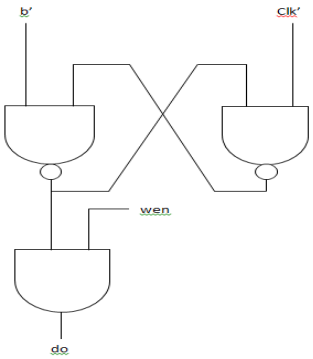


Fig. 8. Sense Amplifier Logic Diagram

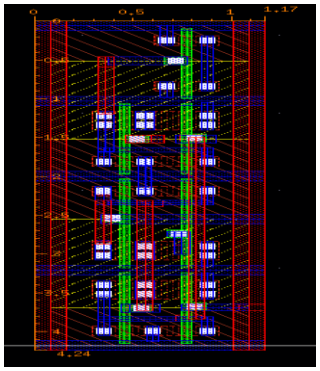


Fig. 9. Sense Amplifier Leaf Cell Layout

V. CONTROL SECTION

The control section consists of control signals wen and clk. These signals control the read and write operation of the entire memory. Read or write operation is performed only when the clock signal is active high, otherwise the data is latched. When the wen signal is active high the data is read and when active low the data is written.

A write select generator generates a wsel signal which activates the write amplifier. It consists of an MS DFF that latches the wen signal. The output of MS DFF serves as an input to the AND gate along with clk signal to generate wsel signal as shown in the Fig 10. The layout of MS DFF is designed with minimum area considerations as shown in the Fig 11.

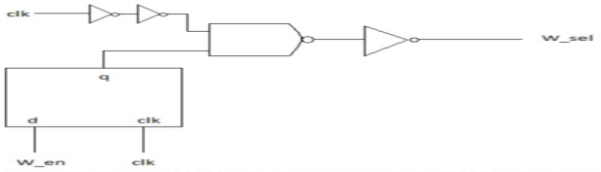


Fig. 10. WSEL Generator Logic Diagram

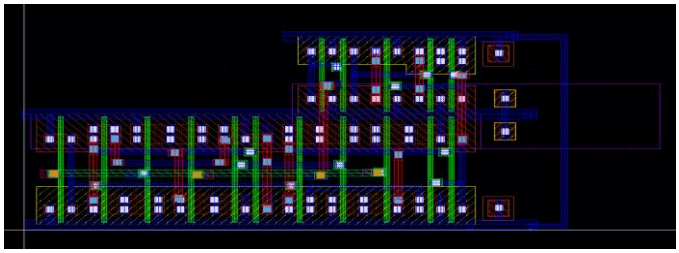
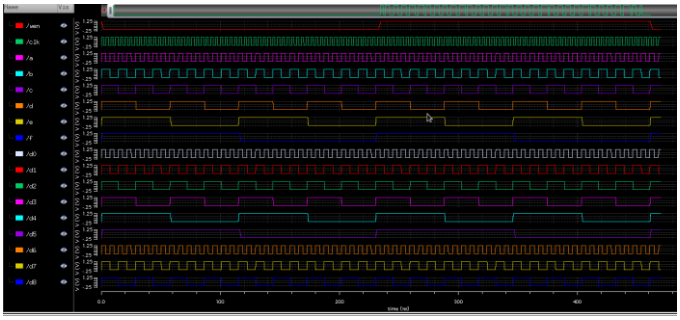


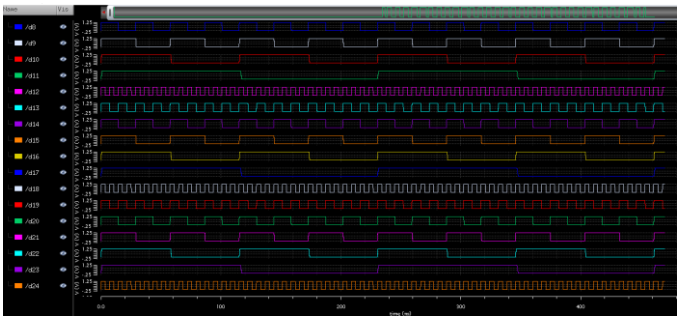
Fig. 11. WSEL Generator Layout

VI. SIMULATION AND RESULT

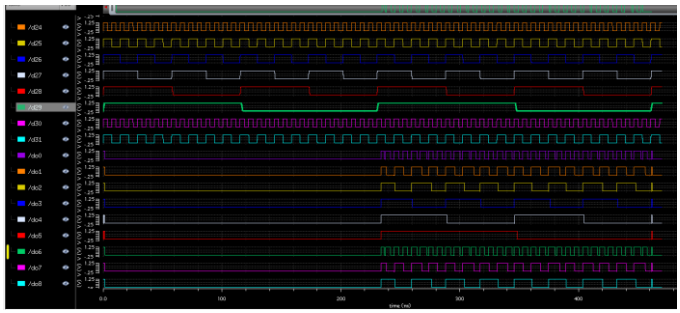
For a clock frequency of 250 MHz the simulation waveforms are as shown below. The overall area of the SRAM memory with clean DRC and LVS is 4.505nm^2.



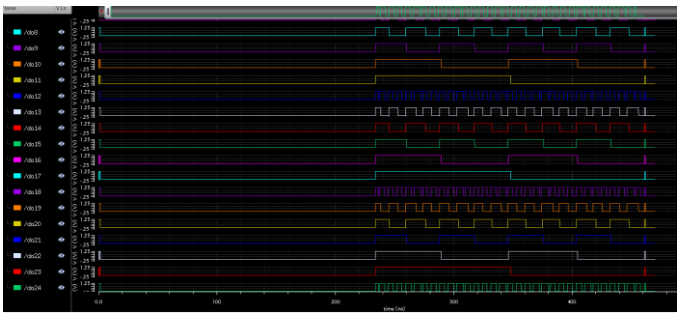
(a)



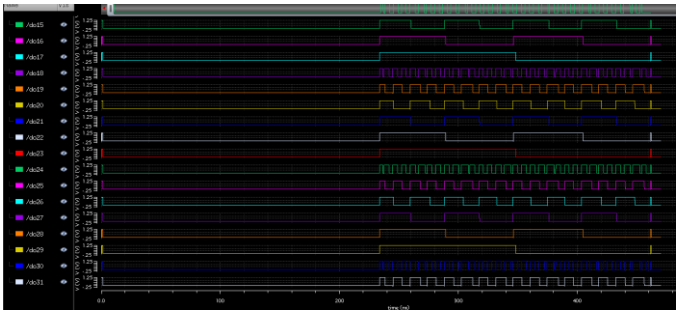
(b)



(c)



(d)



(e)

Fig. 12. Schematic Simulation

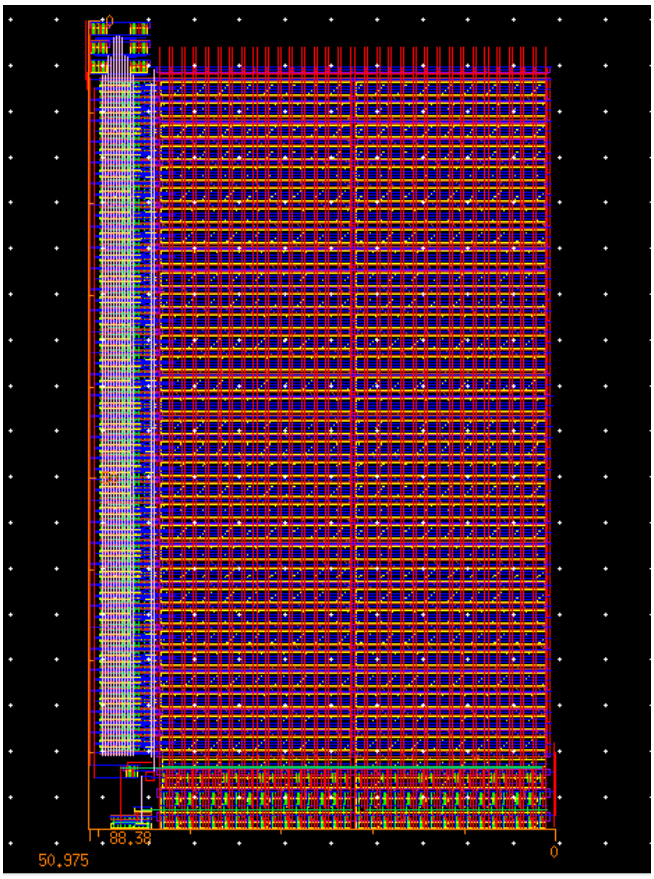


Fig. 13. SRAM Layout

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