Published by :
http://www.ijert.org
International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Volume 13, Issue 12, December 2024

CMOS-Based RF Energy Harvesting using a Novel Rectifier-Amplifier Circuit with Dickson's Topology and Integrated LDO

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***Abstract*: This article focuses on the design, simulation, and optimization of an efficient MOSFET-based RF energy harvesting system using Dickson's topology rectifier, followed by a pmos based error amplifier and LDO(Low Dropout Voltage Regulator), implemented in 180nm CMOS technology. The primary objective is to create an energy harvesting system capable of converting low-power RF signals—such as those emitted by WiFi routers—into a stable DC output. The system employs a microstrip patch antenna resonating at 2.4 GHz to capture ambient RF energy. The circuit achieves an output voltage of 3.65 V from an input RF signal of just 1 V, demonstrating a high-efficiency energy conversion suitable for low-power applications. This work has potential applications in powering IoT devices and other battery-less, energy-efficient systems.**

***Keywords*—RF-energyHarvesting,Rectifier-Amplifer-circuit, Dickson's topology, CMOS, Integrated LDO, Antenna**

I. INTRODUCTION

The present scenario of power generation for making the latest technological gadgets and systems work such as Internet-of-Things (IoTs)-like wireless sensors, or other tiny computing machines is encountering problems related to power supply. Batteries are no longer a good choice due to their short life-spans, hazards of explosivity. Batteries with longer life-span and devices with safer charging modes are the needs of the hour. In this connection one can think of harvesting energy in the IoT environment it self as well as from the surrounding environment. Of late many alternate energy sources are being probed for a profitable use at a micro-level that are cleaner with least risk associated with them. RF energy harvesting is one amongst them. Many notable technologies have come into existence in this area. Tapping the possible sources of ambient energy (RF) especially from the surrounding electromagnetic field though yields a weaker potential still plays a significant role in this regard. An electromagnetic field harvester generally comprises four blocks to convert radio-frequency (RF) energy to direct-current (DC) energy, namely an antenna, a matching network, a rectifier and a voltage converter. Shape of the antenna, topology of matching network, rectifier or voltage converter, or combination of functions are some of the variables that can be studied to come out with systems that are suitable for developing technologies involving simple to complex systems.

Recent works on RF-energy harvesting have come out various trapping devices, rectifier circuits and other amplifier devices. A review of radio-frequency energy harvester (RFEH) design is given in in the overview by Mouapi, A. [1]. Most RFEHs have been considered for a frequency range below 5 GHz, though microwave applications have been reported recently [2]. The major metrics of performances are the minimum input RF power that can start-up the EH system, the open-voltage at the targeted input RF power level and the effective efficiency when the rectenna is loaded with an impedance equal to its internal impedance (optimal load condition) [3].

Radio-frequency electromagnetic waves can be harnessed to produce an alternative source of energy to replace batteries in many low-power device applications. Beragama Vithanageet al[4] came out with an efficient radio frequency (RF) energy harvesting circuit was designed and constructed using a dynamic Pi-matching network in order to convert frequency-modulated electromagnetic waves in the range of 88-108 MHz to direct current through a 3-step process. The circuit consisted of a 50 Ω copper plate dipole antenna, a Pi impedance matching network, and a five-stage voltage doubler circuit. These three modules are connected through SubMiniature version A (SMA) connectors for convenient assembly. Eid, A.; Costantine et al [5], Bahhar, C[6] came out with suitable antenna systems for efficient RF-energy harvesting systems.Xuan Viet Linh Nguyen et al came out with 3D plastronics Radio Frequency Energy Harvester on Stereolithography Parts and also rapid 3D plastronics[7,8]. Gu, X et al designed a Zero-bias-diode-based rectifier using temperature difference[9]. Stoopman, M et al came out with a Design of a CMOS Rectifier and Small Loop Antenna for

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Volume 13, Issue 12, December 2024

Highly Sensitive RF Energy Harvesters[10]. According to the review by Husam Hamid Ibrahim et al[11] Radio frequency energy harvesting (RF-EH) is a potential technology via the generation of electromagnetic waves since this advanced technology offers the supply of wireless power that is applicable for battery-free devices, which makes it a prospective alternative energy source for future applications. the review also stressed the abundant source of RF-EH from the surroundings sources, including nearby mobile phones, Wi-Fi, wireless local area network, broadcast television signal or DTS, and FM/AM radio signals. In contrast, the energy is captured by a receiving antenna and rectified into a working direct current voltage.

It is very clear that the RF-EH technology can significantly revolutionize the power generation to meet the needs of internet based technologies. The energy harvesting circuits depend on cutting-edge electrical technology to achieve significant efficiency, given that they are built to perform with considerably small current and voltage.

CMOS stands for Complementary Metal-Oxide-Semiconductor, a technology used to make digital devices, memory chips, and computer processors. CMOS is a type of semiconductor technology that uses metal-oxide-semiconductor field-effect transistors (MOSFETs) to create electronic circuits. Complementary metal-oxide semiconductor (CMOS) is a fabrication technology for semiconductor systems that can be used for the construction of digital circuitry, memories and some analog circuits. The technology is based on the pairing of two metal oxide semiconductor field effect transistors (MOSFET), one of which is a p-type and the other an n-type transistor. The term metal oxide semiconductor is a reference to the traditional structure of the device where there would be a metal gate on top of an oxide layer on top of a semiconductor. Today, the metal layer is replaced by a polysilicon layer most of the time. The PMOS transistor or P-channel metal oxide semiconductor is a kind of transistor where the p-type dopants are utilised in the channel or gate region. This transistor is exactly the reverse of the NMOS Transistor. These transistors have three main terminals; the source, the gate & the drain where the transistor's source is designed with a p-type substrate, and the drain terminal is designed with an n-type substrate. In this transistor, the charge carriers like holes are responsible for the conduction of current.

Return loss, S11, and voltage standing wave ratio (VSWR) are all parameters that measure the performance of an antenna or transmission line: Return loss and VSWR are two important measures of efficient power transmission and both of them can be interconverted to obtain the value of one another. Just by entering the return loss the VSWR can be obtained using this calculator.

Formula:

$$\text{VSWR} = \frac{1+10^{\frac{-RL}{20}}}{1-10^{\frac{-RL}{20}}}$$

Where RL = Return Loss

Return loss (S11): A measure of the amount of power reflected by a transmission line or antenna. It's also known as the reflection coefficient. Return loss is expressed as a negative value in decibels (dB), such as -10 dB. A higher return loss is better, as it indicates that the devices or lines are well-matched.

Voltage standing wave ratio (VSWR): A measure of the ratio of the peak voltage amplitude to the minimum voltage amplitude of a wave on a transmission line. A VSWR of 1 is ideal, as it means there's no reflected power at the antenna port. S11 as input VSWR: A VNA measures S11 and converts it to input VSWR.

The far field radiation pattern of an antenna describes how the antenna radiates electromagnetic energy:

The far field is the region of space farthest from the antenna where the electromagnetic radiation is established. The far field is also known as the radiation zone or Fraunhofer region. In the far field, the radiation pattern is independent of distance from the antenna. The electric and magnetic fields are orthogonal to each other, and the radiation is similar to plane waves. The radiated power decreases as the square of the distance from the antenna. The far field's distance from the antenna is affected by the antenna's size and frequency. The higher the frequency, the further away the far field will be.antenna parameters are usually measured in the far field. Analyzing patterns include MATLAB and Simulink to plot antenna far-field patterns at multiple frequencies on the same graph.

Ambient RF energy harvesting is related to a case of low RF power. In this condition, the expected DC voltage at the rectenna output is quite low and supplying a (low-power) circuit requires at least 1 V as an order of magnitude with respect to CMOS electronics. Energy harvesting system capable of converting low-power RF signals especially those emitted by WiFi routers in the surrounding environment into a stable DC output are the need of the hour. Hence this RF-energy harvester is designed wherein a CMOS based specifically MOSFET-based RF energy harvesting system using Dickson's topology rectifier is designed to trap the RF and it is further fed to a pmos based error amplifier and LDO(Low Dropout Voltage Regulator). The novel technology comprises of implementing in a 180nm CMOS technology**.**The system employs a microstrip patch antenna resonating at 2.4 GHz to capture ambient RF energy. Hence for the current design of RF-EH using CMOS technology comprising of MOSFETs are employed and similarly PMOS based LDOs and error amplifiers are employed to tap the electromagnetic energy associated with the RF associated with the WIFI routers for powering IoT based systems with the help of a microstrip patch antenna possessing copper annealed substrate. The efficiency of the designed RF- EH is evaluated in terms of the generally adhered parameters for evaluating the efficiency of the antenna and the energy transmission such as Return loss, S11, and voltage standing wave ratio (VSWR). The RF-EH thus fabricated is tested under specific conditions of the system to come out with its efficiency as the suitable RF energy harvester

II. FORMULATIONS AND EQUATIONS FOR ANTENNA DESIGN

The antenna is designed taking FR4-lossy(as mentioned in the CST Studio library), with an ε(permittivity) of 4.3,for a resonating frequency of f0 = 2.4 Ghz.
The width of the patch antenna is obtained using the formula

$$W = \frac{c}{2f_o\sqrt{\frac{\varepsilon_R+1}{2}}} \quad (1)$$

From here we obtain a value of W= 37.8mm
To calculate effective permittivity ε(eff) , the below formula is used

$$\varepsilon_{eff} = \frac{\varepsilon_R+1}{2} + \frac{\varepsilon_R-1}{2}\left[\frac{1}{\sqrt{1+12\left(\frac{h}{W}\right)}}\right] \quad (2)$$

Assuming height of substrate h to be 1.6mm and W= 37.8mm as calculated above ,gives an ε(eff) of 3.31

$$L = \frac{c}{2f_o\sqrt{\varepsilon_{eff}}} - 0.824h\left(\frac{(\varepsilon_{eff}+0.3)\left(\frac{W}{h}+0.264\right)}{(\varepsilon_{eff}-0.258)\left(\frac{W}{h}+0.8\right)}\right) \quad (3)$$

From the equation(3) we find that the Length of substrate comes out to be 29mm

The impedance of the antenna comes out as 310 ohm,the inset feed line impedance is taken as standard 50 ohm, according to these values the depth of the inset feed line is calculated using the below formula

$$D = \frac{L}{\pi}\cos^{-1}\left(\sqrt[4]{\frac{Z_{Feedline}}{Z_{Antenna}}}\right)$$

Hence D = 8.16mm

III. METHODOLOGY

The RF energy harvesting system design began with a microstrip patch antenna,which is subjected to optimization by performing experiments so as to enable the microstrip antenna resonate at 2.4 GHz for capturing ambient RF energy from sources like WiFi routers. Simulation studies were conducted using CST Studio Suite 2023 Lite, across a frequency range of 1 GHz to 3 GHz. The microstrip antenna comprised of a FR-4 lossy substrate.FR-4 lossy substrate was selected for its cost-effectiveness, easy-availability and reliable performance at 2.4 GHz, with standard annealed copper used for the patch to ensure high conductivity. The simulation parameters included a hexahedral mesh configuration with Number of cells in each direction to be Nx = 73, Ny = 51, and Nz = 24. The characteristics evaluated included Return loss(S11), Voltage Standing Wave Ratio(VSWR) ,and farfield radiation patterns.The rectifier-amplifier circuit was developed in Keysight ADS. The Dickson topology rectifier, designed with 180nm CMOS technology and transient analysis was performed for a 1V RF input at 2.4 GHz to yield a stable DC output. This rectifier stage was followed by a PMOS-based LDO with an error amplifier to regulate the output voltage. Finally, the antenna hardware was implemented and tested using a Vector Network Analyzer(VNA) to validate S11 parameters.

A. Dickson topology CMOS Rectifier

The Dickson topology CMOS rectifier circuit is given in Figure 2. The Dickson topology CMOS rectifier comprises of two MOSFETs numbered 16 and 17 designed to work at 180nm which falls with in the natural band with for RF. The rectifier circuit is constructed as given in figure 2 wherein the circuit works out at 1V RF input at 2.4 GHz to yield a stable DC output. The lengths and widths of the MOSFETs were 0.4um, and 40um for MOSFET16, 120um for MOSFET 17. MOSFET 16 was CMOSN type and MOSFET 17 was CMOSP type.The rectifier circuit used in this paper is a single-stage dickson topology rectifier. In a multistage model , biasing happens with reference to the previous stage, whereas in a single-stage rectifier, self-biasing works as follows: the input RF signal drives the diode-connected MOSFET (DCM), which allows current to flow and charge the capacitor during the positive peaks of the signal, creating a DC voltage across the capacitor that acts as a reference for subsequent conduction cycles, ensuring continuous rectification.

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International Journal of Engineering Research & Technology (IJERT)
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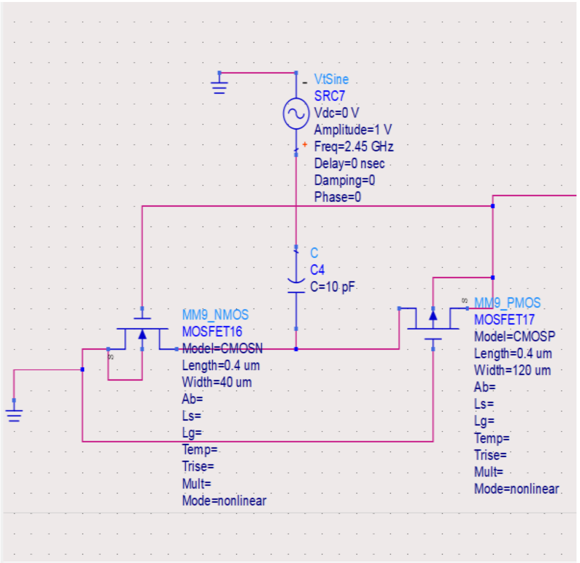

Figure 2. Dickson topology CMOS Rectifier

B. Microstrip Patch antenna

The microstrip patch antenna is constructed using FR4-lossy(as mentioned in the CST Studio library), with an ε(permittivity) of 4.3,for a resonating frequency of f0 = 2.4 Ghz. The optimal width is calculated according to equation (1) and it is found to be 37.8mm. Assuming the height of substrate h to be 1.6mm and taking the optimal width W as 37.8mm the effective permittivity ε(eff) for the microstrip antenna is calculated according to equation (2) as given previously and it is found to be equal to 3.31 ε(eff) .T he Length of substrate of the microstrip patch antenna is calculated as per equation (3) and it is found to be equal to 29mm. The impedance of the antenna is found to be equal to 310 ohm. The inset feed line impedance is kept at standard 50 ohm, and accordingly the depth of the inset feed line is calculated and it is found to be equal to 8.16mm. The microstrip patch antenna thus constructed for the RF- EH is given in Figure1.

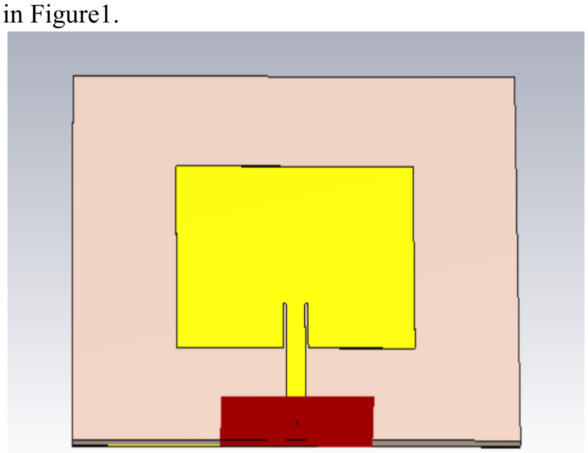

Figure 1. Microstrip Patch Antenna
Substrate : FR4-Lossy
Patch,Ground : Copper Anealed

C. Error Amplifier and PMOS based LDO

The electrical energy thus captured using microstrip patch antenna and rectified using Dickson topology rectifier is directly fed to the PMOS based low voltage dropout regulator (LDO) further comprising the error amplifier circuit to obtain a steady DC voltage. Here, Rectifier stage is followed by a PMOS-based LDO with an error amplifier to regulate the output voltage. The PMOS-based LDO comprises of MOSFETs 11-15 as given in Figure 4. , with length 1 µm and width 15 µm The error amplifier circuit is depicted in Figure 3. It comprised of a grid comprising of 8 MOSFETs.

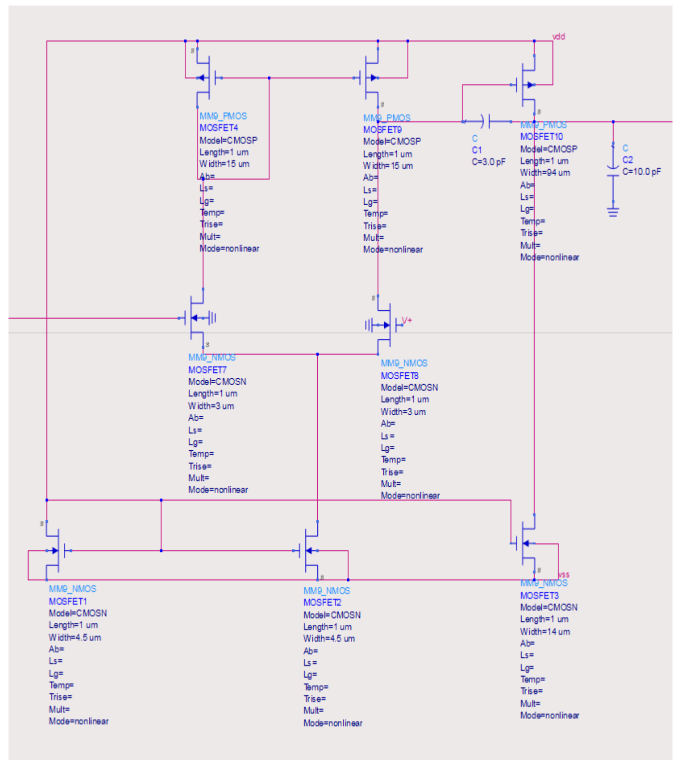

Figure 3. Error amplifier

D. Final Circuit

The overall RF-EH design thus comprising the microstrip patch antenna connected to Dickson topology rectifier, PMOS based LDO combined with the error amplifier to work at 2.4 GHz for capturing ambient RF energy from sources like WiFi routers is depicted in Figure 5.

E. Antenna simulation Results

The microstrip antenna comprising of a FR-LOssy ground patch with copper annealed substrate that can resonate at 2.4 GHz for capturing ambient RF energy from sources like WiFi routers is subjected to simulation studies. Simulation studies were conducted using CST Studio Suite 2023 Lite, across a frequency range of 1 GHz to 3 GHz. The simulation parameters included a hexahedral mesh configuration with Number of cells in each direction to be Nx = 73, Ny = 51, and Nz = 24 . The characteristics evaluated included Return loss(S11), Voltage Standing Wave Ratio(VSWR) ,and farfield radiation patterns The results are depicted in Figure 6

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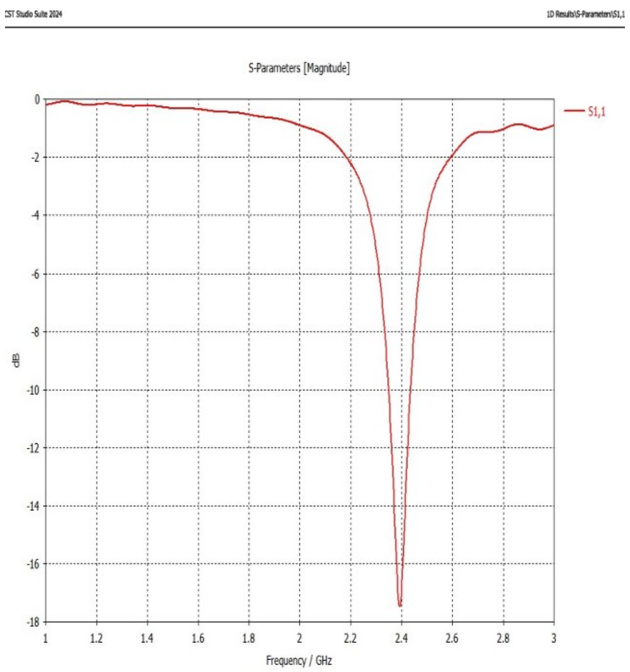

. Figure 6 .\S11 Parameter result of microstrip antenna

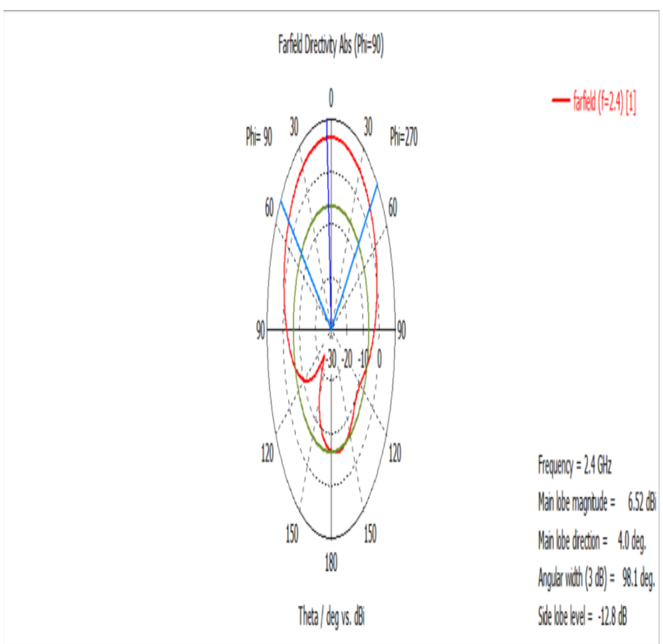

Figure 7. Farfield results of Antenna

F. Far field antenna results

Since far field radiation pattern of an antenna describes how the antenna radiates electromagnetic energy, the microstrip patch antenna thus designed based on Dicksons topology analysis is subjected far field metric study. The far field's distance from the antenna is affected by the antenna's size and frequency and the higher the frequency, the further away the far field will be. Hence antenna parameters are measured in the far field by analyzing patterns by plotting antenna far-field patterns at multiple frequencies on the same graph using MATLAB and Simulink and the same is given in Figure 7.

G. Fabrication and testing of the RF-EH

Figures 8 and 9 depict the fabricated microstrip patch antenna and the antenna S11 testing using Vector network analyzer.

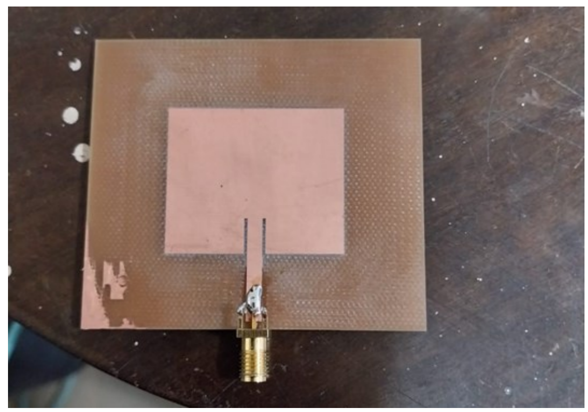

Figure 8. Fabricated microstrip antenna

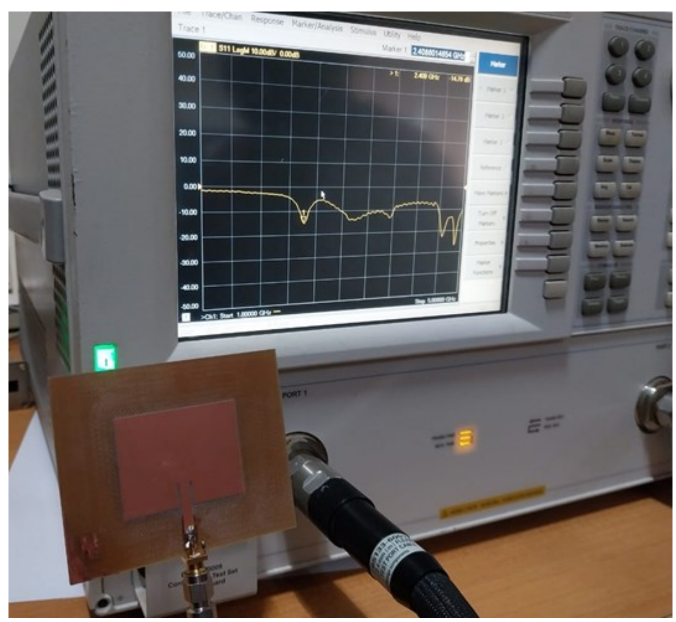

Figure 9. Antenna S11 testing using Network Analyzer

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Volume 13, Issue 12, December 2024

H. Simulation of the fabricated CMOS based RF- EH and testing using S11 antenna.

The microstrip patch antenna designed consisting of a Dickson topology rectifier, designed with 180nm CMOS technology that worked at 1V RF input at 2.4 GHz to yield a stable DC output and a PMOS-based LDO with an error amplifier to regulate the output voltage is subjected to simulation studies to validate S11 parameter using a Vector Network Analyzer(VNA) and the results are given in Table 1. The results clearly indicate the efficacy of the RF energy harvester in terms of the output voltage which stood at 3.65V for an input voltage 1V at a miller capacitance of 3pf when the reference voltage of the LDO was 1.2V

I. Simulation and analysis results for CMOS rectifier-amplifier circuit Vector Network Analyzer(VNA) to validate S11 parameters

Table 1. Simulation and analysis results for CMOS rectifier-amplifier circuit

Parameters	Values
Input Voltage	1 V
Output voltage	3.65 V
Reference voltage for LDO	1.2 V
Miller Capacitance	3pf

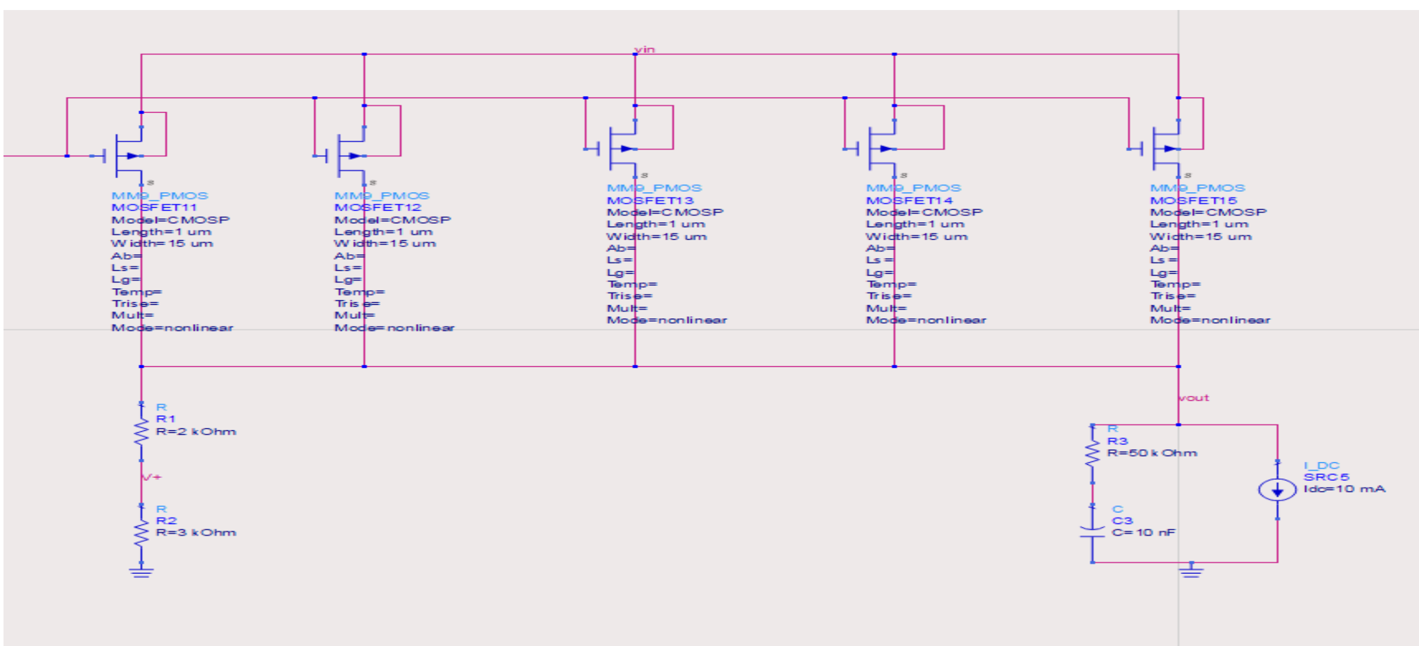

Figure 4. PMOS based LDO

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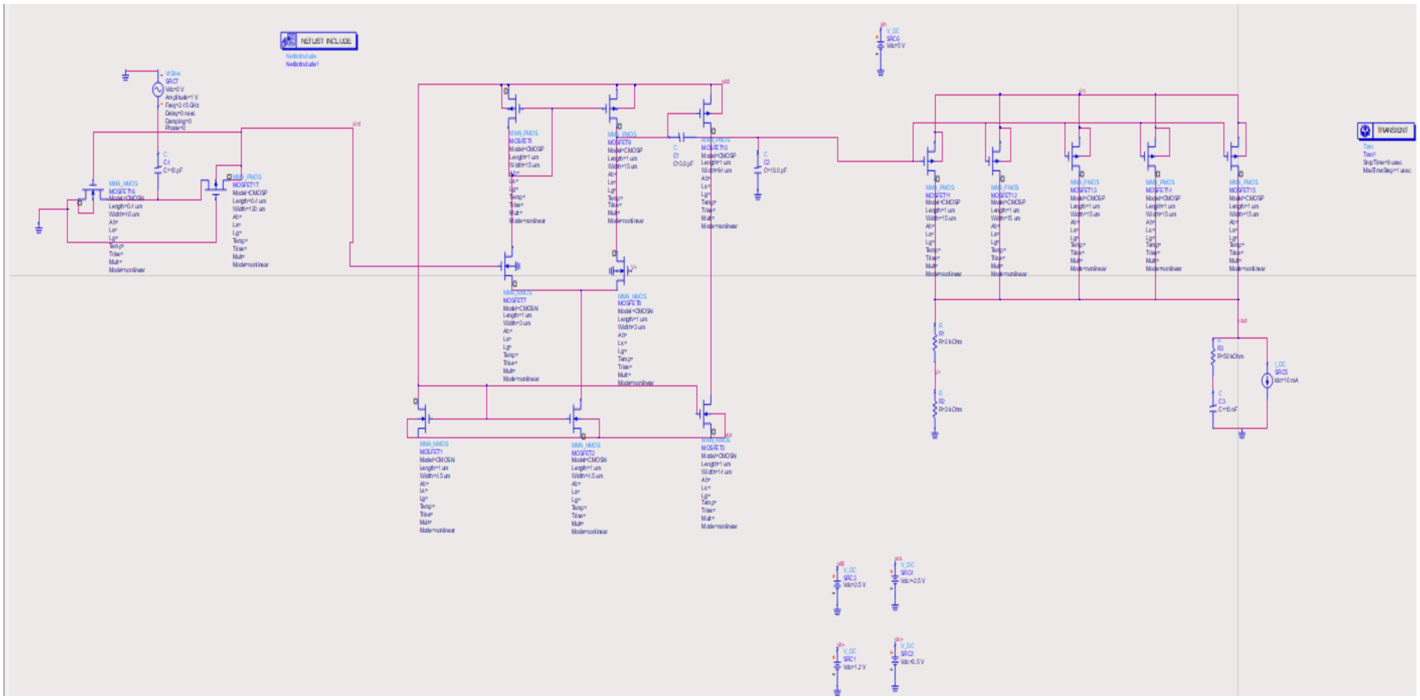

Figure 5. Final Circuit Fabrication and testing

IV. RESULTS AND DISCUSSION

The design of the CMOS-based RF-EH using Dickson topology rectifier resulted in a working RF energy harvester using ambient RF from the ambient WiFi routers that can power IoT applications. The studies included the optimization of an efficient MOSFET-based RF energy harvesting system using Dickson's topology rectifier,followed by pmos based error amplifier and LDO(Low Dropout Voltage Regulator), implemented in 180nm CMOS technology. The primary objective to create an energy harvesting system capable of converting low-power RF signals—such as those emitted by WiFi routers—into a stable DC output is achieved by constructing a microstrip patch antenna using FR-Lossy substrate with copper annealed patch. The system employs a microstrip patch antenna resonating at 2.4 GHz to capture ambient RF energy. The circuit achieves an output voltage of 3.65 V from an input RF signal of just 1 V, demonstrating a high-efficiency energy conversion suitable for low-power applications. The antenna simulation studies evaluated Return loss(S11), Voltage Standing Wave Ratio(VSWR) ,and farfield radiation patterns over a frequency range of 1GHz to 3 GHz clearly established the efficiency of RF energy harvester.

V. CONCLUSION

The CMOS-based RF energy harvester comprising of the microstrip patch antenna and rectifier-amplifier circuit based on Dickson topology and integrated LDO could create an energy harvesting system capable of converting low-power RF signals—such as those emitted by WiFi routers—into a stable DC output. The circuit achieves an output voltage of 3.65 V from an input RF signal of just 1 V, demonstrating a high-efficiency energy conversion suitable for low-power applications. The designed RF energy harvester has potential applications in powering IoT devices and other battery-less, energy-efficient systems.

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VII. ACKNOWLEDGEMENT

One of the contributing authors Siddhardha Sreeramagiri expresses his deep gratitude to NITK, Suratkal for providing excellent facilities for carrying out this work. Thanks are due to the HOD, ECE, NITK, and technical staff for their assistance. I profusely thank my mother and mentor Dr.T Bhavani(Consultant IP, Sravathi Advance Process Technologies Pvt. Ltd., Bengaluru) for helping me prepare the manuscript.

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