Closed Loop Control of Three Phase Multilevel Inverter for Photovoltaic System

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***Abstract*—In this paper harmonic reduction of three phase diode clamped multilevel inverter for grid connected solar system is analyzed. Solar system is controlled and maximum power is obtained by fuzzy based MPPT technique. Sinusoidal Pulse Width Modulation (SPWM) is used to control the three phase three level and five-level inverter and the simulation is achieved through MATLAB/Simulink. The results of the three phase three-level and five-level inverter are compared and low THD rate is achieved for high level inverter.**

Keywords—three phase three level and five-level inverter, SPWM, THD, Solar system, FLC.

I. INTRODUCTION

Energy demand is the major problem today. So, we are in a situation to use alternate energy source. Renewable energy sources put a path in alternate energy sources. There are numerous energy sources like solar power, wind power, tidal power and geothermal energy power. Here, solar power is considered. PV generation has numerous advantages like emitting noise; fuel costs and maintenance; it does not cause pollution [1]. The PV system operates at its highest efficiency at maximum power point. The amount of power generated by a PV generator depends on operating voltage of the PV array.

The maximum power operating point changes with insolation level and temperature [2]. Maximum power is tracked from the PV array by several techniques. These techniques are named as MPPT techniques such as perturbation & observation, incremental conductance, parasiticcapacitance, constantvoltage, neural network and fuzzy logic control have been proposed to extract maximum power from the PV array [3]. In this paper FLC is used to track the MPPT from the PV array. Design of fuzzy is simple and the implementation is cheap and good. The output is fast and accurate. The output of PV array is connected to inverter [4].

Multilevel voltage source inverter is recognized as an important alternative to the normal two-level voltage source inverter especially in high voltage applications. Instead of using one converter to convert an AC current into a DC current, a multilevel inverter uses a series of semiconductor power converters thus generating higher voltages. The multilevel inverter is more powerful, it provides energy in higher-power situations. Thus, multilevel inverters are suitable for high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum [5]. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. The other attractive features of the multilevel inverter are staircase waveform quality, common mode voltage, input current, switching frequency.

Multilevel inverter has several topologies like diode clamped multilevel inverter, flying capacitor multilevel inverter, and cascaded inverter with different DC sources. Neutral Point Clamped (NPC) or Diode clamped multilevel inverter topology is employed in this paper due to their benefits such as: limit voltage stress; the capacitors need to filter only the high-order harmonics of the clamping diodes currents, low-order components intrinsically cancel each other; switching frequency can be low; reactive current and negative phase sequence current can be controlled.

Abundant modulation techniques have been introduced for control of inverter like Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse width Modulation (SVPWM) Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) [6]. Among all techniques Sinusoidal Pulse Width Modulation (SPWM) is used here.

II. SOLAR ARRAY

Solar array is the combination of solar cells connected either in series or parallel type. Series connections are responsible for increasing the voltage of the module whereas the parallel connection is responsible for increasing the current in the array [7]. A solar cell can be modeled by a current source and an inverted diode connected in parallel to it. It has its own series and parallel resistance. Series resistance is due to hindrance in the path of flow of electrons and parallel resistance is due to the leakage current. This model is shown in fig.1. In this PV array of KC200GT is used. KC200GT has following specifications: maximum power-200W; maximum power voltage-26.3V; maximum power current-7.61A.

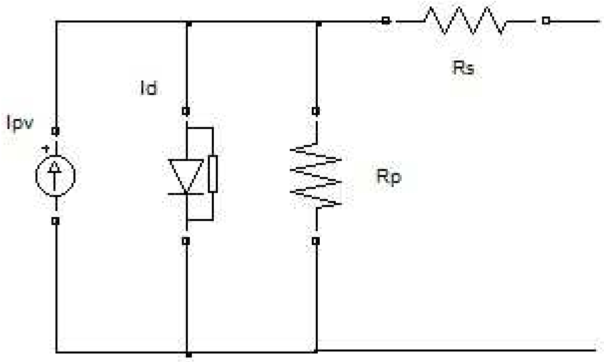

Fig 1.Equivalent circuit of a solar cell

The basic current equation of solar array is

$$I = I_{sc} - I_d \qquad (1)$$

where

$$I_d = I_o(e^{qv_d/kT} - 1) \qquad (2)$$

From (1) and (2),

$$I = I_{sc} - I_o\left(e^{qv_d/kT} - 1\right) \qquad (3)$$

where,

I_o is reverse saturation current of diode.
I_{sc} is short circuit current.
q is electron charge.
$v_d$is voltage across diode.
k is Boltzmann constant.
T is junction temperature in kelvin.

As sunlight strikes a solar cell, the incident energy is converted directly into electrical energy without any mechanical effort. Transmitted light is absorbed within the semiconductor by using its energy to excite free electrons from a low energy status to an unoccupied higher energy level. When a solar cell is illuminated, excess electron-hole pairs are generated by light throughout material hence the p-n junction is electrically short circuited and current will flow.

The incidence of light on the cell generates charge carriers that originate an electric current if the cell is short circuited [8]. $I - v$and$P - v$ characteristics of the solar cell [9], [10] are determined by MATLAB which is described below in fig.2. Maximum power point (MPP) is obtained from the PV curve and Isc is short circuit current, Voc is open circuit voltage.

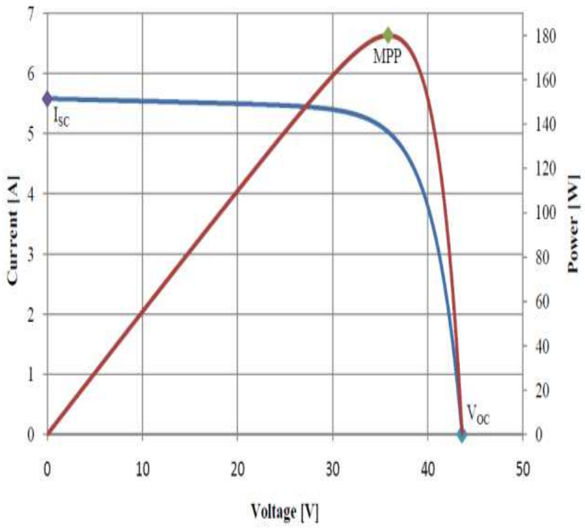

Fig.2.P-V and I-V characteristics of solar cell

Fill factor (FF) is widely used to measure the solar cell overall quality. It is the ratio of the actual maximum power ($I_{MPP}V_{MPP}$) to the theoretical one ($I_{SC}V_{OC}$), which is not obtainable. The reason for that is that the MPP voltage and current are always below the open circuit voltage and the short circuit current respectively, because of the series and shunt resistances and the diode depicted in fig.1. The typical fill factor for commercial solar cell is usually over 0.70.

$$FF = \frac{I_{MPP}V_{MPP}}{V_{OC}I_{SC}} \qquad (4)$$

where,

I_{MPP} is maximum power point current.
V_{MPP} is maximum power point voltage.
V_{OC} is the open circuit voltage.
ISC is the short circuit current.

III. MPPT CONTROL

MPPT is a technique used to track the maximum power from the solar panel. MPPT algorithms are necessary because solar arrays have nonlinear voltage-current characteristics with a unique point where the power produced is maximum [11]. One of the computational methods which have demonstrated fine performance under different environmental operating conditions is the fuzzy based maximum power point tracking technique. This technique is used here as a MPPT control technique. FLC depend on shape of the membership functions and the rule base, not on the complex mathematical model. A Mamdani fuzzy logic controller has been proposed to perform the MPPT, this kind of controller areusually used in feedback controlmode,because they are simple, present low sensibility to noise in the input.

Basically FLC has three parts namely: Fuzzification, Inference Engine and Defuzzification.

A. Fuzzification

In fuzzification the conversion process of crisp set into linguistic fuzzy sets using fuzzy membership function takes place. The membership function is a curvature that describes each point of membership value in the input space [12]. Membership functions are assigned as Negative Big $(-ve\ B)$, Negative Medium $(-ve\ M)$, Negative Small $(-ve\ S)$, Zero, Positive Small$(+ve\ S)$, Positive Medium $(+ve\ M)$, and Positive Big $(+ve\ B)$.

The value of input error E (k) and change in error CE (k) are normalized by an input scaling factor. The input scaling factor has been designed such that input values are between -1 and 1. Membership functions have many structures; among those triangular memberships function is used shown in fig.3 because for any particular input there is only one dominant fuzzy subset. Fuzzy rule base is the basic function of fuzzification. Fuzzy rule base for these seven linguistic variables is shown in table. I.

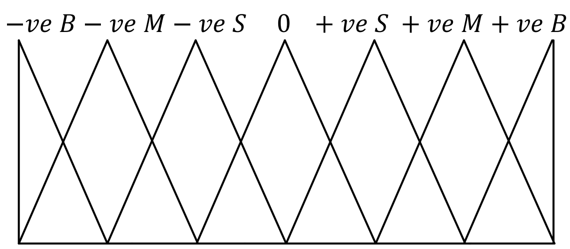

Fig.3 Input and output membership function for fuzzy

TABLE I. FUZZY RULE BASE

E(k)	CE(k)						
	−veB	***−veM***	***−veS***	***Zero***	***+veS***	***+veM***	***+veB***
−veB	−veB	−veB	−veB	−veB	−veM	−veS	zero
−veM	−veB	−veB	−veB	−veM	−veS	zero	+veS
−veS	−veB	−veB	−veM	−veS	zero	+veS	+veM
zero	−veB	−veM	−veS	zero	+veS	+veM	+veB
+veS	−veM	−veS	zero	+veS	+veM	+veB	+veB
+veM	−veS	zero	+ves	+veM	+veB	+veB	+veB
+veB	zero	+veS	+veM	+veB	+veB	+veB	+veB

B. Inference Engine

Using If-Then type fuzzy rules converts the fuzzy input to the fuzzy output. Fuzzy inference engine is an operating method that formulates a logical decision based on the fuzzy rule setting and transforms the fuzzy rule base into fuzzy linguistic output.

Syntax for IF and THEN rules

The fuzzy rules are written as

If <fuzzy proposition> *then* <fuzzy proposition>

C. Deffuzification

The last step in the FLC process is the defuzzification, which takes the implied fuzzy set from the inference engine and transforms it back to a real crisp output. The Center Of Gravity (COG) defuzzification method is used [13].

IV. MULTILEVEL INVERTER

A multilevel power converter structure has been used in high power and medium voltage situations. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment [14]. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. An m-level NPC inverter has m-1 capacitors on the DC bus. These capacitors are used as a filter circuit. The voltage across each capacitor isV_{dc}, and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. Fig.4 represents the circuit diagram for three phase five-level inverter. The switches are triggered by switching states [15].Three phase five-level inverter has eight switches in each phase and each switch has parallel diode to avoid reverse conduction.

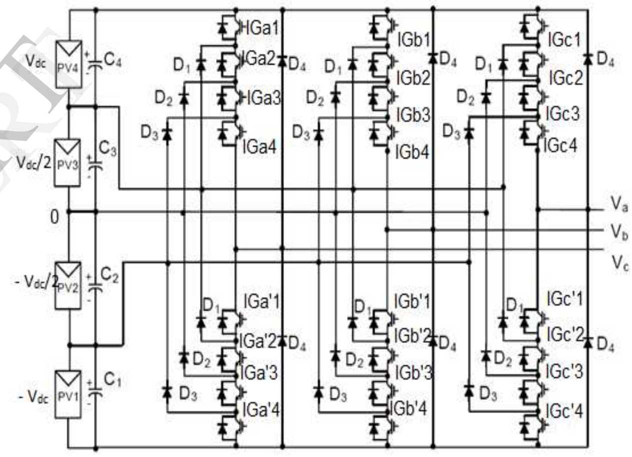

Fig.4 circuit diagram of three phase five-level inverter

Each phase has four complementary pairs that is turning on one of the switches of the pair; require that the other switch of that pair to be off. The complementary pair of phase c is (IGc1, IGc'1), (IGc2, IGc'2), (IGc3, IGc'3), (IGc4, IGc'4). Here switches are denoted by IGx1.IG indicates the switch IGBT, x denotes the phase of the inverter and the last numeric term denotes the position of the switch in the x phase. The switching table for the circuit shown in fig.4 is indicated in table.II. Switch condition 0 means OFF state and 1 indicates ON state. In general for an m-level inverter m-1 switches should be ON at any given time. The m-level NPV inverter has an m-level output phase voltage and a 2(m-1) level output line voltage. The number of diodes required for each phase would be 2(m-2).

TABLE II. SWITCHING STATES OF THREE PHASE FIVE LEVEL INVERTER FOR PHASE c

Switching states	IGc 1	IGc 2	IGc 3	IGc 4	IGc' 1	IGc' 2	IGc' 3	IGc' 4
	1	1	1	1	0	0	0	0
	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
	0	0	0	1	1	1	1	0
	0	0	0	0	1	1	1	1

The clamping diodes are used to block the reverse voltage. For example if the negative sides of phase c are ON means, the D1 diode block , D3 diode blocks .

Sinusoidal pulse width modulation is one type of modulation technique used to trigger the switches. It is obtained by two signals called sine wave called as reference signal and triangular wave called as carrier signal. By comparing these two signals pulses are obtained. Pulse width of the pulses is varied according to the area of the two signals. When sinusoidal wave has magnitude higher than the triangular wave, the comparator output is high, otherwise low which is shown in figure.5.

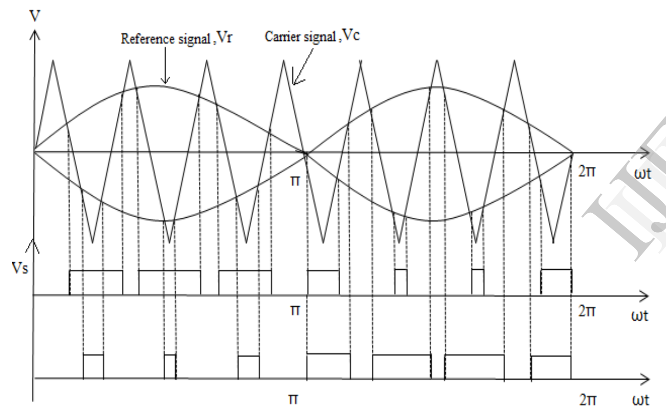

Fig.5 sinusoidal pulse width modulation technique

The comparator output is processed in a trigger pulse generator in such a manner that the output voltage wave of the inverter has a pulse width in agreement with the comparator output pulse width. Sinusoidal signal amplitude determines the modulation factor [16]. Modulation factor is given by

——(5)

where A_m denotes the maximum value of reference voltage ( ) and A_c is peak to peak value of triangle wave ( ).
To maintain the low total harmonic distortion, the modulation index should be maintained between 0 and 1.For three-level inverter four triangular wave signals are compared with one reference signal. Pulse width of thepulses is varied according to the area of the two signals.

———(6)

V. MATLAB SIMULATION RESULTS

The simulation results of three phase three level and five-level inverter are compared in terms of THD rate. The modulation technique used is SPWM. The shape of the output voltage of the inverter is determined by the modulating index. The block diagram of the inverter circuit is shown in fig.6.

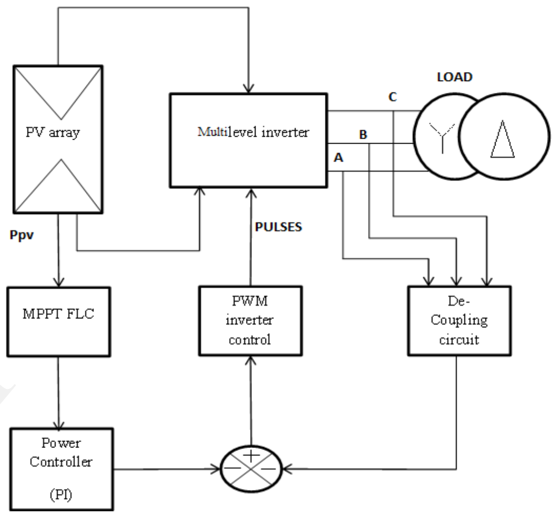

Fig.6 Block diagram of inverter circuit

The three phase three level inverter is simulated and the line voltage is presented in fig.7

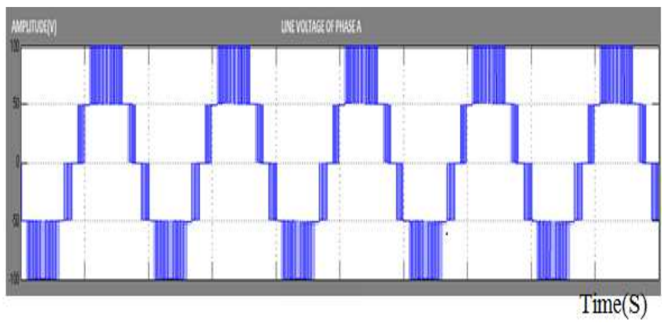

Fig.7 line voltage of three phase three level inverter of phase

It is clear from the graph that the voltage has three- level from reference line. These levels vary as the level of multilevel inverter is varied. The voltage shown on fig.8 has five levels from the reference line as it is a three phase five level inverter.

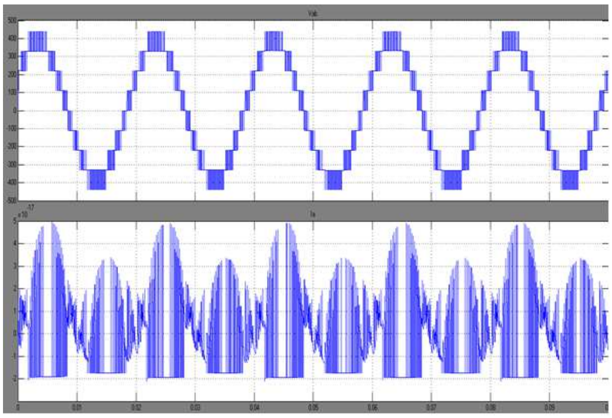

Fig.8 voltage and current waveforms for three phase five-level inverter

Now, three phase three level inverter and five level inverter are compared and this paper clears the concept that high level inverter has low THD rate. The THD values of three phase three level inverter for both open loop and closed loop is shown in figs 9 and 10.

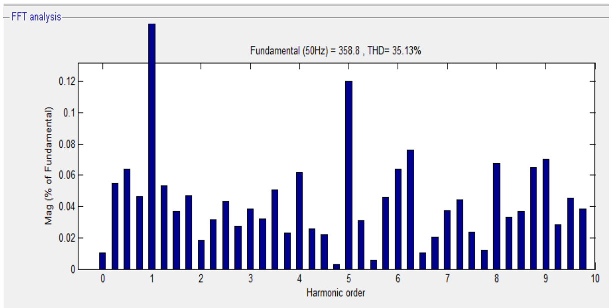

Fig.9 Open loop FFT analysis of three phase three level inverter

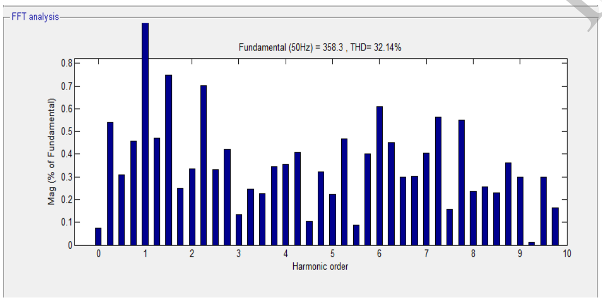

Fig.10 Closed loop FFT analysis of three phase three level inverter

The THD rate of three phase three level inverter is about 35.13% and 32.14% for open loop and closed loop. Controllers reduce the harmonics in the inverter circuit for better performance. The THD rate of three phase five level inverter is presented in figs.11 and 12 for open loop and closed loop.

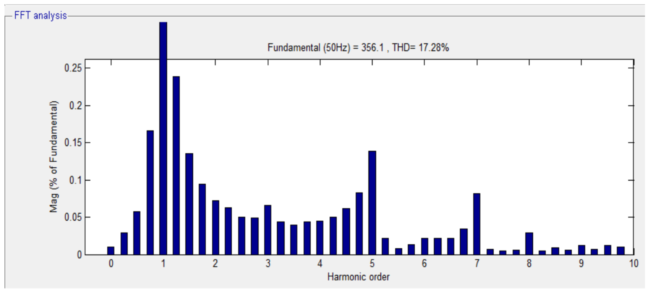

Fig.11 Open loop FFT analysis of three phase five level inverter

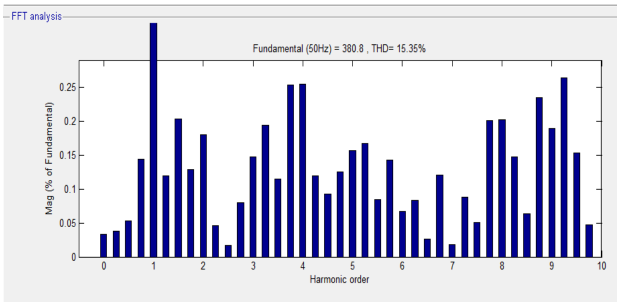

Fig.12 Closed loop FFT analysis of three phase five level inverter

For three phase five level inverter also closed loop THD rate i.e.15.25% is low when compared to open loop THD rate i.e.17.28%.

TABLE.III. THD COMPARISON

SL.NO	NO.OF LEVELS	THD% (OPEN LOOP)	THD% (CLOSED LOOP)
1	3	35.13	32.14
2	5	17.28	15.35

VI. CONCLUSION

In this paper three phase three-level and five- level inverter is discussed for sinusoidal pulse width modulation technique and concludes that the THD rate is low for high level multilevel inverter. Three phase three level inverter has THD rate of about 35.13% and 32.14% for open loop and closed loop respectively. THD rate of three phase five level inverter for open loop and closed loop is 17.28% and 15.35%. From these values it is concise that the THD rate goes on decreasing when levels are increased in multilevel inverter. And also FLC works well while tracking the maximum power from the solar array. Since it is applicable to nonlinear system the performance is good.

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