

Characterization of Nanoscale MOSFETs using Analytical Technique

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Abstract: A novel RF-MOSFET (Radio Frequency Metal Oxide Semiconductor Field Effect Transistor) model with PTM (Predictive technology model) for 90 nm CMOS (Complementary Metal Oxide Semiconductor) technology is presented. A simple and accuracy method is developed to directly extract all the high frequency parasitic effect from measured S-parameter biased at zero and linear region. This model is proposed to overcome some of short channel effects at nano-scale highly doped drain and source based on the conventional small signal MOSFET (Metal Oxide Semiconductor Field Effect Transistor) equivalent circuit, RF (RadioFrequency) characterization of CMOS (Complementary Metal Oxide Semiconductor) has been taken up. The excellent correspondence is achieved between simulated and measured S-parameter (Scattering parameter) from 1GHz to 10 GHz frequency range. Silvaco TCAD (Technology Computer Aided Design) tool is used to describe this model.

Keywords: Nanoscale complementary metal-oxide-semiconductor characterization, Parameter extraction using analytical method.

I. INTRODUCTION

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{dD} , x_{dS}) of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise.[1]

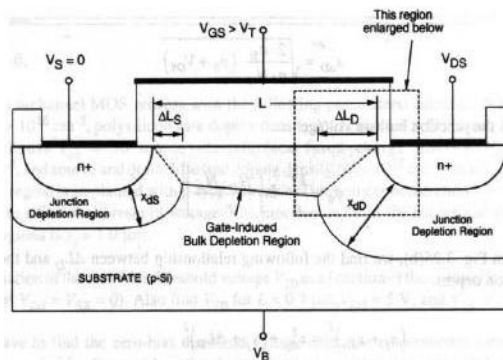


Fig.1 Cross-section of a typical advanced MOSFET [1]

For CMOS RFIC development, developing circuits at high frequency and low voltage becomes a challenge, especially

since most of the MOSFET models are not designed for either low voltage or high frequencies. Undesired interaction with a low resistivity substrate adds to the task of designing RF circuit on CMOS processes [2],[3],[4],[5]. Device characterization and modeling at RF frequencies is necessary to allow accurate prediction of circuit performance prior to fabrication. The ultimate goal in modeling is a versatile model with few parameters (less than 20 parameters) and good performance in all region of operation including high frequency operation.[5],[6],[7].

In order to overcome the drawback of previously reported approaches, a novel model is presented to accurately predict the high frequency behavior of RF-MOSFET [4],[5]. A typical advanced MOSFET is shown in Fig.1. The complete new equivalent circuit small signal RF-model is shown in Fig.2.

RF characterization of CMOS has been taken up based on their respective small signal model. By doing Y- or Z-parameter analysis of their respective model and analytical procedure for parameter extraction has been developed and presented here.[4],[5]

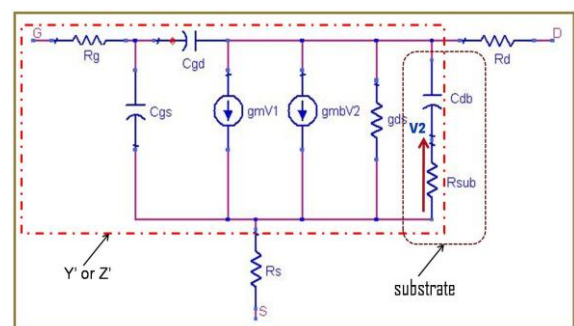


Fig. 2 Small signal RF Model [5]

The small signal RF model of Fig.2 has been used for analysis and the Y & Z parameters have been found in terms of the circuit parameters. The parameters are Gate resistance (R_g), drain resistance (R_d), source resistance (R_s), gate-to-drain capacitance (C_{gd}), drain-to-base capacitance (C_{db}), gate-to-source capacitance (C_{gs}), drain-to-source transconductance (g_{ds}), and the substrate parameters i.e. substrate resistance (R_{sub}), substrate capacitance (C_{db}). [5],[6],[7],[8].

II. SPECIFICATION OF 90 nm TECHNOLOGY NODE OF PTM MODEL OF CMOS:[9]

Table-1

Nano- CMOS: Technology node: 90 nm NMOS						
L_{eff}	T_{ox}	V_{dd}	V_{th}	R_{dsw}	I_{on}	I_{off}
35 nm	1.4 nm	1.2 V	0.2 V	180 $\Omega/\mu m$	1100 ($\mu A/\mu m$)	50 (nA/ μm)

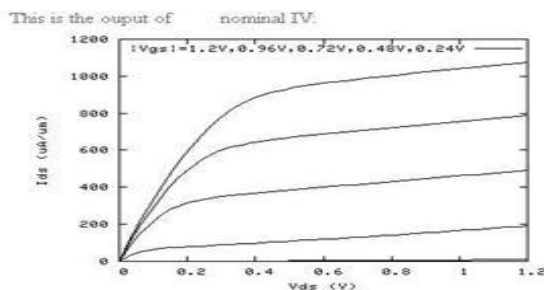


Fig.3 Output characteristics of generated 90nm NMOS

III. RF MODEL DEVELOPMENT

To have an efficient design environment, design tools with accurate models for devices and interconnect parasitics are essential. It has been known that for analog and RF applications the accuracy of circuit simulations can be strongly determined by the device models. Accurate device models become crucial to correctly predict the circuit performance.[6]

For a model to describe the device characteristics accurately, all important model parameters should be extracted from the actually Fabricated NMOS device [10]. The RF model development steps are shown using a flowchart shown in Fig.4

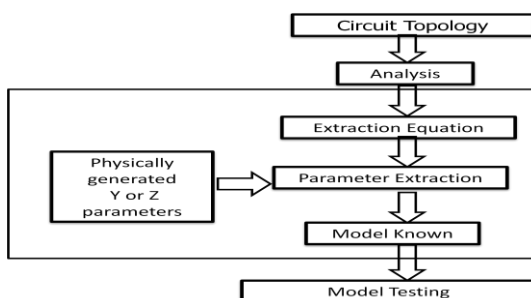


Fig. 4 Flowchart for Model Development [6]

IV. FABRICATION OF NANOSCALE MOSFET

Here fabrication of nanoscale MOSFET is performed using ATLAS(SILVACO) TCAD tool. LDD (Lightly Doped Drain) is used to overcome device degradation short channel effects.[6],[11],[12] And improved a lot but still have a chance of improvement. Heavily doped drain and source, lightly doped drain and source extensions and lightest doping of gate. The device structure of fabricated NMOSFET is shown in Fig.5.

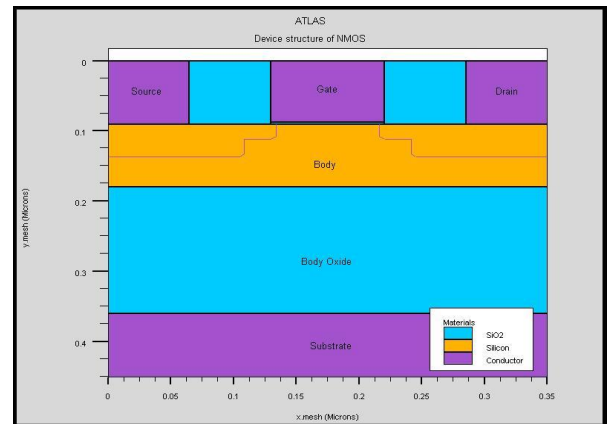


Fig.5 Device Structure of Fabricated MOSFET [10]

V. ANALYSIS AND PARAMETER EXTRACTION

The equivalent small signal RF model is shown in Fig. 2. Circuit analysis of the small signal RF model yielded the following results.

In the frequency ranges $\omega \ll [R_g (C_{gs} + C_{gd})]^{-1}$

and $\omega \ll [L_g (C_{gs} + C_{gd})]^{-1}$, a simplified

expression for small signal Y-parameters Y'_{11} , Y'_{21} ,

Y'_{12} , and Y'_{22} of the circuit enclosed by dashed line in Fig. 2. can be derived as: [5],[6][7].

A. Y-parameters

$$Y'_{11} \cong \omega^2 R_g (C_{gs} + C_{gd})^2 + j\omega (C_{gs} + C_{gd}) \quad (1)$$

$$Y'_{21} \cong g_m - j\omega C_{gd} \quad \dots \dots \dots (2)$$

$$Y'_{12} \cong -j\omega C_{gd} \quad \dots \dots \dots (3)$$

$$Y'_{22} \cong g_{ds} + j\omega C_{gd} + \frac{j\omega g_m R_{sub} C_{db}}{1 + j\omega R_{sub} (C_{sub} + C_{db})} + \frac{j\omega C_{db} (1 + j\omega R_{sub} C_{sub})}{1 + j\omega R_{sub} (C_{sub} + C_{db})} \quad (4)$$

B. Z-parameters

$$\text{Re}[Z_{12}] \cong R_s + B C_{gd} / (\omega^2 A^2 + B^2) \quad (5)$$

$$\text{Im}[Z_{12}] \cong -\omega A C_{gd} / (\omega^2 A^2 + B^2) \quad (6)$$

$$\text{Re}[Z_{22}] \cong R_s + R_d + (C_{gs} + C_{gd}) B / (\omega^2 A^2 + B^2) \quad (7)$$

$$\text{Im}[Z_{22}] \cong \omega B R_g (C_{gs} + C_{gd})^2 - \omega A (C_{gs} + C_{gd})^2 / (\omega^2 A^2 + B^2) \quad (8)$$

Where,

$$A = C_{gd} C_{gs} + C_{db} (C_{gs} + C_{gd}) \quad (9)$$

$$B = g_{ds} (C_{gd} + C_{gs}) + g_m C_{gd} \quad (10)$$

In order to determine the other parameters, they can be shown in terms of real and imaginary part of Y' or Z' as shown below.

a) Transconductance,

$$g_m = \text{Re} al(Y'_{21}) \quad (11)$$

b) Drain-to-source transconductance,

$$g_{ds} = \text{Re} al(Y'_{22}); \text{ when } \omega \rightarrow 0 \quad (12)$$

c) Gate resistance,

$$R_g = \text{Re} al(Y'_{11}) / \text{Im}(Y'_{11})^2 \quad (13)$$

d) Gate-to-drain capacitance,

$$C_{gd} = -[\text{Im}(Y'_{12})] / \omega \quad (14)$$

e) Gate-to-source capacitance

$$C_{gs} = [\text{Im}(Y'_{11}) / \omega] - C_{gd} \quad (15)$$

f) Extraction of Substrate Parameters R_{sub} , C_{db} and g_{mb}

The extraction equations are given as follows:

$$R_{sub} = \frac{\text{Re}(Y_{22}) - g_{ds}}{(\text{Im}(Y_{22}) + \text{Im}(Y_{12}))^2 - g_{mb} (\text{Re}(Y_{22}) - g_{ds})} \quad (16)$$

$$C_{db} = \frac{\text{Re}(Y_{22}) - g_{ds}}{R_{sub} \omega (\text{Im}(Y_{22}) + \text{Im}(Y_{12}))}, \quad (17)$$

$$g_{mb} \approx 0.2 \times g_m \quad (18)$$

VI. EXTRACTION RESULTS

TABLE-2

For $V_{gs} = 0.3 \text{ V}$ $V_{ds} = 0 \text{ V}$, $R_s = 3 \Omega$ $R_d = 5.95 \Omega$		
	Bias point 1 $V_g = 0.3 \text{ V}$, $V_d = 1.0 \text{ V}$	Bias point 2 $V_g = 0.3 \text{ V}$, $V_d = 1.5 \text{ V}$
g_m	3.8 mS	4.5 mS
g_{ds}	1.06 mS	1.241 mS
R_g	1.606 Ω	1.38 Ω
C_{gs}	319.07 fF	308.5 fF
C_{gd}	117.01 fF	112.96 fF
R_{sub}	22 m Ω	14.49 m Ω
C_{db}	90.0 fF	88.12 fF
g_{mb}	0.76 mS	0.9 mS

VII. S-PARAMETERS OF FABRICATED MOSFET

S-parameters of this fabricated device at bias point $V_g = 0.3 \text{ V}$ and $V_d = 1.5 \text{ V}$ can also be produced as:

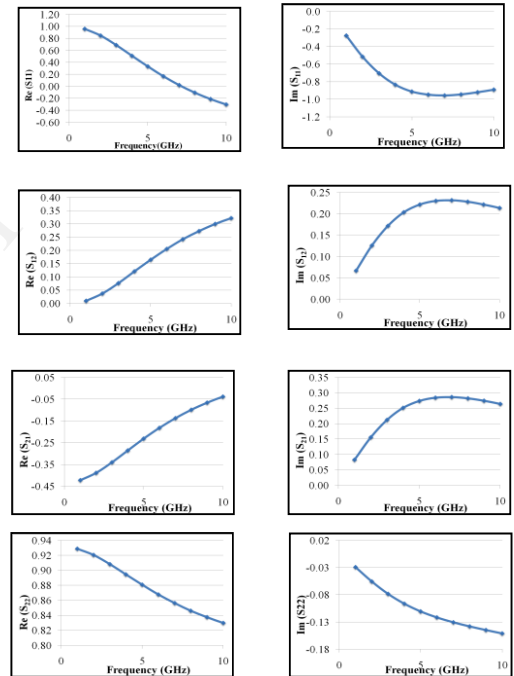


Fig.6 Generated S-parameters of Fabricated MOSFET

Short channel effects are studied and hence lightly doped drain and lightly doped source regions are considered to overcome these effects. ATLAS (Silvaco) TCAD tool is used for fabrication of MOSFET of channel length 90nm, gate oxide thickness as 2nm and threshold voltage 0.26V. DC-IV characteristics and S-parameters are generated. Now MOSFET is fabricated and shows the desired characteristics and can be used for further analysis.

VIII. MODEL TESTING

The components in the RF model has been determined, hence the RF model is known. For model testing, S-parameters of the model are generated and compared with the Fabricated NMOS Device S-parameters.

The comparison of Fabricated NMOS Device and modelled S-parameters will show that if the Fabricated NMOS Device and modelled plots are close then model is accurate within the permissible limit. The s-parameter is generated from the model using ADS (Advanced Design Systems).

IX. COMPARISON OF GENERATED AND MODELLED S-PARAMETERS

The comparison of the Modelled and Generated from Fabricated NMOS S-parameters is shown herewith. Fig.6 shows the comparison S-parameters at bias point 1 i.e. $V_g = 0.3 \text{ V}$ and $V_d = 1.0 \text{ V}$.

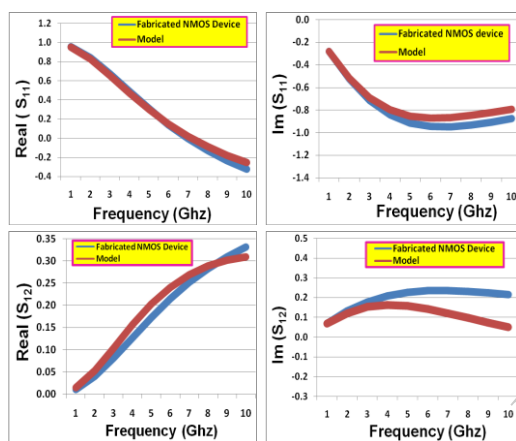


Fig. 7(a) Plot for S_{11} and S_{12} Vs Frequency at bias point 1

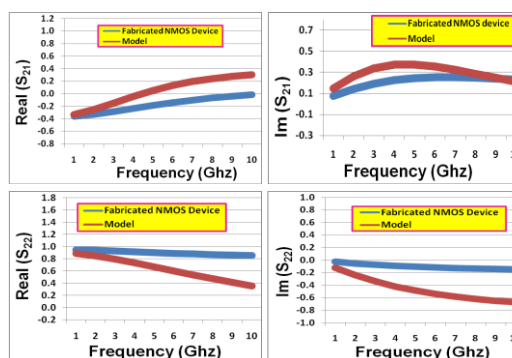


Fig. 7 (b) Plot for S_{21} and S_{22} Vs Frequency at bias point 1

X. SUMMARY

The MOSFET has been successfully fabricated using ATLAS(SILVACO) TCAD tool. The device is solved for dc-iv characteristics and S-parameters are obtained. To overcome some of the short channel effects at nano-scale lightly doped drain and source have been used.[6],[11] The coupling through the substrate is an important effect for mixed mode high-frequency IC design and should be appropriately accounted. At low frequency (<1GHz), it is good enough to model the substrate by a purely resistive network. However at high frequency (>1GHz), where most of the wireless communication systems operate, both resistive and dielectric losses are important and must be appropriately modeled by a combination of R_{sub} and C_{db} . When this is done and appropriate account is taken of the back gate transconductance effect, a much more accurate RF model is developed, which can be used for evaluation output reflection coefficient in individual transistors as well as carrying out circuit design.

REFERENCES

- [1] Fabio D' Agostino, Deniele Quereia " Project on short channel effect in MOSFET" Introduction to VLSI Design (EECS 467), December 2000.
- [2] Singh, N.S.S. ; Electr. & Electron. Eng. Dept., Univ. Teknol. PETRONAS, Tronoh, Malaysia ; Hamid, N.H. ; Asirvadani, V.S. "Accurate modeling method to evaluate reliability of nanoscale circuits" Electron Devices and Solid State Circuit (EDSSC), 2012 IEEE International Conference on Date of Conference: 3-5 Dec. 2012
- [3] C. C. Wu, et al., "A 90-nm CMOS device technology with high-speed, general-purpose, and low-leakage transistors for system on chip applications," IEDM Tech. Dig., pp. 65–68, 2002.
- [4] Rodriguez, A. ; Dept. of Electr. Eng., Univ. of Texas-Pan American, Edinburg, TX, USA ; Huq, H.F. "Validation of nano-CMOS Predictive Technology Model tool on NanoHUB.org" Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference on Date of Conference: 15-18 Aug. 2011
- [5] jun liu, xiao-jun xu, ling-ling sun " Accurate Modeling and extraction methodology for RF MOSFET valid upto 40 GHz" IEEE 2006, Microelectronics CAD centre, Hangzhou Dianzi University, China.
- [6] M.S. Alam and G.A. Armstrong, "Extrinsic parameter extraction & RF modeling of CMOS", International Journal of Solid State Electronics, Elsevier Publication, Volume 48, Issue 5, 2004, pp. 669-674.
- [7] Lan Wei et al, " Parasitic Capacitance Analytical Model and Impact on circuit level performance" IEEE Transaction on Electron Device, Vol. 58 No.5, May 2011.
- [8] Yu cao, Takashi Sato Michael Ovshanky, Dennis Sylvester and Chenming Hu. "New paradigm of predictive MOSFET and inter connect modeling for early circuit simulation" Custom integrated circuit cnf pp 201-204. IEEE 2000 ICC.
- [9] www.ptm.asu.edu
- [10] Online documentation: <http://www.silvaco.com/>
- [11] Markov, S.; Xingsheng Wang; Moezi, N.; Asenov, A. "Drain Current Collapse in Nanoscaled Bulk MOSFETs Due to Random Dopant Compensation in the Source/Drain Extensions Electron Devices, IEEE Transactions on Volume: 58 , 2011