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Characterization Of High Speed CMOS Resistive Dividing Comparator In Different CMOS Technologies

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Abstract

In this paper different types of analysis of Resistive Dividing comparator along with the buffer stage is presented. Various analysis of characteristics of comparator such as propagation delay, speed, power dissipation, input common mode range, offset has been carried out in three different technologies 0.35um, 0.25um and 0.18um. The supply voltage is kept at 3v, 2.5v, 1.8v for 0.35um, 0.25um and 0.18um technologies respectively.

1. Introduction

A Comparator is a circuit that compares an analog signal with another analog signal or reference & outputs a signal in digital form, either logic'0' or logic '1'. The comparator find it's application in converting analog signals into digital signals. Usually, the comparator can be considered as 1- bit ADC. While designing the comparators factors which must be considered are power consumption, propagation delay, offset, input common mode range. With the help of dynamic latch comparators silicon area can be reduced by removing the pre-amplification stage[1] [2] of the conventional comparator. Also, by replacement of traditional amplifier chain comparators less power is dissipated by dynamic latch comparators. they are also useful to achieve low power dissipation by replacing traditional amplifier- chain comparators. This paper focuses on resistive dividing comparator.

2. Resistive Dividing Comparator and Buffer Stage

2.1. Resistive Dividing Comparator

Figure.1. shows the schematic of resistive dividing comparator. The circuit works in regenerative mode when the Clk signal goes high. As the Clk is high the nMOS transistor M9 are on and the pMOS transistors M6 and M13 will be off. In regenerative mode the circuit compares the input voltages with the help of transistors which will be operated in triode region.

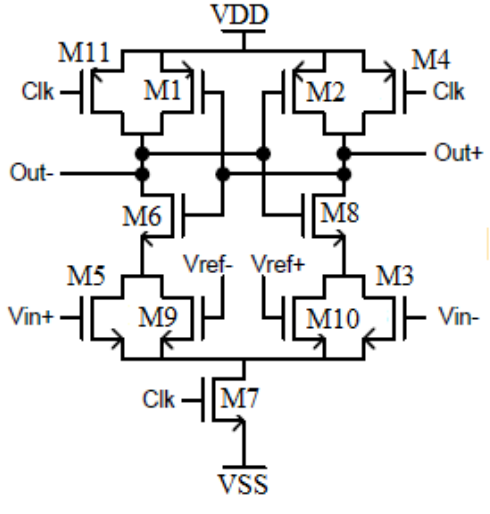

Figure 1. Resistive Dividing comparator[1]

The circuit is in reset mode when the Clk signal goes low. As The Clk is low nMOS transistor M9 is off and hence circuit will get disconnected from the V_{SS}. At the same time, pMOS transistors M13 and M6 are on and hence the outputs will be precharged upto VDD.

2.2. The Buffer Stage

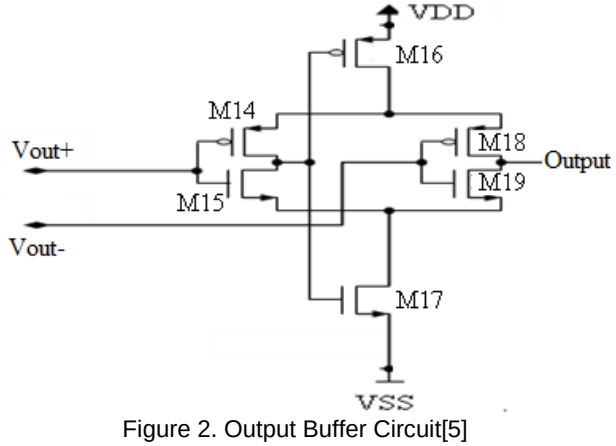

Figure 2. Output Buffer Circuit[5]

The circuit diagram for output buffer circuit used in the comparator is shown in figure 2[5]. The output buffer stage is also known as post amplifier. This circuit is self biasing differential amplifier which has differential inputs as Vout+ & Vout- and does not have any slew rate limitations. It is also useful in giving the output in proper shape.

3. Designing of Comparator

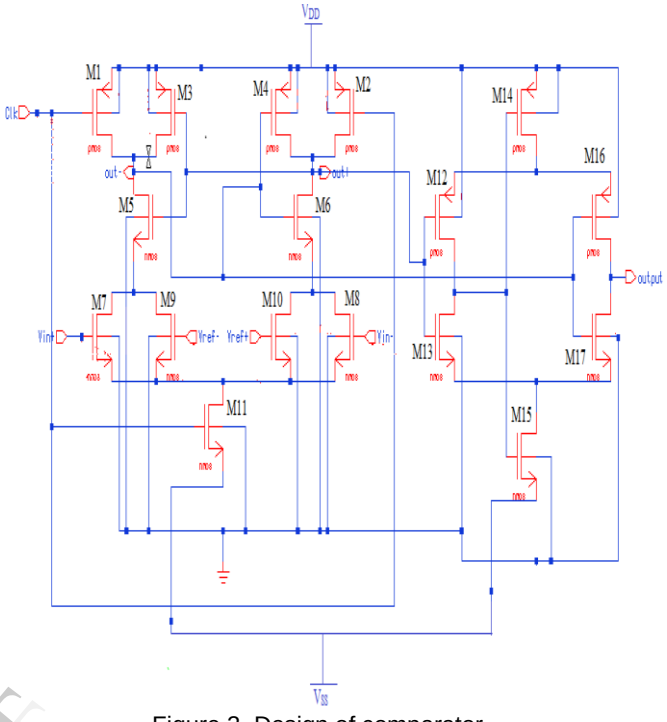

Figure 3. Design of comparator

Fig.4 shows the circuit diagram of comparator consisting of resistive dividing network and output buffer stage. The two ended output of the resistive dividing comparator are Vout+ & Vout-. Both the outputs of the comparator are inputs to the buffer. Thus the two ended output of resistive dividing comparator is being converted into single ended output for different types of analysis.

Table 1.
CMOS Transistor widths for different technologies

Transistor	Technology		
	0.35um	0.25um	0.18um
M1,M2	11	10	8
M3,M4	9	8	6
M5,M6,M11	4.5	4	3
M7,M8,M9,M10	5.5	5	4
M12,M14,M16	9	8	6
M13,M15,M17	4.5	4	3

Table I given above shows different widths of the transistor to be used according to the chosen technology. The length for the transistor is 0.35um, 0.25um and 0.18um respectively for 0.35um,0.25um and 0.18um technology.

4. Simulation Results

The simulated results are obtained for three different technologies 0.35um 0.25um and 0.18um. In table II, different voltage values are given for supply voltage VDD and VSS, reference voltage Vref+ and Vref-, input voltage Vin+ and Vin-.

Table2.
CMOS Transistor widths for different technologies

Voltage Terminals	Technology		
	0.35um	0.25um	0.18um
Vdd	3	2.5	1.8
Vss	-3	-2.5	-1.8
Clk	3	2.5	1.8
Vin+	3	2.5	1.8
Vin-	-3	-2.5	-1.8
Vref+	1.5	1.25	0.9
Vref-	-1.5	-1.25	-0.9

4.1. Simulated Waveforms in 0.35um Technology

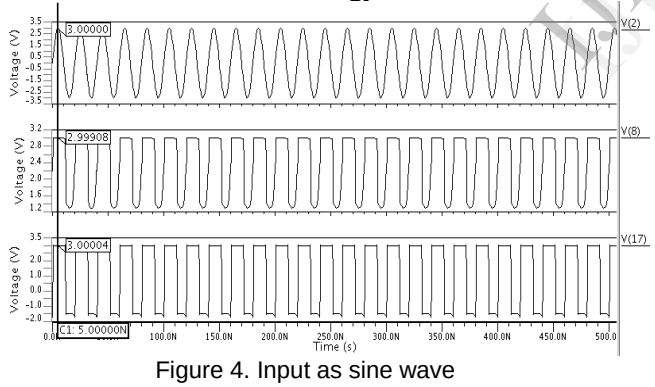

Figure 4. Input as sine wave

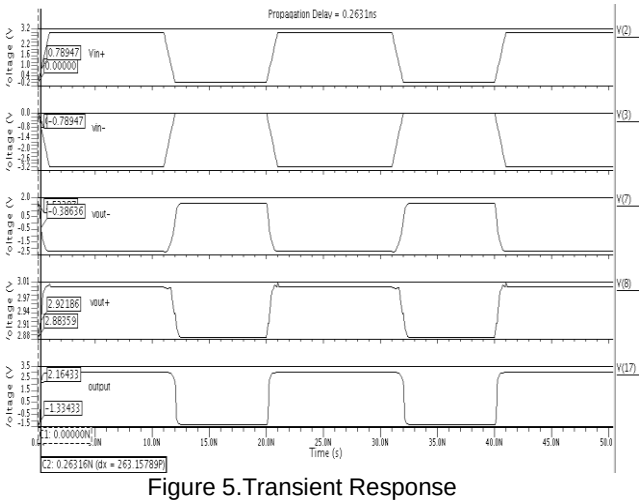

Figure 5.Transient Response

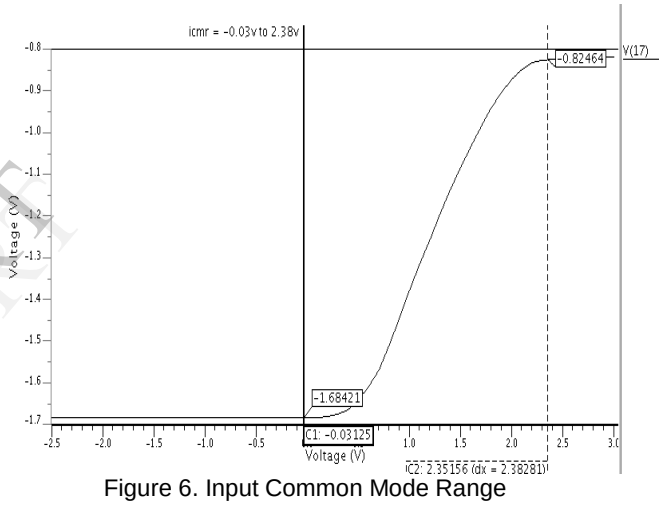

Figure 6. Input Common Mode Range

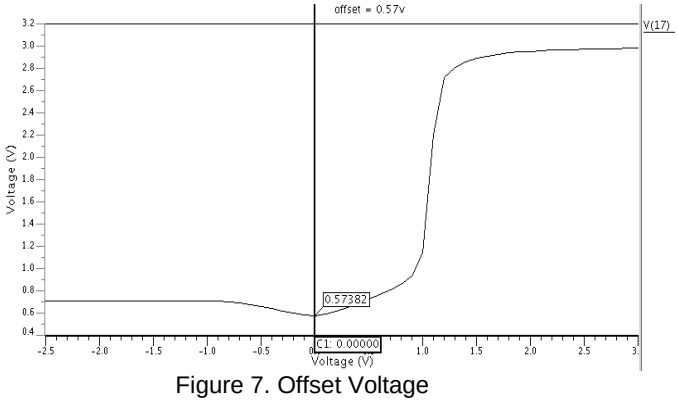

Figure 7. Offset Voltage

4.2. Simulated Waveforms in 0.25um Technology

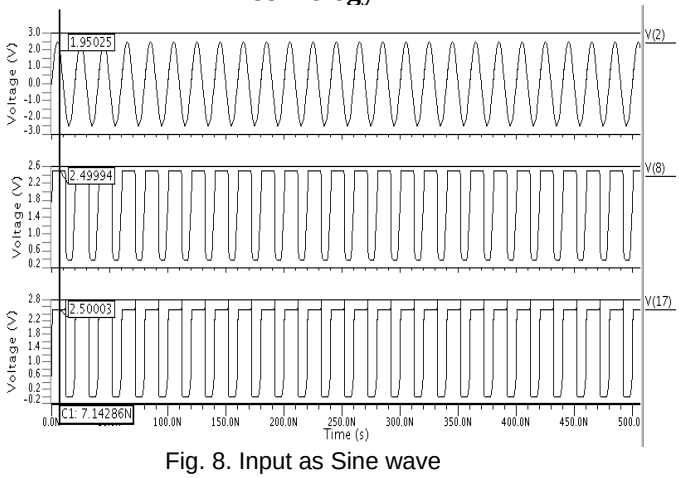

Fig. 8. Input as Sine wave

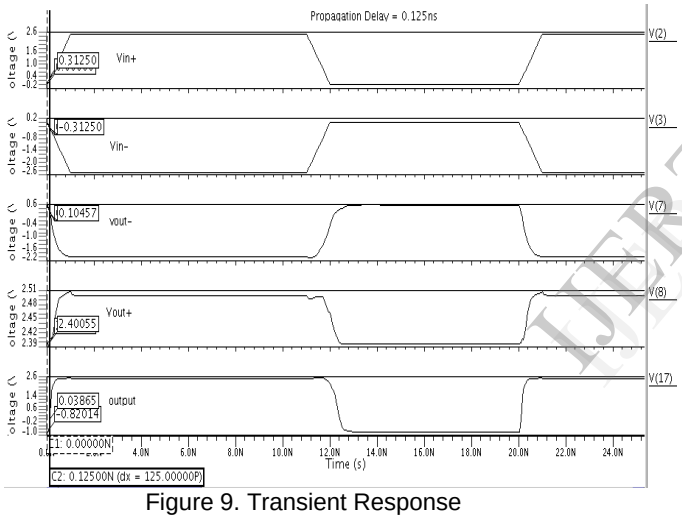

Figure 9. Transient Response

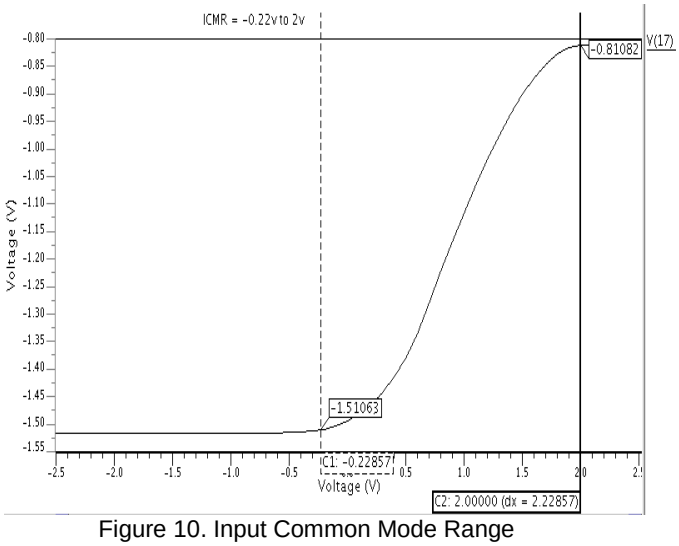

Figure 10. Input Common Mode Range

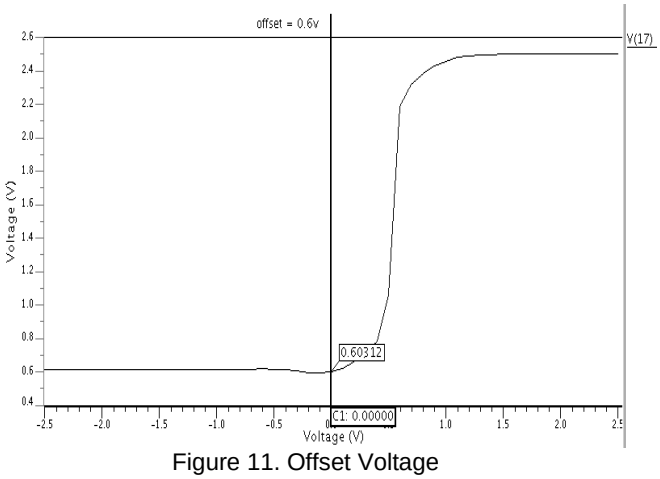

Figure 11. Offset Voltage

4.3. Simulated Waveforms in 0.18um Technology

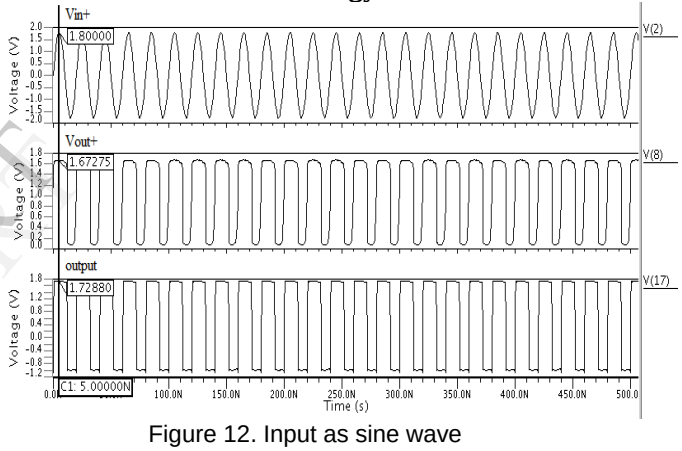

Figure 12. Input as sine wave

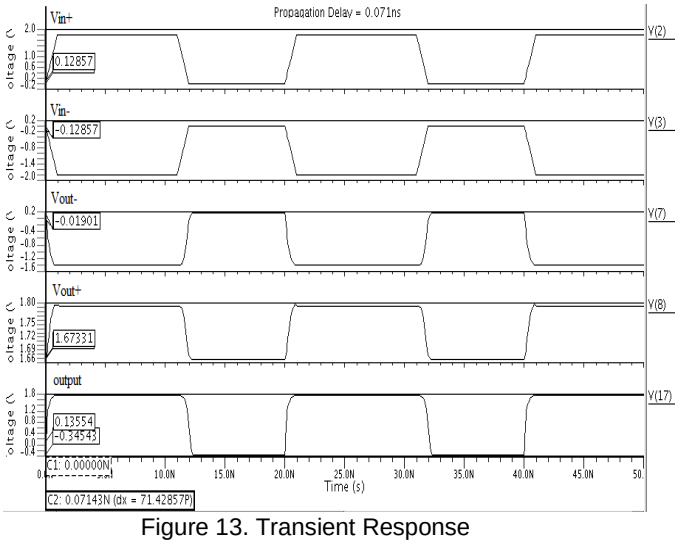

Figure 13. Transient Response

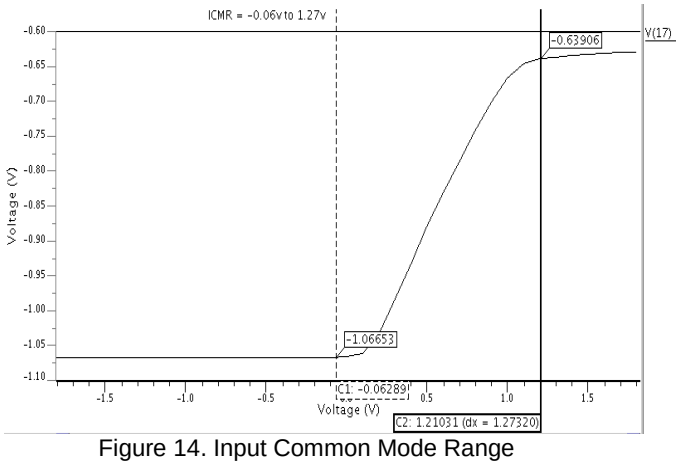

Figure 14. Input Common Mode Range

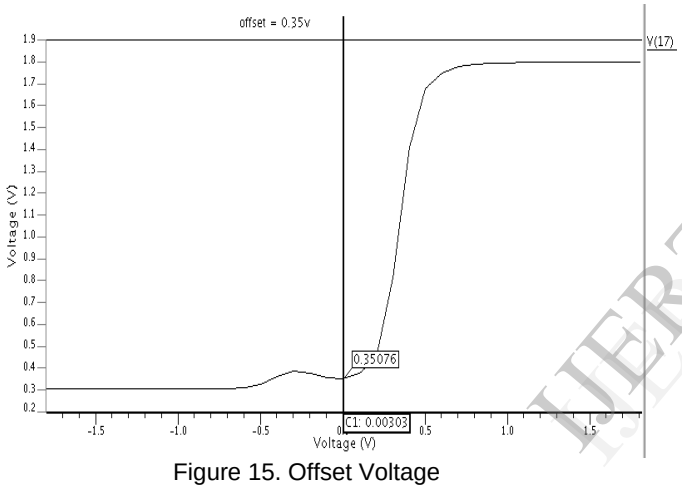

Figure 15. Offset Voltage

5. Conclusion

In this paper, simulated results are presented for the comparator for three different technologies, 0.35um, 0.25um and 0.18um. The summary of the comparison for the comparator in different technologies is given in the Table 3.

Table 3.
Different measured parameter values for different technologies

Parameters	Technology		
	0.35um	0.25um	0.18um
Propagation Delay(ns)	0.26	0.125	0.078
Speed(GHz)	3.84	8	12.28
ICMR(V)	-0.03 to 2.38	-0.22 to 2	0.06 to 1.27
Offset(V)	0.57	0.6	0.35
Power Dissipation(mV)	15.23	19.8	7.25

6. References

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