A Generalized Cascaded 31 Level Inverter using Series Connection of Submultilevel Inverters for Induction Motor Drive Applications

S Y Mudassir Hussain
Student, M. Tech 4th Semester,
Department of Instrumentation Technology,
Dayananda Sagar College of Engineering,
Bangalore, India

Rajashekhar J S
Associate Professor, H.O.D
Department of Instrumentation Technology,
Dayananda Sagar College of Engineering,
Bangalore, India

***Abstract*: Multilevel inverters are extensively used because of their increased power rating with reduced harmonics and electromagnetic interference. In this paper, initially a thirteen level inverter is proposed, that is a new method for sub multilevel inverter is proposed as a generalized multilevel inverter. The proposed multilevel inverter uses minimum number of switches. and then by just adding two more switches to the proposed multilevel inverter 31 level of multilevel inverter is then proposed. As the number of levels increases the harmonics is also reduced, hence reducing the harmonics, comparing the simulation results in terms of output voltage, current, and harmonics of both 13 and 31 level multilevel inverter. The proposed system will be tested using matlab/simulink.**

Keywords: Generalized topology, multilevel inverter, optimal structure, submultilevel inverter.

I. INTRODUCTION

Multilevel inverters include an array of power semiconductors and dc voltage sources, the output of which generate voltage with stepped waveform in comparison with a two-level voltage-source inverter (VSI). The multilevel voltage source inverter enables to synthesize output voltages with reduced harmonic distortion and lower electromagnetic interference. By increasing the number of levels in multilevel inverter output voltage have more steps in generating a staircase waveform, which has a less harmonic distortion. Although a larger number of levels increases the number of devices that must be controlled and control complexity. As a result, the most attractive applications of this technology are in medium to high voltage ranges. A multilevel inverter achieves high power ratings, and also enables the use of renewable energy sources such as PV cells, wind and fuel cells which can be easily interfaced to the multilevel inverter system for a purpose of high power application. The advantages of multilevel inverters are their smaller output voltage step, which results in voltage capability being high, lower harmonic components, low switching losses, and better electromagnetic compatibility and high power quality. It can also operate at both high switching frequency fundamental switching frequency PWM. The on field applications include use in laminators, pumps, compressors fans, blowers and mills. Simultaneously, several multilevel inverter topologies have been developed.

II.BLOCK DIAGRAM

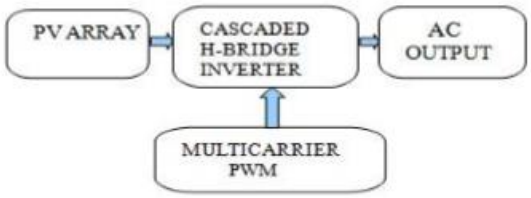

Fig.1. Block diagram

Fig. shows the block diagram of the proposed multilevel inverter. The PV array which is connected to the Cascaded H-Bridge Multilevel inverter converts sunlight directly into DC power. Cascaded H-Bridge multilevel inverter converts DC power into AC power for AC load and it is controlled by multicarrier PWM technique. The Proposed Cascaded Multilevel Inverter is simply a number of conventional multi-level bridges, whose AC terminals are simply connected in series to synthesize a multi level square wave output voltage waveform. The circuit needs independent dc source which is supplied from photovoltaic cell.

1. **PV ARRAY**:

- Equivalent model

A Photovoltaic cell is a device used to convert solar radiation directly into electricity. It consists of two or more thin layers of semiconducting material, most commonly silicon. When the silicon is exposed to light, electrical charges are generated. A PV cell is usually represented by an electrical equivalent one-diode model shown in fig

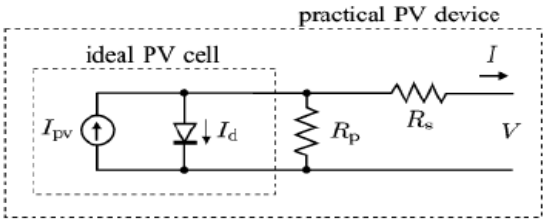

Fig.2. PV Array

The model contains a current source, one diode, internal shunt resistance and a series resistance which represents the resistance inside each cell. The net current is the difference between the photo current and the normal diode current which is given by the equation.

$$ID = IO\ [e^{\frac{q(V+IRs}{KT}} - 1] \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$I = I_L - I_O\ [e^{\frac{q(V+IRs}{KT}} - 1] - \frac{V+IRs}{Rsh} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Where I is the cell Current(A). Q is the charge of electron (coul). K is the Boltzmann's constant (j/K). T is the cell temperature (K). IL is the photo current (A). Io is the diode saturation current.(A) Rs , Rsh are cell series and shunt resistances (ohms). V is the cell output voltage (V).

2. CASCADED H-BRIDGE INVERTER

The CHB multilevel inverters use series-connected H-bridge cells with an isolated dc voltage sources connected to each cell. The CHB multilevel inverters can be divided into two groups from the viewpoint of values of the dc voltage sources: the symmetric and the asymmetric topology. In the symmetric topology, the values of all of the dc voltage sources are equal. This characteristic gives the topology good modularity. However, the number of the switching devices rapidly increases by increasing the number of output voltage level. In order to increase the number of output voltage level, the values of the dc voltage sources are selected to be different, these topologies are called asymmetric. The CHB multilevel inverters have been industrially employed in several applications fields such as pump, fans, compressors, etc. In addition, they have recently been proposed for other applications like photovoltaic power-conversion system and wind power conversion. The topologies discussed previously are the conventional topologies. Many other multilevel inverter topologies have been introduced in recent years. One of the topologies is the modular multilevel inverter. This topology is simpler than the cascaded four-switch-bridge-based inverter and has several advantages, such as modular extension to any number of levels and redundancy. However, the topology does not consider reduction in the number of components used. The multilevel inverter presented is based on symmetric topology and uses series/parallel connection of the dc voltage sources. This topology uses lower number of switches in comparison with the symmetric CHB multilevel inverter. The topologies presented in and consider reduction in the components. These topologies are basically based on asymmetric topologies; hence, the used dc voltage sources have different values. However, the number of switching devices still remains high in these topologies. An in-level active npc inverter has been presented in which is the modification of the standard active NPC converter. Nami et al. present a hybrid multilevel inverter using the CHB and the diode-clamped topology. This paper proposes a new multilevel inverter topology using series-connected sub multilevel inverters. The proposed multilevel inverter uses reduced number of switches. Initially, the proposed submultilevel inverter is described and then the series connection of them to form a multilevel inverter is discussed. The optimal structures of the proposed multilevel inverter regarding several factors (e.g., number of switches, number of dc voltage sources, standing voltage on the switches, etc.) are also obtained. The power loss of the proposed topology is calculated. Afterward, the proposed multilevel inverter is compared with other multilevel inverter topologies considering the number of switches. A design example is then given which is used for simulation studies.

3. MULTICARRIER PWM TECHNIQUE

The Multicarrier PWM technique was introduced and uses several triangular carrier signals and only one modulating sinusoidal signal as reference wave to generate the PWM switching signals. If an 'n' level inverter is employed, 'n-1' carriers will be needed. At every instant each carrier is compared with the modulating signal. Each comparison gives one if the modulating signal is greater than the triangular carrier, zero otherwise. The results are added to give the voltage level, which is required at the output terminal of the inverter. Frequency modulation ratio is defined as the ratio of carrier frequency and modulating frequency.

Mf = fc/ fm ..... (4)

Amplitude modulation ratio is defined as the ratio of amplitude of modulating signal and amplitude of carrier signal.

Ma = Am/□ n−1□ Ac …….(6)

Using this technique THD value can be reduced.

III. PROPOSED GENERALIZED MULTILEVEL INVERTER

A. Proposed Submultilevel Inverter

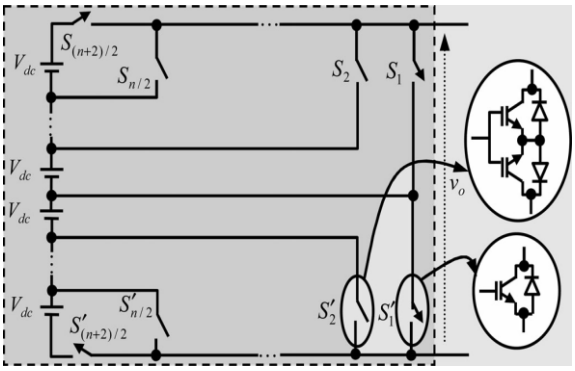

Fig.3. Proposed generalized submultilevel inverter.

Fig 3 shows the proposed sub multilevel inverter. As in Fig 3, the topology consists of n dc voltage sources. In general, dc voltage sources can have the different values. However, to have equal voltage steps, dc voltage sources are considered to be the same and equal to Vdc. Each SMI consists of n + 2 number switches. Some of the switches in the circuit are unidirectional and the others are bidirectional. The unidirectional switche consist of an insulated gate bipolar transistor with diode connected antiparallel to it. The switches S1, S_ 1 , S(n+2)/2 , and S_ (n+2)/2 are unidirectional and all other switches are bidirectional; hence, they have to be both positive and negative voltages. For instance, when S(n+2)/2 is turned ON, voltage Vdc is on the switch Sn/2 , and if the switch S(n−2)/2 is turned ON, the voltage equal to −Vdc is on the switch Sn/2 . The same conditions are applicable for the other switches. Hence, the switches have to be both positive and the negative voltages. In addition, the switches should conduct the backward current that is as a result of inductive characteristics of the load. Therefore, It can be concluded that the switches must be bidirectional. There are some circuit configurations for bidirectional switches. The common emitter topology is used in this topology because it needs one gate driver for a switch. Looking at the types of the switches, 2n IGBTs are required in the following SMI. The number of the antiparallel diodes is equal to the number of IGBTs.

The proposed SMI can only generate zero and positive voltage levels. The zero output voltage is obtained when both the switches are turned ON at same instant. proper switching between the switches can generate other voltage levels. Table I shows the different states of the switches for each output voltage value. In this table, 1 means that the switch is turned ON and 0 indicates that the switch is in OFF state.

Considering Fig. 3, for each value of the output voltage of SMI, two switches must be turned ON, one from the lower switches and the other one from the upper switches of the circuit. For example, to get output voltage of *V*dc, the switches *S*_1 and *S*2 are turned ON. the switches *Sn*/2 and *S*_ (*n*+2)/2 should be turned ON in order to obtain the output voltage of (*n* − 1)*V*dc.

State	Switches states									v_o
	S_1	S_1'	S_2	S_2'	…	$S_{n/2}'$	$S_{n/2}$	$S_{(n+2)/2}$	$S_{(n+2)/2}'$	
1	1	1	0	0	…	0	0	0	0	0
2	0	1	1	0	…	0	0	0	0	V_{dc}
3	0	0	1	1	…	0	0	0	0	$2V_{dc}$
⋮	⋮	⋮	⋮	⋮	…	⋮	⋮	⋮	⋮	⋮
$n-1$	0	0	0	0	…	1	1	0	0	$(n-2)V_{dc}$
n	0	0	0	0	…	0	1	0	1	$(n-1)V_{dc}$
$n-1$	0	0	0	0	…	0	0	1	1	nV_{dc}

TABLE I Output voltages for states of switches

B. Proposed Generalized Multilevel Inverter

To achieve the desired voltage and number of voltage levels The proposed submultilevel inverters is connected in series. Fig 4 shows *m* submultilevel inverters connected in series. Each SMI has *n* number of dc voltage source. The dc voltage source in each SMI are equal. The output voltage of the SMI are always positive or zero. It is necessary to change the voltage polarity in every half cycle to operate as an inverter. For this purpose an H-bridge inverter is added to the output of the series connected SMI. It is important to note that the switches of the H-bridge must have higher voltage. This is to be considered in the design of the inverter. However, switches are turned ON and OFF once during a fundamental frequency cycle. hence, these switches would be high-voltage low-frequency switches.

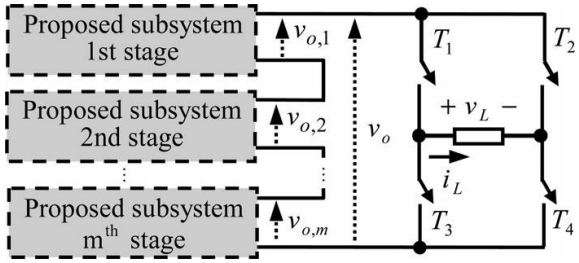

Fig.4 Proposed general multilevel inverter using series connection of *m* proposed SMI, each one has *n* dc voltage sources.

IV. SIMULATION RESULTS

- ***13 level inverter***

For the simulation the load is an R load with the value of 45 Ω. The output voltage frequency is assumed 50 Hz. There are many other control methods used for multilevel inverter. It can be observed that the staircase control method is used in this multilevel inverter. The term staircase control method is used to state that in this method, transition from one level to the other level happens once. This control method tends to generate a staircase voltage which minimizes the error with respect to the reference voltage.

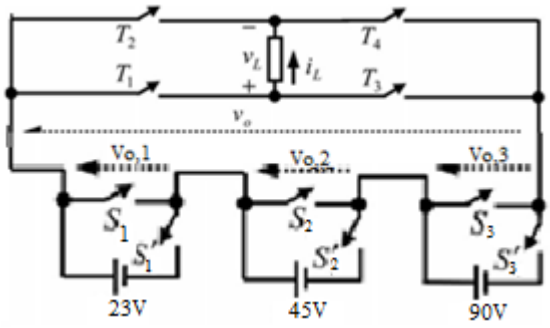

Fig.5. Thirteen-level inverter based on the proposed Asymmetric topology with *n* = 1 and *m* = 3.

Fig.5 shows the 13-level inverter based on the proposed asymmetric multilevel inverter with *n*=1. Three dc voltage

sources each of them 90V, 45V, 23V have been used so that the maximum output voltage will be 158 V. The number of IGBTs for a 13-level inverter in the proposed topology is 10.

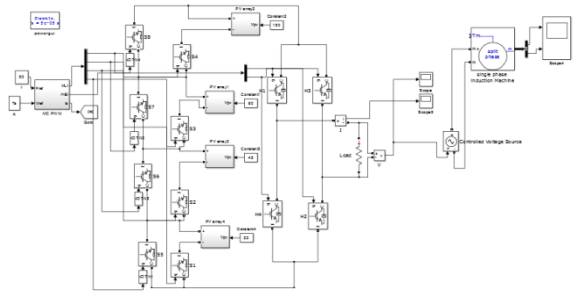

Fig 6. Schematic of thirteen level inverter.

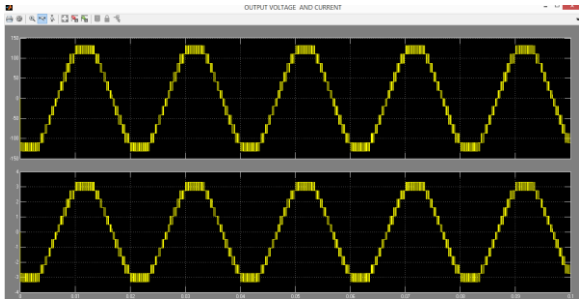

Fig 7 output voltage and current of thirteen level

Fig 7 shows the output voltage of the cascaded submultilevel inverters. The polarity of the voltage is changed using the H-bridge connected to the output of the submultilevel inverters. In the test condition (R = 40, Vo,max = 158 V), referring to figure 7 the output voltage is 130.2 volts and the output current is 3.3A hence the putput power is 429.66W.

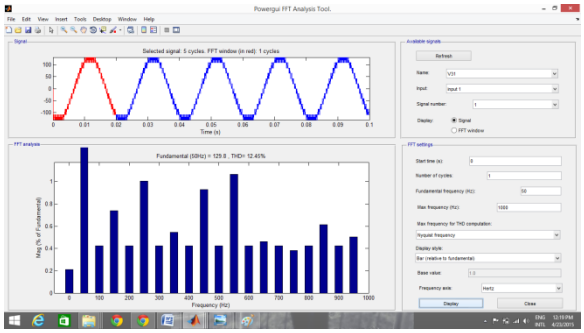

Fig 7. Total harmonic distortion

Fig 7 shows the total harmonic distortion The proposed topology has the advantage of its reduced number switches and harmonics are reduced with THD value of 12.45% at 130.2V is achieved. For proposed harmonic spectrum of the simulation system is as shown in the fig.7, which shows the results are well within the specified limits of IEEE standards. The results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB.

- ***31 level inverter***

For the simulation the load is an R load with the value of 45 Ω. The output voltage frequency is assumed 50 Hz. There are many other control methods used for multilevel inverter. It can be observed that the staircase control method is used in this multilevel inverter. The term staircase control method is used to state that in this method, transition from one level to the other level happens once. This control method tends to generate a staircase voltage which minimizes the error with respect to the reference voltage.

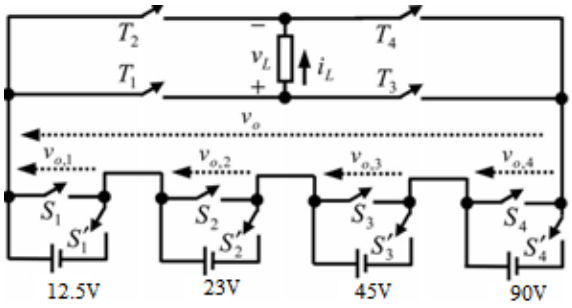

Fig.8. Thirteen-level inverter based on the proposed Asymmetric topology with n = 1 and m = 4.

Fig.8 shows the 13-level inverter based on the proposed asymmetric multilevel inverter with n=1. Four dc voltage sources each of them 90,45,23,12.5 V have been used so that the maximum output voltage will be 170.5 V. The number of IGBTs for a 13-level inverter in the proposed topology is 12.

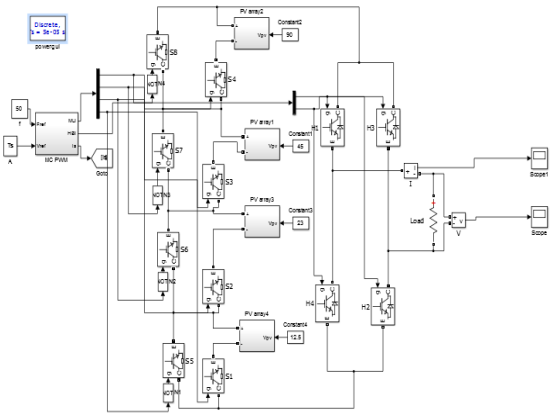

Fig 9. Schematic of 31 level inverter.

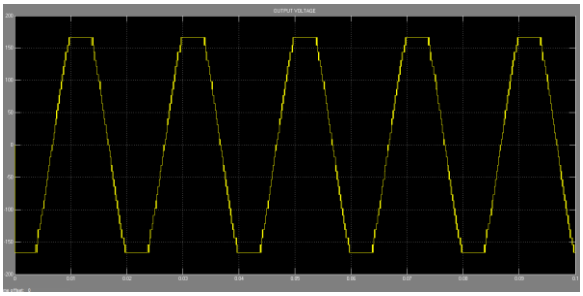

Fig 10 output voltage of 31 level

Fig 10 shows the output voltage of the cascaded submultilevel inverters. The polarity of the voltage is changed using the H-bridge connected to the output of the submultilevel inverters. In the test condition (R = 45, Vo,max = 170.5 V),as in fig 10 and fig 11 the output voltage and output current obtained are166.5V 3.7A respectively. In this condition, active output power of the inverter is about 616W.

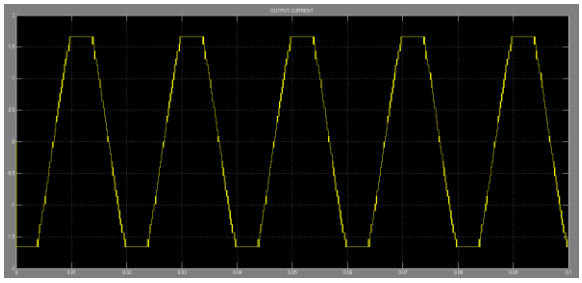

Fig 11 output current of 31 level

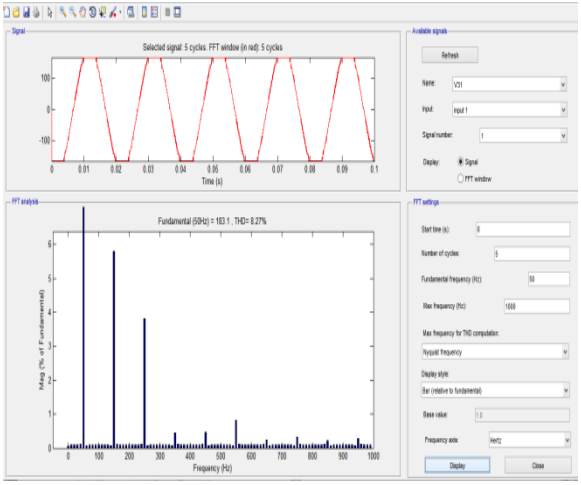

Fig 12. Total harmonic distortion of 31 level inverter.

Fig 12 shows the total harmonic distortion The proposed topology has the advantage of its reduced number switches and harmonics are reduced with THD value of 8.27% at 166.5V is achieved. For proposed harmonic spectrum of the simulation system is as shown in the fig.12, which shows the results are well within the specified limits of IEEE standards. The results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB.

PARAMETERS	13 LEVEL INVERTER WITH DC SOURCE	31 LEVEL INVERTER WITH PV SOURCE
NO. OF SWITCHES	10	12
OUTPUT VOLTAGE (V)	130.2	166.5
OUTPUT CURRENT (A)	3.3	3.7
OUTPUT POWER (W)	429.66	616
HARMONICS	12.45%	8.27%

TABLE II Simulation results

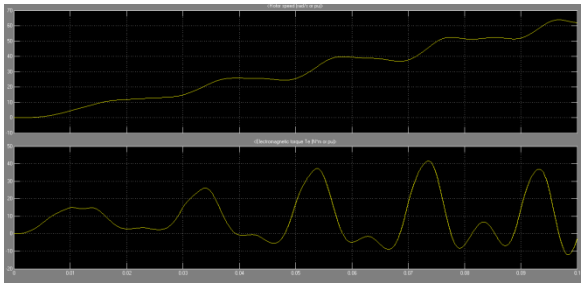

Fig.13. Torque and speed behavior of induction motor.

Many current and future designs will incorporate the use of induction motors as the primary source for traction in electric vehicles. Designs for heavy duty trucks and many military combat vehicles that have large electric drives will require advanced power electronic inverters to meet the high power demands (>250 kw). Development of electric drive trains for these large vehicles will result in increased fuel efficiency, lower emissions, and likely better vehicle performance (acceleration and braking). Multilevel inverters are uniquely suited for these applications because of the high VA ratings possible with these inverters.

V. CONCLUSION

A multilevel inverter with individual dc sources has been proposed for use in large electric drives for 13 level inverter and then a 31 level inverter with less number of switches and with PV source has been proposed. Simulation results have shown that with the control strategy operates the switches at the fundamental frequency, the converters have low output voltage, Total Harmonic Distortion(THD), and power factor.

Simulation has been done in the MATLAB /SIMULINK. From the simulation it is noted that new MLI topology works well and shows hope to reduce the cost and complexity. Whenever the output voltage levels gets increased, the number of switches will be used is very less compared to other multilevel topologies. By the increase in output voltage levels the total harmonic distortion starts get reduced, so that it can be used in many power applications.

VI. REFERENCES

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