

# Cascaded H-Bridge 11-level Multilevel Inverter

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**Abstract:-** This paper basically focusses on the design and implementation of a topology for a three phase eleven level cascaded H-bridge multilevel inverter by employing different kinds of switching methods. The basic purpose of this work is to increase the number of voltage level at the output with reduction of complexity to power circuit. The main advantages of this proposed topology is to reduce the Total Harmonic Distortion and minimise electromagnetic interface EMI generation and high voltage with very nearly to sine waveform. In this work, several kinds of carrier pulse width modulation techniques are proposed as which reduced the total harmonic distortion and improve the out voltage from the proposed topology and POD modulation techniques reduce the Total Harmonic Distortion. A number of H-bridge arranged in cascade form to increase the voltage level with the different switching schemes It is observed that this new topology can be recommended to three phase eleven level cascaded H-bridge inverter for getting optimum performance over the conventional methods. This performance is optimized in the eleven level of inverter. Improving the fundamental waveforms and reducing the total harmonic distortion is achieved by Utilizing 60 IGBTs and switching is arranged by a topology in cascaded form. The simulation model is produced by MATLAB 2018 software version.

**Key Words:** Cascaded H-bridge multilevel inverter, total harmonic distortion THD, Electromagnetic Interface, different phase pulse width modulation,

## 1. INTRODUCTION:

The present status of global electricity demand is rapidly growing which caused the depletion of conventional energy resources like coal, oil, natural gas, etc. While the worldwide concern is how to fulfill the future electricity demand by using sustainable and reliable energy sources like non-conventional or renewable energy resources (RES). So the researchers are mainly focussing on that power generation source which is based on conventional energy resources. Solar photovoltaic and windmill energy are the two main types of conventional energy resources that take part in power generation [1-3]. Solar energy has some advantages over wind energy in terms of installation cost, maintenance, and availability. The output nature of Renewable Energy Sources is DC voltage and mainly they are intermittent which results in inherently unstable Output, which results in the reduction of stability and quality of power which can be improved by applying multi-level inverters (MLI) at the output of Renewable Energy Resources [4,5]. The idea of the multi-level inverter was given by Baker and Bannister in beginning of 1975, According to which it generates stepped waveform by using either single or multiple voltage sources as it has ability to give an effective interface with Renewable Energy Resources [6].

The attractive features of multi-level inverters are output waveform with less THD, smaller common-mode voltage, low dv/dt, less electromagnetic interference, reduction of requirement of passive filter, and low switching loss. Multilevel Inverter operates at both fundamental and high-frequency pulse width modulation but the common drawback is, it requires a more number of switches followed by their driving circuits which makes it complex and costly [7-9]. The controlling and modulation of multi-level inverters becomes difficult with development in multi-level inverters topologies. The stepped waveform produced by multi-level inverters having some lower-order harmonics, which results in fluctuations in voltage, increases in losses, and effect the quality of power. With proper controlling and modulation techniques, the above mentioned issue can be reduced [10]. There are two basic control schemes high-frequency switching scheme and low-frequency switching scheme in which low frequency have ability to give better control [11]. Selective harmonic elimination schemes are Low Switching frequency schemes. Sinusoidal pulse width modulation, and space vector pulse width modulation are the high-frequency switching techniques [12].

While Reduced Switched Multi-level Inverters generates a great number of step levels with less numbers of switches is much needed in the present circumstances.

## 2. CONCEPT OF MULTI-LEVEL INVERTERS AND STAIRCASE WAVEFORM

Inverters are distributed into the four main categories based on output waveform which are the square wave, quasi wave, two levels pulse width modulation inverter, and multi-level inverters [13].

Multi-level inverter gets more existence in recent decades both in the industrial and research area. The concept of multi-level inverters is based on producing a stepped voltage waveform at the output which is close to sinusoidal waveform by applying power semiconductor switches with d.c voltage sources [14]. In multi-level inverters for generating a stepped waveform closer to a sinusoidal waveform, a proper driving circuit and isolated or non-isolated DC sources are employed for controlling power semiconductor devices. To approach the sinusoidal waveform without an expensive passive filter and bulky transformer number of step levels at the output should be increased [15-16]

The benefit due to which multi-level inverters get attention is according to the literature [17-20].

- The staircase waveform produces lower harmonic and smaller dv/dt which results in minimization of bulky filters.
- The lesser common-mode voltage thus motor bearing stress get reduces.
- Electromagnetic interference is lower.
- Multi-level inverters draw low distortion current.
- If the asymmetrical sources are used then more levels can be generated with the equal number of switches, practically it can be possible by using different RES like solar photovoltaic, wind, fuel, cell, etc.

### 3. CONVENTIONAL MULTI-LEVEL INVERTERS

Traditionally, the Multi-Level Inverters can be classified, based on their circuit design into three types that are Neutral Point Clamped MLI, Capacitor Clamped MLI, and Cascaded H-Bridge MLI. The Cascaded H-Bridge MLI is mostly used because of its flexibility and redundancy. The modified structure of the Cascaded H-bridge inverter makes it easily designed for any desired number of levels [21,22].

### 4. PROPOSED TOPOLOGY:

This topology requires sixty semiconductor switches and fifteen isolated dc voltage sources  $V_{dc}$  shown in fig 1. Operation Of Three-Phase Eleven-Level Inverter arranged in Cascaded Manner Operation of the three-phase eleven-level inverter with CHB topology is easily explained with the help of figure.

Theswitches  $S_1, S_2, S_6, S_8, S_{10}, S_{12}, S_{14}, S_{16}, S_{18}, S_{20}, S_{21}, S_{22}, S_{26}, S_{28}, S_{30}, S_{32}, S_{34}, S_{36}, S_{38}, S_{40}, S_{41}, S_{42}, S_{46}, S_{48}, S_{50}, S_{52}, S_{54}, S_{56}, S_{58}, S_{60}$  are made turned on the output voltage will be “ $V_{dc}$ ” which is level 1. The output voltage will be “ $+2V_{dc}$ ” (which is level 2)

When

Switches  $S_1, S_2, S_5, S_6, S_{10}, S_{12}, S_{14}, S_{16}, S_{18}, S_{20}, S_{21}, S_{22}, S_{25}, S_{26}, S_{30}, S_{32}, S_{34}, S_{36}, S_{38}, S_{40}, S_{41}, S_{42}, S_{45}, S_{46}, S_{50}, S_{52}, S_{54}, S_{56}, S_{58}, S_{60}$  are turned “on”. Similarly output voltage will become “ $5V_{dc}$ ” (which is level 5). When switches  $S_1, S_2, S_5, S_6, S_9, S_{10}, S_{13}, S_{14}, S_{17}, S_{18}, S_{21}, S_{22}, S_{25}, S_{26}, S_{29}, S_{30}, S_{33}, S_{34}, S_{37}, S_{38}, S_{41}, S_{42}, S_{45}, S_{46}, S_{49}, S_{50}, S_{53}, S_{54}, S_{57}$  and  $S_{58}$ .

When

Switches  $S_2, S_4, S_6, S_8, S_{10}, S_{12}, S_{14}, S_{16}, S_{18}, S_{20}, S_{22}, S_{24}, S_{26}, S_{28}, S_{30}, S_{32}, S_{34}, S_{36}, S_{38}, S_{40}, S_{42}, S_{44}, S_{46}, S_{48}, S_{50}, S_{52}, S_{54}, S_{56}, S_{58}$  and  $S_{60}$  “on” the output voltage is zero (which is level 0).  $S_3, S_4, S_7, S_8, S_{11}, S_{12}, S_{15}, S_{16}, S_{19}, S_{20}, S_{23}, S_{24}, S_{27}, S_{28}, S_{31}, S_{32}, S_{35}, S_{36}, S_{39}, S_{40}, S_{43}, S_{44}, S_{47}, S_{48}, S_{51}, S_{52}, S_{55}, S_{56}, S_{59}$  and  $S_{60}$  turn negative half cycle can be produced across load. The voltage blocking capacity for every switch is  $V_{dc}$  [23]. The operation of this topology can also be easily understood by mode of operation of single-phase eleven-level inverter shown in figure 2. Each voltage source

“ $V_{dc}$ ” is required 100V. There are eleven sufficient switching modes in generating the multistep levels for a eleven-level inverter.

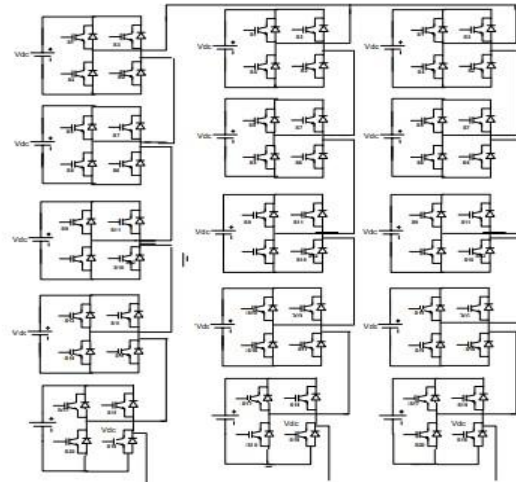


Fig. 1. Cascaded H-Bridge 11 Level Inverter

FFT analysis of a three phase 11 level inverter CHB shown below. Improving the fundamental waveforms and reducing the total harmonic distortion by using 60 IGBTs and switching is arranged by a topology in cascaded manners

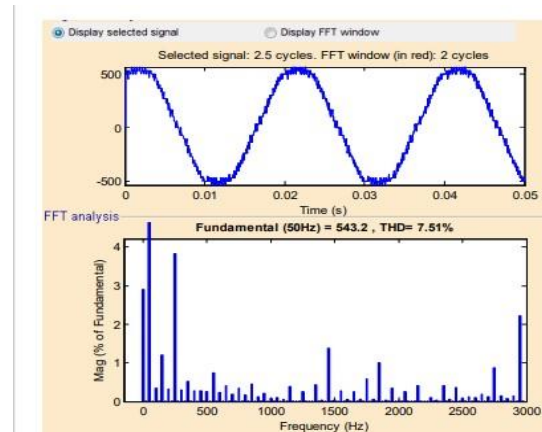


Figure 2: PWM Output Voltage and Harmonic Spectrum in 3 phase 11 level CHB Inverter.

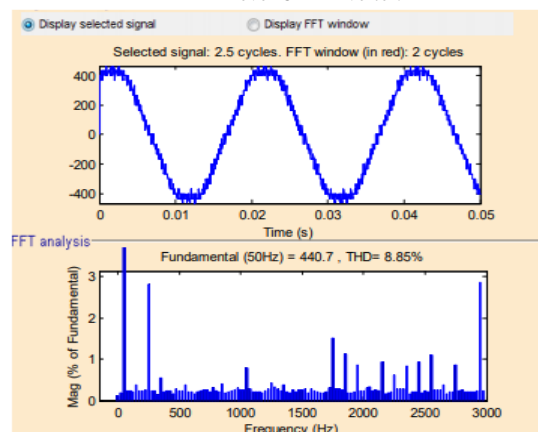


Figure .3: PWM output voltage and harmonic spectrum in three phase nine level CHB inverter (Modulation index 1.2)

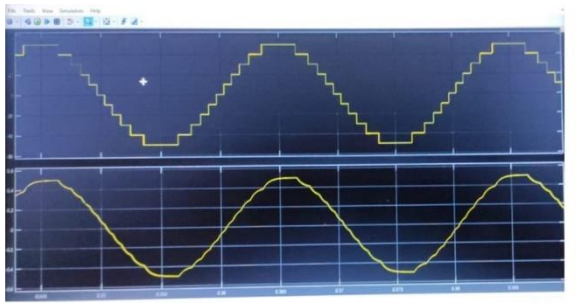


Fig:4Output Waveform of 11-level CHB MLI

(X-Axis:TimeY-Axis:The magnitude of voltage and number of input level)

TABLE -1: NO. OF COMPONENTS:- The number of required components for eleven level inverter is Table BELOW:

Inverter type	NPC	Flying Capacitor	Cascaded.	Proposed
Main switches	$2(N-1)$	$2(N-1)$	$2(N-1)$	$(N-1)+4$
Main diodes	$2(N-1)$	$2(N-1)$	$2(N-1)$	$(N-1)+4$
Clamping diodes	$2(N_2)$ $(N-1)$	0	0	0
DC bus Capacitor/Isolated supplies	$(N-1)$	$(N-1)$	$3(N1)/2$	$(N-1)/2$
Flying capacitors	0	$(N-1)$ $(N-2)/2$	0	0
Total numbers	$(N1)$ $(2N+1)$	$(N1)$ $(N+8)/2$	$11/2$ $(N-1)$	$(5N+11)/2$

TABLE 2: %THD comparison for different level and different Modulation Index

MODULATION INDEX	PWM PERCENTAGE THD FOR 11-LEVEL	PWM PERCENTAGE THD FOR 9-LEVEL
0.92	13.29	15.76
.95	12.10	14.76
.99	11.31	13.28
1	9.54	12.73
1.2	7.51	8.8

### 5. REDUCED SWITCH MULTI-LEVEL INVERTERS

Conventional Multi level Inverter topologies have several advantages and numerous applications but they are suffering from a more number of switch counts and their driving circuits and proportionally it increases as the number of levels increased which makes it complicated and resulted in a reduction of the system reliability. So the researchers are mainly focused on how to minimize the no. of switches of Multi-level Inverter. By reducing the no. of switches, no. of diodes, no. of capacitors, and no. of voltage sources a Recently Developed RS MLI, i.e., Reduced Switch Multilevel Inverter can optimize which results in the reduction of complexity, overall cost, and loss of the system.

### 6.MERITS:

- In recent years, multilevel inverters are attracting lot of attentions due to the increasing higher power quality requirements.

- It possesses the several features such as reduced harmonic distortion, near sinusoidal output voltage waveform and reduces dv/dt stress.
- The basic unit does not need any extra charge balancing control circuits and complicated commutation methods which counted as a great merit.
- The Internal resistance of power diode and capacitor can damp the unequal voltage between capacitor and DC voltage source during the charging operation which results to introduce an effective power circuit.

### 7.Demerits:

- The main drawback of multilevel inverters is that the number of switches increases with the no. of levels.
- In early stages of multilevel Inverters, development of control circuitry for large number of power switches was a significant problem but continuous evolution of CPLD, DSP & FPGA Devices solved these problems.
- Other Demerit of this MLI is the requirement of multiple numbers of DC sources, mainly provided by capacitors. Balancing the voltage sources during operation under different load conditions is much challenging.

### 8. CONCLUSION

The increase in requirement for electrical energy and the depletion of conventional resources makes the world's attraction towards the resources which are vast in nature and also efficient. So the researchers are focused on how to optimize and make the gadgets, equipment, and converting devices keeping in view factor of energy-efficient to achieve the present requirement of energy. A Multi-level Inverter is also a converting device on which a lot of research has been done, By reducing the counts of the components and minimized THD content present in the output of the inverters resulting into much efficiency. Now various new topologies named as reduced switch multi-level inverters come into practical application. Further researches are in progress for optimizing and minimizing the no. of switches and making the RSMLI more and more efficient. Multilevel cascaded H bridge inverters of 9 levels and 11 levels have been simulated using MATLAB. The following conclusions can be resulted from the analysis. If number of level increases, the Total Harmonic Distortion resulted into small value. Hence it results into elimination of the requirement of filters. Though, Total Harmonic Distortion decreases with increase in number of levels, Sometimes lower or Sometimes higher harmonic contents persist prevalent in each level. These harmonics will proved more dangerous in induction drives. Hence the future work may be focalized by applying closed loop control with suitable elimination of harmonics. **6.2**



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