

Cascaded 13 Level Inverter using Series Connection of SubMultilevel Inverters

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Abstract—Now a days Multilevel inverters are used extensively due to their increased power rating, with improving harmonic performance and reduced electromagnetic interference. In this paper, initially a new topology for submultilevel inverter is proposed and then series connection of the submultilevel inverters is proposed as a generalized multilevel inverter. The proposed 13 level multilevel inverter uses minimum number of switching devices. Special attention has been given to obtain optimal structures regarding different conditions such as number of switches, and standing voltage on the switches, number of voltage sources, etc. The proposed system will be tested using MATLAB/SIMULINK.

Index Terms — Generalized topology, multilevel inverter, optimal structure, submultilevel inverter.

I. INTRODUCTION

Multilevel inverters include an array of power semiconductors and dc voltage sources, the output of which generate voltage with stepped waveform in comparison with a two-level voltage-source inverter (VSI). The multilevel voltage source inverter enables to synthesize output voltages with reduced harmonic distortion and lower electromagnetic interference. By increasing the number of levels in multilevel inverter output voltage have more steps in generating a staircase waveform, which has a less harmonic distortion. Although a larger number of levels increases the number of devices that must be controlled and control complexity. As a result, the most attractive applications of this technology are in medium to high voltage ranges[1]. A multilevel inverter achieves high power ratings, and also enables the use of renewable energy sources such as PV cells, wind and fuel cells which can be easily interfaced to the multilevel inverter system for a purpose of high power application. The advantages of multilevel inverters are their smaller output voltage step, which results in voltage capability being high, lower harmonic components, low switching losses, and better electromagnetic compatibility and high power quality. It can also operate at both high switching frequency fundamental switching frequency PWM. The on field applications include use in laminators, pumps, compressors fans, blowers and mills. Simultaneously, several multilevel inverter topologies have been developed.

There are three different topologies have been proposed for multilevel inverters namely

1. Neutral point clamped multilevel inverter.
2. Flying capacitor multilevel inverter.
3. Cascaded H-bridge (CHB) multilevel inverter.

The Neutral point clamped multilevel inverter also called diode clamped can be consider the first generation of multilevel inverter introduced by Nabae et al., which was a 3 level inverter. The 3-level case of the NPC multilevel inverter has been widely applied in different fields. Unlike the Neutral point clamped type, the flying capacitor multilevel inverter offers some redundant switching states that can be used to regulate capacitors voltage. As the control scheme becomes complicated, the number of capacitors increases by increasing the number of voltage levels. The Cascaded H-bridge multilevel inverter use series connected H-bridge cells with the isolated dc sources connected to each cell. The CHB multilevel inverter can be divided into two groups from the point view of values of the DC voltage sources namely the symmetric and the asymmetric topology. Now In the symmetric topology, all the values of the DC voltage sources are equal. The characteristics give the topology better modularity. However, with the increase in the number of output voltage levels the number of switching devices rapidly increases. If the values of the DC voltage sources are different, then these topologies are called asymmetric topologies[2]. The Cascaded H-bridge multilevel inverters have been industrially employed in several application fields such as pumps, fans, compressors, mills, blowers. In addition, recently they have been proposed for other applications like PV power-conversion systems and wind power conversion.

This paper proposes a new multilevel inverter topology using series-connection of submultilevel inverters. The proposed following multilevel inverter uses less number of switches. Initially, the proposed SMI is described and then the series connection of them to form a MLI is discussed. The optimal structures of the proposed MLI regarding several factors are also obtained. The power loss of the present topology is calculated. Afterwards, the proposed MLI is compared with other multilevel inverter topologies considering the number of switches [5].

II. PROPOSED GENERALIZED MULTILEVEL INVERTER

A. Proposed Submultilevel Inverter

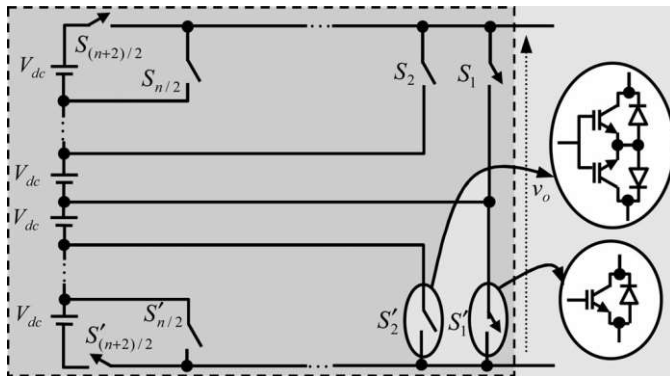


Fig 1. Proposed generalized submultilevel inverter.

Fig 1 shows the proposed sub multilevel inverter. As in Fig 1, the topology consists of n dc voltage sources. In general, dc voltage sources can have the different values. However, to have equal voltage steps, dc voltage sources are considered to be the same and equal to V_{dc} . Each SMI consists of $n + 2$ number switches. Some of the switches in the circuit are unidirectional and the others are bidirectional. The unidirectional switch consist of an insulated gate bipolar transistor with diode connected antiparallel to it. The switches S_1 , S_{-1} , $S_{(n+2)/2}$, and $S_{-(n+2)/2}$ are unidirectional and all other switches are bidirectional; hence, they have to be both positive and negative voltages. For instance, when $S_{(n+2)/2}$ is turned ON, voltage V_{dc} is on the switch $S_{n/2}$, and if the switch $S_{(n-2)/2}$ is turned ON, the voltage equal to $-V_{dc}$ is on the switch $S_{n/2}$. The same conditions are applicable for the other switches. Hence, the switches have to be both positive and the negative voltages. In addition, the switches should conduct the backward current that is as a result of inductive characteristics of the load. Therefore, It can be concluded that the switches must be bidirectional. There are some circuit configurations for bidirectional switches. The common emitter topology is used in this topology because it needs one gate driver for a switch. Looking at the types of the switches, $2n$ IGBTs are required in the following SMI. The number of the antiparallel diodes is equal to the number of IGBTs [4].

The proposed SMI can only generate zero and positive voltage levels. The zero output voltage is obtained when both the switches are turned ON at same instant. proper switching between the switches can generate other voltage levels. Table I shows the different states of the switches for each output voltage value. In this table, 1 means that the switch is turned ON and 0 indicates that the switch is in OFF state.

Considering Fig. 1, for each value of the output voltage of SMI, two switches must be turned ON, one from the lower switches and the other one from the upper switches of the circuit. For example, to get output voltage of V_{dc} , the switches S_{-1} and S_2 are turned ON. the switches $S_{n/2}$ and $S_{-(n+2)/2}$ should be turned ON in order to obtain the output voltage of $(n-1)V_{dc}$.

State	Switches states									v_o
	S_1	S'_1	S_2	S'_2	$\dots$	$S'_{n/2}$	$S_{n/2}$	$S_{(n+2)/2}$	$S'_{(n+2)/2}$	
1	1	1	0	0	$\dots$	0	0	0	0	0
2	0	1	1	0	$\dots$	0	0	0	0	V_{dc}
3	0	0	1	1	$\dots$	0	0	0	0	$2V_{dc}$
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\dots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
$n-1$	0	0	0	0	$\dots$	1	1	0	0	$(n-2)V_{dc}$
n	0	0	0	0	$\dots$	0	1	0	1	$(n-1)V_{dc}$
$n-1$	0	0	0	0	$\dots$	0	0	1	1	nV_{dc}

Table 1. Output voltages for states of switches

B. Proposed Generalized Multilevel Inverter

To achieve the desired voltage and number of voltage levels The proposed submultilevel inverters is connected in series. Fig 2 shows m submultilevel inverters connected in series. Each SMI has n number of dc voltage source. The dc voltage source in each SMI are equal. The output voltage of the SMI are always positive or zero. It is necessary to change the voltage polarity in every half cycle to operate as an inverter. For this purpose an H-bridge inverter is added to the output of the series connected SMI. It is important to note that the switches of the H-bridge must have higher voltage. This is to be considered in the design of the inverter. However, switches are turned ON and OFF once during a fundamental frequency cycle. hence, these switches would be high-voltage low-frequency switches[3].

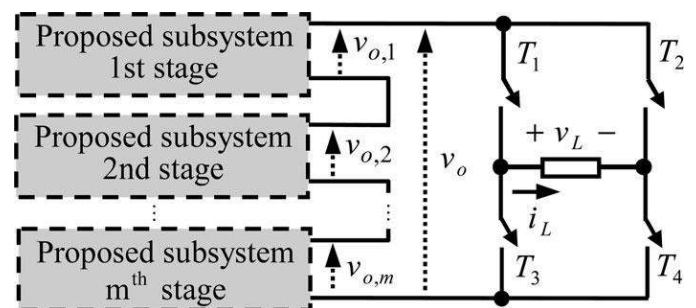


Fig 2. Proposed general multilevel inverter using series connection of m proposed SMI, each one has n dc voltage sources.

III. SIMULATION RESULTS

For the simulation the load is an R load with the value of 45 Ω . The output voltage frequency is assumed 50 Hz. There are many other control methods used for multilevel inverter. It can be observed that the staircase control method is used in this multilevel inverter. The term staircase control method is used to state that in this method, transition from one level to the other level happens once. This control method tends to generate a staircase voltage which minimizes the error with respect to the reference voltage.

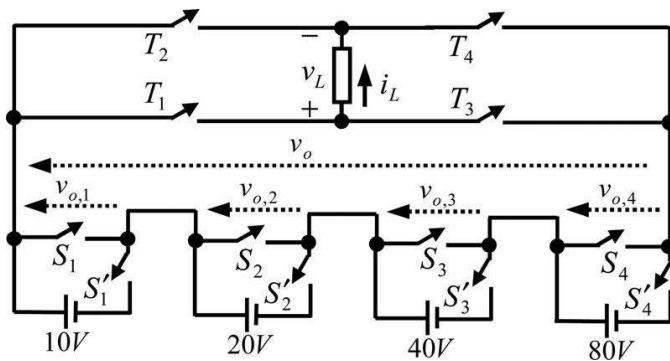


Fig. 3. Thirteen-level inverter based on the proposed Asymmetric topology with $n = 1$ and $m = 4$.

Fig. 3 shows the 13-level inverter based on the proposed symmetric multilevel inverter with $n=1$. Four dc voltage sources 90V, 45V, 23V, 12.5V have been used so that the maximum output voltage will be 170V. The number of IGBTs for a 13-level inverter in the proposed topology is 12.

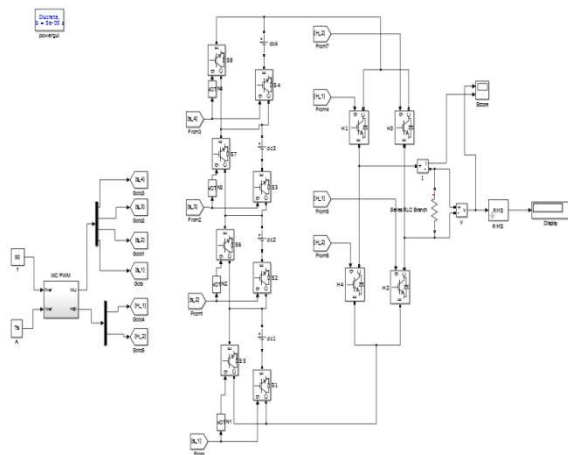


Fig 4. Schematic of thirteen level inverter.

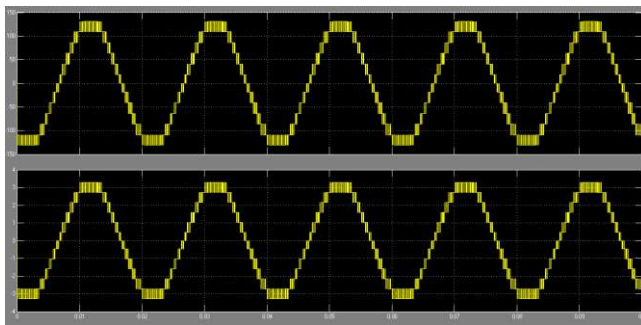


Fig 5 output voltage of thirteen level

Fig 5 shows the output voltage of the cascaded submultilevel inverters. The polarity of the voltage is changed using the H-bridge connected to the output of the submultilevel inverters. In the test condition ($R = 45$, $V_{o,max} = 100$ V), the power loss of the proposed multilevel inverter, shown in Fig. 5, is about 12W. However, the power loss of the asymmetric CHB topology with the same conditions (with the same value of voltage and load) is about 15.5 W. It can be as a result of the fact that in the following topology less semiconductor devices are in the current path in any instant of time in comparison with the asymmetric CHB topology. In this condition, active output power of the inverter is about 217 W.

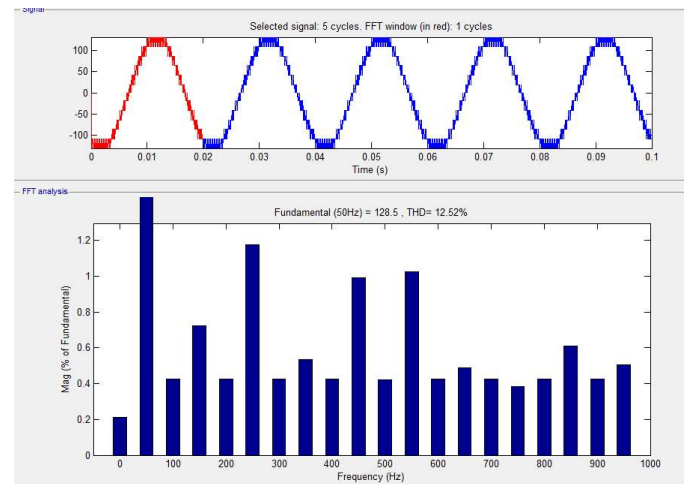


Fig 6. Total harmonic distortion

Fig 6 shows the total harmonic distortion. The proposed topology has the advantage of its reduced number switches and harmonics are reduced with THD value of 12.52 at 128.5V is achieved. For proposed harmonic spectrum of the simulation system is as shown in the fig.4, which shows the results are well within the specified limits of IEEE standards. The results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB.

IV. CONCLUSION

A multilevel inverter with individual dc sources has been proposed for use in large electric drives. Simulation results have shown that with the control strategy operates the switches at the fundamental frequency, the converters have low output voltage, Total Harmonic Distortion(THD), high efficacy and power factor.

Simulation has been done in the MATLAB /SIMULINK. From the simulation it is noted that new MLI topology works well and shows hope to reduce the cost and complexity. Whenever the output voltage levels gets increased, the number of switches will be used is very less compared to other multilevel topologies. By the increase in output voltage levels the total harmonic distortion starts get reduced, so that it can be used in many power applications.

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