Capacitance Scaling Based Energy Efficient Internet of Things (IoTs) Enable CAM Design on FPGA

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***Abstract*—This paper deals with Capacitance scaling based Energy Efficient Content Addressable Memory. We have analyzed IO power reduction by scaling down the capacitance from 4000pF to 50pF with intermediate value of 2000pF, 1000pF, 500pF at different frequencies i.e. 1 GHz, 2.4 GHz, 3.6 GHz, 4.9 GHz, 5 GHz, 5.9 GHz, 60 GHz bands of WLAN channels. We have tested the compatibility of our device with wireless network by operating it on different frequency ranges of WLAN Channel. There is 79.57% reduction in IO power, when we scale down capacitance from 4000pF to 50 pF at 1 GHz and 93.33% reduction in IO power, when we scale down capacitance from 4000pF to 50 pF at 60 GHz. In this work, we are using 28nm technology based Kintex-7 FPGA and Verilog Hardware Description Language. Our CAM is Internet of Things (IoTs) enabled in which we are using 128 bit IP address of Internet Protocol Version 6 (IPv6). With the help of this IP address, connectivity to the different objects from this CAM can be provided.**

Keywords*—*Capacitance, Energy Efficient, Internet of Things, Content Addressable Memory.

I. INTRODUCTION

Core dynamic power is not dependent on output load capacitance [1]. IO power and static power is dependent on output load capacitance [1]. There is 99.72% reduction in IOs power consumption of Universal Asynchronous Receiver Transmitter (UART) when output load is scaled from 10,000pf to 5pF in IOB setting of FPGA [1].

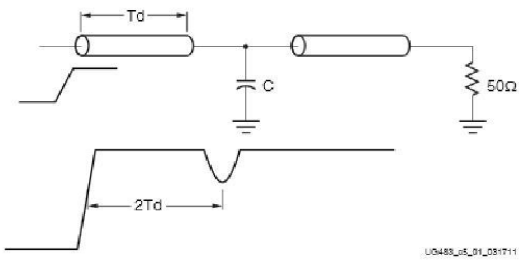

Figure 1: Shunt Capacitance for Reduction in Impedance [1]

Fig.1 shows the shunt capacitance which reduces the impedance that ultimately reduces overall power consumption of our device [2]. Memory mainly refers to the physical device used to store the sequence of instructions (program), data permanently or temporarily. Memory devices usually store and retrieve data with the use of address at specific memory location.[3-15] Different types of memories used are Random Access Memory (ROM), Content Addressable Memory (CAM) etc. The only difference in these type of memories is the way in which the data is fetched. In case of RAM the user supplies the memory address and in return data word [8] stored at that memory address is given to the user. On the other hand CAM is designed to make it easy for the user to search data by simply searching the data through the content [12]. In CAM user supplies the data word that is related to the data to be searched and CAM tries to search its entire memory to find the presence of data anywhere in its memory. On the result of this search , list of storage addresses are given where the data word was present. As compared to the other memory devices CAM is fast in all the searching application.[4] due to which CAM is used for High Speed search operation [13]. CAM involves a large amount of circuitry due to which it is more power consumptive [12]. So we use CAM only at those places where the slow speed is not tolerable. Two types of CAM mainly used are Binary CAM, ternary CAM [4]. Binary CAM uses data search words containing 0s and 1s, on the other hand Ternary CAM uses a third state i.e 'Don't Care' or 'X' [9] which making our searching process more effective. For e.g. Ternary CAM [10] can have a stored word "X010X" which will match any of these words "10101", "10100", "00101", "00100". It increases our option for search by making it more flexible but also increases the cost of it .CAM that we are going to design is Capacitance based which means the ability of an object to store the electric charge [3]. Any object (body) that can be electrically charged exhibits capacitance. The output load is the sum of capacitance of pin and capacitance of device. The unit of capacitance is Farad but we have used pico Farad (pF) which is one trillionth (10^{-12}) of a farad [4]. Power that is directly proportional to capacitance reduces when capacitance is reduced i.e when we reduce capacitance, and then there is reduction in IO power, leakage power. In the cases below there is no significant difference in the leakage power but in IO power and the total. Energy is being saved through this

device which varies from 79.57% to 93.33% by using different frequencies bands (1 GHz, 2.4 GHz, 3.6 GHz, 4.9 GHz, 5 GHz, 5.9 GHz, and 60 GHz).

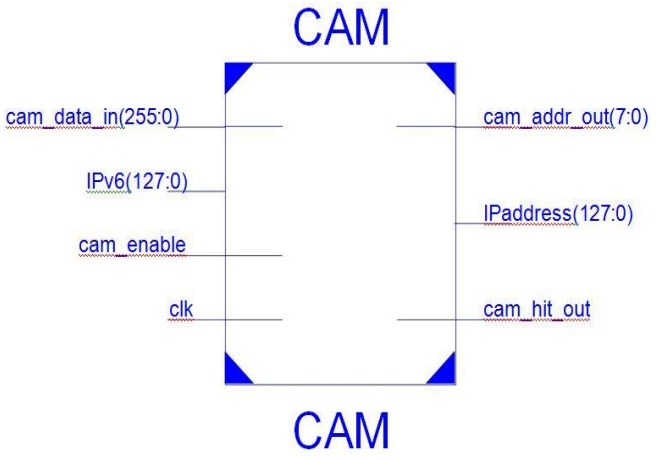

Fig. 2: Top Level Schematic of CAM

In this research we have used 9 register, 9 Flip-Flops, 507 multiplexers out of which 254 are 1-bit 2-to-1 multiplexer and 253 8-bit 2-to-1 multiplexer. Other components are 599 basic elements (BELS) which contains 1 inverter (INV), 3 LUT2 (Look Up Table), 69 LUT3, 65 LUT4, 224 LUT5, 237 LUT6, 9 Flip-flops/Latches (D Flip Flop with reset), 1 clock buffer (BUFGP), 266 IO Buffers out of which there are 357 Input Buffer (IBUF) and 9 output buffer (OBUF). Our CAM is Internet of Things (IoTs) [5] enabled in which we are using 128 bit IP address of Internet Protocol Version 6 (IPv6) [3]. With the help of this, connectivity to the different objects from this CAM can be provided. Earlier, Capacitance scaling is used to design energy efficient UART [1], power optimized Register [2], and ALU [15]. Here, we are extending that approach to energy efficient CAM.

II. RESULT

Unit of capacitance is Farad (F). The output load capacitance is in range of 50pF-4000pF. We are doing power analysis in form of clock power, logic power, signal power, IO power, and leakage power. Unit of power is Watt (W). Power is directly proportional to capacitance and frequency. Therefore, power dissipation will increase with increase in either capacitance or frequency or both.

A. When CAM is Operating at 1 GHz Frequency.

TABLE 1: POWER DISSIPATION AT DIFFERENT CAPACITANCE

C→ Power↓	50pF	500pF	1000pF	2000pF	4000pF
Clock	0.008	0.008	0.008	0.008	0.008
Logic	0.005	0.005	0.005	0.005	0.005
Signal	0.024	0.024	0.024	0.024	0.024
IO	0.029	0.042	0.056	0.085	0.142
Leakage	0.147	0.147	0.147	0.147	0.148
Total	0.213	0.226	0.240	0.269	0.326

There is 79.57% reduction in IO power, when we scale down output load capacitance from 4000pF to 50pF at 1 GHz as shown in Figure 3 and Table 1.

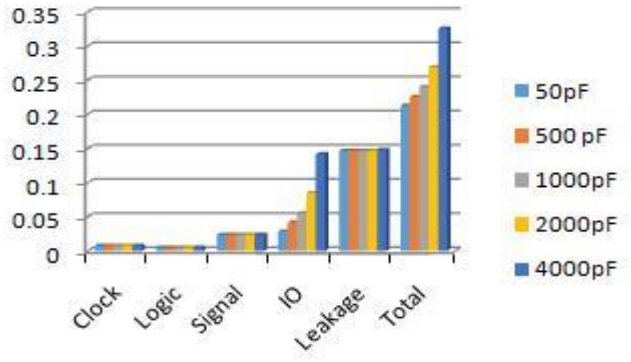

Fig. 3: Power Dissipation at 1GHz Frequency and Different Capacitance

B. When CAM is Operating at 2.4 GHz Frequency.

TABLE 2: POWER DISSIPATION AT DIFFERENT CAPACITANCE.

C→ Power↓	50pF	500pF	1000pF	2000pF	4000pF
Clock	0.019	0.019	0.019	0.019	0.019
Logic	0.011	0.011	0.011	0.011	0.011
Signal	0.058	0.058	0.058	0.058	0.058
IO	0.076	0.150	0.232	0.396	0.724
Leakage	0.148	0.148	0.149	0.151	0.155
Total	0.312	0.387	0.470	0.636	0.967

There is 89.50%, reduction in IO power, when we scale down capacitance from 4000pF to 50pF at 2.4 GHz device operating frequency as shown in Figure 4 and Table 2. The frequency of WLAN Channel 802.11b/g/n is 2.4 GHz.

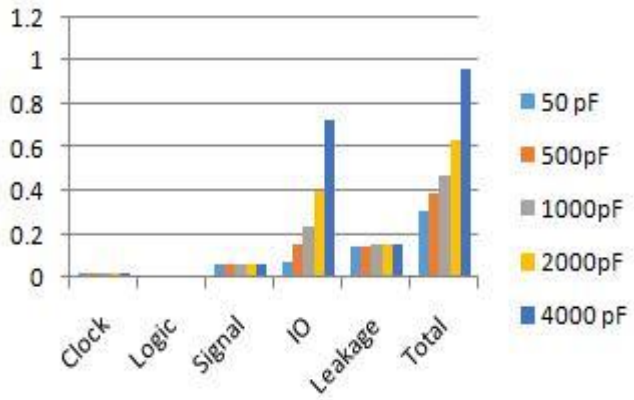

Fig. 4: Power Dissipation at 2.4GHz Frequency and Different Capacitance

C. When CAM is Operating at 3.6 GHz Frequency.

TABLE 3: POWER DISSIPATION AT DIFFERENT CAPACITANCE.

C→ Power↓	50pF	500pF	1000pF	2000pF	4000pF
Clock	0.029	0.029	0.029	0.029	0.029
Logic	0.017	0.017	0.017	0.017	0.017
Signal	0.087	0.087	0.087	0.087	0.087
IO	0.118	0.253	0.404	0.706	1.310
Leakage	0.149	0.150	0.152	0.155	0.162
Total	0.399	0.536	0.689	0.994	1.605

There is 90.99%, reduction in IO power, when we scale down capacitance from 4000pF, 2000pF, 1000pF, 500pF, 50pF at 3.6 GHz as shown in Figure 5 and Table 3. The frequency of WLAN Channel 802.11y is 3.6 GHz.

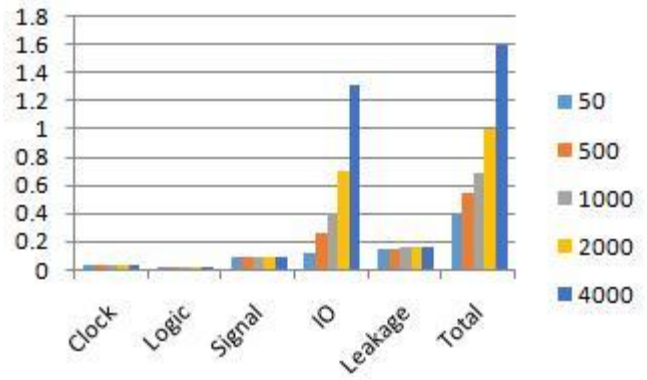

Fig. 5: Power Dissipation at 3.6GHz Frequency and Different Capacitance

D. When CAM is Operating at 4.9 GHz Frequency

TABLE 4: POWER DISSIPATION AT DIFFERENT CAPACITANCE

C→ Power↓	50pF	500pF	1000pF	2000pF	4000pF
Clock	0.039	0.039	0.039	0.039	0.039
Logic	0.023	0.023	0.023	0.023	0.023
Signal	0.119	0.119	0.119	0.119	0.119
IO	0.162	0.362	0.585	1.029	1.918
Leakage	0.150	0.152	0.154	0.159	0.170
Total	0.493	0.695	0.920	1.369	2.269

There is 91.55%, reduction in leakage power, when we scale down capacitance from 4000pF, 2000pF, 1000pF, 500pF, 50pF at 4.9 GHz as shown in Figure 6 and Table 4.

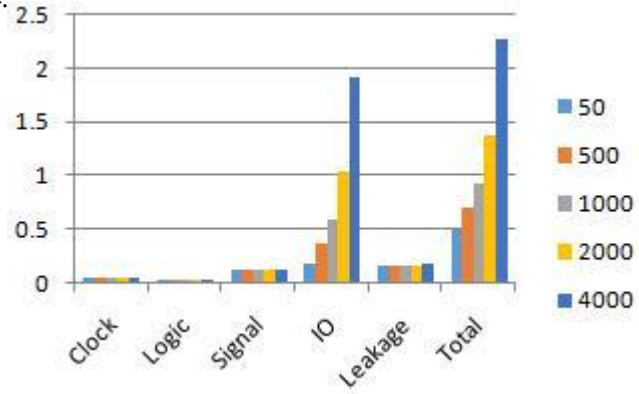

Fig. 6: Power Dissipation at 4.9GHz Frequency and Different Capacitance

E. When CAM is Operating at 5 GHz Frequency

TABLE 5: POWER DISSIPATION AT DIFFERENT APACITANCE

C→ Power↓	50pF	500pF	1000pF	2000pF	4000pF
Clock	0.040	0.040	0.040	0.040	0.040
Logic	0.023	0.023	0.023	0.023	0.023
Signal	0.121	0.121	0.121	0.121	0.121
IO	0.166	0.371	0.599	1.055	1.968
Leakage	0.150	0.152	0.154	0.159	0.170
Total	0.500	0.708	0.938	1.400	2.323

There is 91.56%, reduction in IO power, when we scale down capacitance from 4000pF, 2000pF, 1000pF, 500pF, 50pF at 5 GHz as shown in Figure 7 and Table 5.

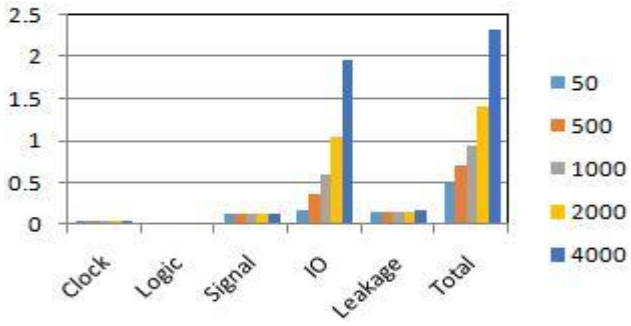

Fig. 7: Power Dissipation at 5GHz Frequency and Different Capacitance

F. When CAM is Operating at 5.9 GHz Frequency

TABLE 6: POWER DISSIPATION AT DIFFERENT CAPACITANCE

C→ Power↓	50pF	500pF	1000pF	2000pF	4000pF
Clock	0.047	0.047	0.047	0.047	0.047
Logic	0.028	0.028	0.028	0.028	0.028
Signal	0.143	0.143	0.143	0.143	0.143
IO	0.197	0.452	0.735	1.302	2.425
Leakage	0.150	0.153	0.156	0.163	0.176
Total	0.565	0.823	1.110	1.682	2.829

There is 91.87%, reduction in leakage power, when we scale down capacitance from 4000pF, 2000pF, 1000pF, 500pF, 50pF at 5.9 GHz as shown in Figure 7 and Table 6.

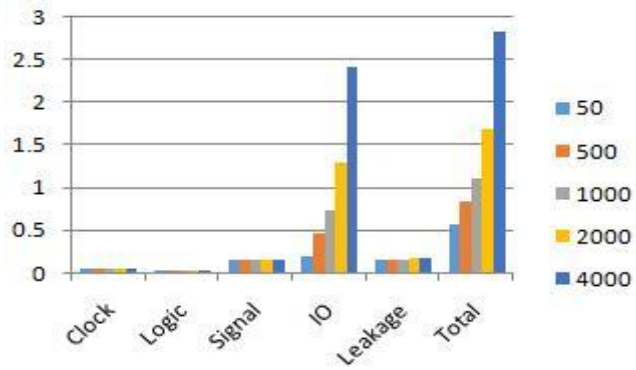

Fig. 8: Power Dissipation at 5.9GHz Frequency and Different capacitance

G. When CAM is Operating at 60 GHz Frequency

TABLE 7: POWER DISSIPATION AT DIFFERENT CAPACITANCE

C→ Power↓	50pF	500pF	1000pF	2000pF	4000pF
Clock	0.482	0.482	0.482	0.482	0.482
Logic	0.111	0.111	0.111	0.111	0.111
Signal	1.325	1.325	1.325	1.325	1.325
IO	2.114	5.486	9.233	16.727	31.715
Leakage	0.195	0.248	0.323	0.539	0.993
Total	4.227	7.653	11.475	19.184	34.626

There is 93.33%, reduction in IO power, when we scale down capacitance from 4000pF, 2000pF, 1000pF, 500pF, 50pF at 60 GHz as shown in Figure 8 and Table 7.

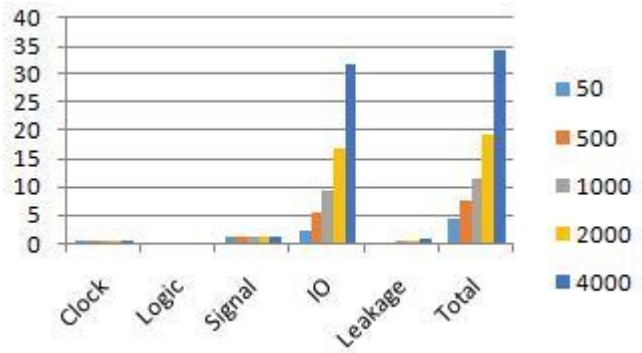

Fig. 9: Power Dissipation at 60GHz Frequency and Different Capacitance

III. CONCLUSION

We achieved Capacitance scaling based energy efficient Internet of Things enabled Content addressable memory Design on FPGA. We used capacitance as a main parameter and by operating device on different capacitance and Wireless network channels using IEEE 802.11 protocols at different frequency range from 1 GHz to 60 GHz we have shown how the power is saved. The CAM design we represented is energy efficient as we can see the reduction in IO power i.e 93.33%-79.57% when we scale down capacitance from 4000pF to 2000pF,1000pF, 500pF,50pF. Although there is no significant reduction in Leakage power, signal power, Clock power but there is reduction in IO power and Total power.

IV. FUTURE SCOPE

In the near future we will design the Energy efficient Internet of things enabled ALU on FPGA. We will also use Ubiquitous computing in our design which is the part of internet of things. We have used 2D IC in this paper but we will implement the design in future using 3D, 4D IC. We have implemented this CAM using 28 nm FPGA, but there is a large scope of implementing CAM on 14nm, 32nm, 40nm, 90nm and large scale FPGA. This design is energy efficient but we can make high performance CAM that will be internet of things enabled.

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