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BLDC Motors – A Survey of Topologies, Control & Applications

Dr. B. Mahesh Kumar[1] Mr. R. Babu Ashok[2]
[1]Associate Professor, [2]Research Scholar
Department of Electrical & Electronics Engineering
Pondicherry Engineering College, Pondicherry – 605 014

Abstract:- **Brushless DC (BLDC) motors are widely used from hard disc to hybrid electric vehicle. The major menace is power quality issues which include Power Quality (PQ) indices viz.DPF (Displacement power Factor), PF (Power Factor) CF (Crest Factor) and THD (Total Harmonics Distortion) of the supply current at AC mains with in specified limit by International Electro Technical Commission PQ standards viz IEC 61000-3-2 , IEC 555-2 and IEC-519 of speed control for class-A equipment < 600W, 16 A per phase. Machine control and drives could be optimized by applying different control techniques. Various methods for PFC such as buck, boost, buck/boost, Cuk, SEPIC, Zeta, push-pull, half bridge, full bridge are presented based on the motor control side.**

Key words: Brush less DC motor (BLDC), PFC (Power Factor correction)

INTRODUCTION:

The harmonic effects are excessive heating, reduced torque in motor/generator, increased voltage stress across capacitor, maloperation in electronic gadgets like switchgear / relays and ultimately reduced life span. Harmonics if unspecified means harmonic current rather than harmonic voltage.

For example the sum of fundamental current (I_1) 100 A and fifth harmonic (I_5) 20 A=102 A (not 120 A) due to root –sum-square.

The AC mains supply waveform is non sinusoidal because DBR does not draw current when the AC voltage is less than the DC linkage voltage (diodes reverse biased) but draws maximum current when AC voltage is higher than DC link voltage. Hence it results in pulsed input current waveform whose value is higher than the peak value of the fundamental input current. It shows 83.13% total harmonic distortion (THD) permissible limit < 19%, 2.3 crest factor and 0.723 power factor permissible limit > 0.9 at AC mains [1].

It is otherwise known as (ECM) electronically commutated motor and having trapezoidal back emf waveforms and are fed with rectangular stator currents. Cost and circuit complexity are the important factors for design tradeoffs between technology and design hardware.

The objective of using PFC converter is to draw sinusoidal supply current in phase with supply voltage. The various topologies suggested are boost, buck, buck-boost, fly back, forward, push-pull, cuk, SEPIC, zeta half bridge, full bridge PWM-VSC etc.

BOOST CONVERTER TOPOLOGY

It is a high speed switching device and one of the switching mode regulators i.e. to convert unregulated DC to regulated DC realized by PWM using the switching device BJT, MOSFET or IGBT. IGBT’s are preferred because it has high input impedance, low on state conduction loss and low switching loss. It is a power converter where output DC voltage is greater than input DC voltage but reduced output current (power, P=V*I is constant) containing 2 semiconductor switches (a diode and a transistor) and at least one storage element (L or C). LC Filters are connected to the output of the converter to reduce voltage ripple. Filter size increases when the harmonic frequency decreases and vice versa [2].

When the source ground and load ground are physically connected to each other i.e, electrically and magnetically then the circuit is said to be non-isolated one.

- Used in battery powered systems like hybrid electric vehicles.
- Portable lighting systems.
- Operation of cold cathode fluorescent tubes

When the source ground and load ground are not physically connected to each Other i.e., electrically and magnetically then the circuit is said to be non-isolated one. The main advantages are isolation, voltage step up/ down and for high frequency switching, size is reduced and vice versa. Multiple outputs provide the possibility of feeding different loads simultaneously. It is used in sensors, controls and safety equipments.

The Switch and diode are designed is such a way that the maximum current it has to handle is twice the load current. Under steady state condition the value of inductance L= $\frac{RD(1-D)^2}{f}$ and C=$\frac{D}{RfV_o}$ Where L is inductance, R is load resistance D-Duty ratio, f is switching frequency and C is Capacitance of capacitor.

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The converter can operate in two distinct modes with respect to inductor current i_L.In CCM the inductor current is always greater than zero. When the average values of the output current is low or the switching frequency 'f' is low the converter may enter DCM.

The CCM is preferred for the high efficiency and good utilization of semiconductor switches and passive components. DCM is used in special control requirements because the dynamic order of the converter is reduced because the energy stored in the inductor is zero at the beginning and at the end of each switching period [3]. It is uncommon to mix these 2 operating modes because of different control algorithms.

BUCK CONVERTER TOPOLOGY

Buck converter is a step down type i.e.$V_o < V_i$ .There are 2 types of dynamics viz.

1.Switching- caused by the switching of transistors , are high frequency (hundreds of KHz).

2.External dynamics- caused by external perturbations such as load or input voltage, low frequency (hundreds of KHz). A unidirectional buck converter replaces transformer with an auxiliary inductor reduces the size and weight of the converter [4]. The conversion efficiency can be 90% by setting 0.2 to 0.9 as the degree of coupling of the coupled inductor.

BUCK BOOST CONVERTER TOPOLOGY

In CCM the inductor has some definite minimum value before time t=0. When switch is ON, the first sub interval of the switching period starts.

The inductor current starts increasing from its minimum values [5]. The diode is reverse biased and thus off. The output capacitor supplies the load in this sub-interval and therefore it is discharged too. The inductor current increases till the switch is made off. The off command can be obtained from the controllers using either (PWM) pulse width modulation or (PFM) pulse frequency modulation. When the switch is made off in the second sub-interval, the inductor depletes the energy partly through the output capacitor and partly to the load. In CCM, switch is turned on before the inductor current reaches zero. The switches are selected for maximum input voltage and maximum inductor current while the diode should withstand load current and load voltage.

The complex controllers are preferred for medium and high power BLDCM. This paper has 9 major parts namely Introduction, State of the art, Classification of PFC topologies, Operation & Control of PFC topologies, Design of PFC topologies, Performance evaluation of PFC topologies, Chaos and constraints in converters, Application potentials and Conclusion.

2 State of the art:

BLDC AND PMSM are widely used for domestic purposes eg. Fans AC, refrigerator, washing machines and dish washers. In which BLDC is preferred because of wide range of speed control especially in low power and ASD. Hence BLDC must satisfy the PQ norms and controlled in the front end. Through many literatures using different converter topologies are suggested but only few confined to PQ analysis and improvement in BLDCM drives.

The efficiency of PMBLDC motor traction drive system is improved by the bidirectional DC-DC converter bridging the source and motor. It also facilitates the energy regeneration during braking, improves the efficiency by 25%. During motoring mode the convertor operates in boost mode the converter and during regeneration acts as generator (i.e. buck mode) to recharge the battery. Absence of transformer reduces the size, weight and cost. This converter is usually designed with voltage source on both the sides hence entire unit acts as fifth order system and becomes complicated. Small dead time is provided during mode transition in order to avoid cross conductance through 2 switches and the convertor output capacitance. The switching loss of VSI increases as square of switching frequency. To reduce switching loss fundamental frequency is reduced. The speed control is achieved by the variable DC link of VSI.

Non-isolated half bridge topology is suitable in high power applications of space craft. The switching losses are reduced by soft switching techniques like Zero Voltage Resonant Technique (ZVRT) is preferred to reduce switching losses.

A Load Commutated Inverter LCI configuration has been suggested for BLDCM. Four quadrant working using current sensorless control scheme is employed but shows sluggish performance during starting.

A new topology with bipolar excitation is named as 'three phase four switch topology' with reduced switching stress is modified for PF correction with six switches [6]. This configuration has the advantages of single phase to three phase conversion with PF close to UPF, enables regenerative braking due to bidirectional current flow between AC supply and BLDCM via DC link. Using Digital Speed Processor (DSP) or Field Programmable Gate Array (FPGA), symmetric PWM scheme is used for triggering the power electronic switches.

By compromising the performance, low cost converters using unipolar excitation of BLDCM is analyzed. The C-dump converter combined with a split supply converter, called as variable DC link topology. It is suitable for low voltage rating and four quadrant operation. Non-isolated PFC converter topologies for unipolar VSI based PMBLDCM drives. By modulating the duty cycle of the convertor switch it ensured the overall system is stable during dynamic conditions. By tracking the current and

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voltage, the power factor obtained at the front end is more than 0.9 and the input current THD is less than 5%.

Power quality converters either be isolated [7] or non-isolated can operate in CCM or DCM. CCM offers an advantage of reduced stress on PFC converter switch but requires higher amount of sensing thus preferred in medium and high power applications. In DCM only a DC link voltage sensing is required hence suitable for low power applications < 1KW.

3. Classification of PFC topologies for PMBLDCM

PFC controllers should confirm not only PQ norms but also cost, compactness and reliability of the controllers Half bridge and push pull configuration use two power switches and work either in buck or boost mode. To reduce switch count three phase four switch inverter is suggested without any input filter. The combination of diode rectifier and step down chopper forms buck PFC Converter having input and output filter for reducing THD of AC mains and ripples at DC output voltage.

The combination of DBR and step up DC chopper is boost PFC Converter having filtering and energy storage elements Using the principle of interleaved or multi cell arrangements and hybrid Schemes to monitor the performance. In the inner current control HF PWM and hysteresis current controls are used. Similarly wide bandwidth Closed loop controllers are practiced in outer voltage loop to meet the PQ standards.

The combination of diode rectifier with buck-boost DC-DC Converter is known as buck-boost converter in isolated and non isolated topologies. In addition to buck-boost mode it operates as fly back,

SEPIC, Zeta, Cuk. In isolation topology HF transformer gives voltage adjustment, motor safety, reduction in weight, size, losses and compactness. It also meets PQ standards almost UPF, low THD from the input AC supply. A large inductor maintains constant current at DC link in the CSI based PFC topology

4. Operations and control of PFC topologies for PMBLDCM drives

The operation is based on two modes [8] viz.

1. Continuous Conduction Mode (CCM)-inductor current is always positive. In CCM the current in the inductor or the voltage across the intermediate capacitor remains continuous but it requires the sensing of 2 voltages (DC link voltage and supply voltage) with input side AC current for PFC operation hence it is not cost effective.

2. Discontinuous Conduction Mode (DCM) – inductor current is zero during off period.DCM requires a single voltage sensor for DC link voltage control and inherent PFC is achieved at the AC mains but at the cost of higher stress on the PFC converter switch hence DCM is suitable for low power applications.

Table.No:01.Comparison of half and full bridge

Sl.No	Characteristics	Half Bridge	Full Bridge
1.	No. of switches	less	More
2.	Cost	low	high
3.	power handling	nominal	double
4.	control scheme	same	same
5.	switching stress	low due to HF isolation transformer	low

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The controllers used are (PI) proportional Integral, Fuzzy Logic controllers (FLC) and Neural – network (NN) with software algorithms. The complexity is reduced by control algorithm.

5. Design of PFC topologies for PMBLDCM

The switching device decides the switching frequency, switching losses, voltage, power and the maximum junction temperature of the device. The inductance limits current ripple and capacitance limits voltage ripple.

HF transformers provide isolation between input & output supply, reduced size, cost, weight and voltage matching. The design of the transformer depends upon the voltage ratio, power rating of the drive and switching frequency.

The PWM strategy is designed for the maximum value of duty ratio as 0.5 for all types of buck converters (i.e. buck forward, half bridge, full bridge, push pull). Moreover it is designed for 100 V DC output and 300W power rating only whereas boost and buck boost converters are designed for 400 V DC and 1200 W power rating.

Boost PFC converters can function in isolated and non isolated configurations with single, two and four switches. Duty ratio lies between 0 and 1 for non isolated single switch boost converter but the half bridge, full bridge and push pull are designed for D as 0.5.

The cuk, SEPIC and Zeta converters work for constant voltage capacitor due to the principle capacitive energy transfer but fly back converters are intended for constant current through the inductor due to the operating principle inductive energy transfer.

6. Performance evaluation of proposed PFC Topologies

The BLDC motor is modeled in MATLAB / Simulink environment for a VSI fed motor. Initially the motor is started with no load and later load is applied. Under steady state condition PQ is monitored through FFT (Fast Fourier Transform) analysis at AC mains.

Modeling of PMBLDC motor drives

For the simplified analysis and simulation purpose few assumptions are made in BLDC motor [9].
The assumptions are

1. Three phase windings are symmetrical i.e., balanced system.
2. Magnetic saturation is neglected.
3. Hysteresis and eddy current losses are not considered.
4. Inherent stator resistances of each motor winding are R and self-inductances are L and they are considered as constant.
5. Stator winding are wye- connected hence zero sequence quantities are absent.
6. Damper windings are not modeled.
7. Both the Magnet and the stainless steel retaining sleeves have high resistivity hence rotor induced current can be neglected.
8. No field current dynamics.

The supply voltage pertaining to each phase of the winding can be written as

$$V_a = Ri_a + L\frac{di_a}{dt} + e_a \qquad ------- (1)$$

$$V_b = Ri_b + L\frac{di_b}{dt} + e_b \qquad ------- (2)$$

$$V_c = Ri_c + L\frac{di_c}{dt} + e_c \qquad ------- (3)$$

As per Newton's second law of motion the angular motion of the rotor is

$$T_e(t) - T_l(t) = J\frac{d\omega(t)}{dt} + B + \omega(t) ----- (4)$$

6.1 Speed controller

The types of speed controllers are PI, Fuzzy precompensated PI (FPPI), sliding mode (SM), hybrid fuzzy PI, NN based and neuro- fuzzy.

6.2 Modeling of PMBLDC motor

This can be represented by the first order differential equations

$$pi_x = \frac{(v_x - i_x R - e_x)}{(L_s + M)} \qquad -------(5)$$

$$p\omega_r = \frac{(p/2)(T_e - T_1)}{(J)} \qquad ----- --(6)$$

$$P\theta = \omega_r \qquad -------(7)$$

$$f(\omega t) = \frac{\pi}{6}t, \quad 0 \le \omega t \le \frac{\pi}{6} \quad -------(8)$$

$$f(\omega t) = 1, \quad \frac{\pi}{6} \le \omega t \le \frac{5\pi}{6} \quad -------(9)$$

$$f(\omega t) = 1 - \frac{1}{\pi}(6\omega t - 5\pi), \frac{5\pi}{6} \le \omega t \frac{7\pi}{6} \quad -------(10)$$

$$f(\omega t) = -1 + \frac{(6\omega t - 5\pi)}{\pi}, \frac{11\pi}{6} \le \omega t \le 2\pi \quad -------(11)$$

$$f(\omega t) = -1, \quad \frac{7\pi}{6} \leq \omega t \leq \frac{11\pi}{6} \qquad ------(12)$$

7. CHAOS & CONSTRAINTS IN CONVERTERS

Power electronic Switches are associated with reactive components (inductance, capacitance and transformers). Some of the assumptions are

Switches are ideal

i.e. i) Zero ON state losses
ii) Zero OFF state losses
iii) Zero Switching state losses
iv) Unlimited voltage/current carrying capability

The function of inverter is to change a DC input voltage to a symmetric AC output voltage of desired magnitude and frequency. Switching devices must operate in the saturation region in order that the ON state voltage drops as well as the power dissipation is low.

Table.No:6 the PQ performance parameters remain within the limit imposed by international PQ standards

S.No	Converter Topology	THD	P.F	C F
1.	Non isolated boost	1.19%	0.999	1.44
2.	Isolated forward boost	0.91%	0.999	1.43
3.	Non isolated buck-boost	4%	0.998	1.42<CF> 1.51
4.	Isolated boost, buck-boost	<2%	0.999	1.43<CF>1.47
5.	Isolated buck	High	0.999	1.44<CF>1.51
6.	Bi directional VSC	2.3%	0.999	1.43

The output DC voltage ripple is less than 5% for boost and buck-boost topologies but less than 10% in case of buck PFC topology. Various performance parameters of PFC controllers like cost, control complexity are summarized in Table No.6. Steady state efficiency is 90%

The characteristics of source voltage (V_s), source current (i_s), motor phase current (i_a), average DC link voltage (V_{dc}), rotor speed (N) and electromagnetic (T_e) for a BLDCM under transient and steady state condition shows the response under starting, load conditions shows near UPF. The performances of current and torque ripples are reduced in all conditions.

Table.No:8

PFC topology	Option
Single switch	**Low power, <500w**
Two / four switch	**1 – 4 kw**

In low power drives, buck PFC topology is preferred for PQ improvement. The buck PFC topology has natural protection against fault current but the HV stress on the switch is more

To operate in step-up or step down voltage, buck-boost PFC topology is a good option. BLDCM using DBR offers reduced number of switches but has a disadvantage of larger time constants, low torque and power density and under utilization of motor.

8. Application potential

The cost of BLDCM is reduced by using sensorless control [10]. By using Application Specific Integrated Circuit (ASIC) ML4425 the

commutations pulses are generated on back-emf sensing. Therefore software modification becomes easier than hardware modifications.

9. Conclusions

The PQ improvement in BLDCM using various PFC converter topologies are simulated, analysed and validated by hardware implementations by the experts working in this field.

Buck PFC is preferred for low power / voltage applications [11].

The buck-boost PFC topologies (either isolated or non isolated) including cuk, SEPIC and Zeta topologies provide low THD of current and high PF at input mains. Two switch PFC topology is better than single switch for medium range (< 1 KW) vide Table No.8. Four switch topology is suitable for 1-2 KW power whereas PWM-VSC is suitable for high power (2-4KW).

FINAL CONCLUSION:

Though these PFC topologies [12] satisfy the PQ norms, drive performance, the selection of topology also depends on cost, control complexity, efficiency, THD, PF, DC link voltage ripple etc. This detailed analysis on various PFC topologies for BLDCM will be useful both for manufacturers and users.

This proposal also gives an insight about the role of various controllers and converters with respect to BLDC motor. It is a tough task to find a unique solution hence a tradeoff may be arrived between design complexity and cost (due to ever falling prices of power electronic components) also owing to multi input nature of BLDCM in the realm of motion control.

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BIOGRAPHIES

Dr.B. MAHESH KUMAR received the B.Tech., Degree in Electrical & Rlectronics Engineering from Madurai Kamaraj University, M.Tech., in Process Control and Instrumentation from N.I.T – Trichy and Ph.D., from Jadavpur University, India. At Present, he is working as Associate Professor in Electrical and Electronics Engineering, Pondicherry Engineering College, Pondicherry. He has several years of academic. His research interests include artificial intelligent techniques in electrical machines and control.

Mr. R. BABU ASHOK is currently working as Principal in Women's Polytechnic College (Constituent college of PIPMATE – Government of Puducherry) Karaikal. His area of interest includes Converters special machines & Drives and Artificial intelligent. He is currently doing his Ph.D at Pondicherry Engineering College, Pondicherry. He has several years of academic experience.