BIST Based Test Applications Enhanced with Adaptive Low Power RTPG and LFSR Reseeding Techniques

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***Abstract*— Power, area and time are the major milestones for VLSI circuits. Power consumed during the scan based test mode of a circuit is much more than that in the normal mode because of increased switching transitions. This work is aimed to reduce the power consumed during testing a circuit without affecting the test coverage, speed and memory requirements. The work can be applied to Built In Self Test (BIST) based test applications. To achieve all these objectives, a Low Power Random Test Pattern Generator (LPRTPG) along with partial LFSR reseeding is added to conventional BIST unit. The experimental results on ISCAS'89 benchmark circuit shows efficiency of the work in terms of reduction in test power and memory requirements.**

Keywords*— *VLSI Testing, built-in self test, low power, test patterns, Transition controller, LFSR Reseeding, Encoding techniques.

1. INTRODUCTION

A Design For Testability (DFT) methodology in which the testing logic to detect faulty chips is built inside the chip itself is called Built In Self Test (BIST).

As the size and complexity of System On Chips (SOCs) continues to grow, testing them is becoming a difficult problem with increased power consumption and reduced test coverage. With the increasing scale of integration, test patterns required to test a chip is also increasing. It results in more number of transitions from 0 to 1 and vice versa. So Power dissipation during scan-based tests is higher than the normal operation of the circuit due to this increased switching activity.

BIST unit comprises of a Linear Feedback Shift Register (LFSR), phase shifter, scan cells from circuit under test (CUT) and a Multiple Input Signature Register (MISR).

Wide varieties of techniques are there to reduce the test mode power consumption in BIST. Many of them insert an extra hardware to reduce switching between scan cells which in turn reduces speed [4]. A technique called selective triggering scan architecture [5] reduces switching activity by utilizing an extra scan chain. Another method uses two LFSRs with different speeds [6] to make outputs of all scan cells constant during test mode. Many techniques such as transition monitoring unit [7], DS LFSR [8] etc., are also used to reduce the test power. All these methods are lacking one or two of our three objectives viz. speed, coverage and memory requirements.

Few techniques concentrate on LFSR which is used to generate random test patterns to be applied to the scan cells. The initial input given to LFSR is termed as its seed value. Reseeding LFSRs frequently will increase compression but does not have any impact on test power [9]. In our work partial LFSR reseeding with encoding algorithm [2] is used in conjunction with adaptive low power random test pattern generator (RTPG) [1] to reduce the test power Power, increase the test data compression and fault coverage and to enhance the test speed.

The rest of the paper is organized as follows; Conventional BIST is explained in section II. Proposed scheme is explained in section III, Partial LFSR Reseeding and Encoding techniques are explained in section IV, Simulation results using ISCAS 89 benchmark circuits are explained in section VI.

II.CONVENTIONAL BIST

The basic architecture of BIST is shown in Figure.1

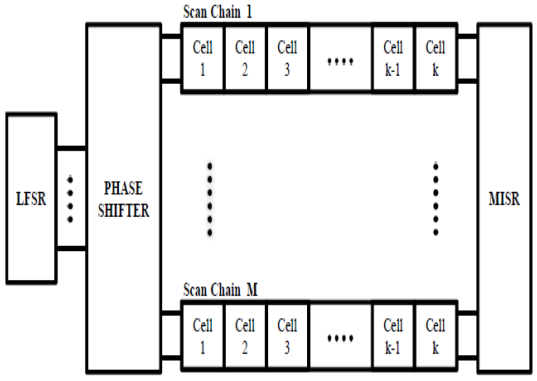

Figure 1. Conventional BIST architecture

It is a combination of flip flops and an XOR gate. When initialized with a seed value, LFSR performs shift and XOR operations to generate different test patterns. Phase shifter is used to deliver the test vectors to the scan cells correctly. LFSR and phase shifter are the basic building blocks of RTPG. Scan cells are the flip flops from CUT. MISR compares the actual test response with precomputed response and indicate the faults if any.

The test vectors generated are directly passed into the scan chain in normal RTPG. This increases the switching activity which results in large power dissipation. In our work a transition controller is inserted to reduce this switching activity. LFSR reseeding and encoding are used to achieve the remaining objectives.

III.PROPOSED SCHEME

The proposed scheme enhances the conventional BIST with three features namely transition controller, partial LFSR reseeding and an encoding algorithm. Proposed architecture is shown in Figure.2.

Transition controller unit comprises of a multiplexer, XNOR gate and a D flip-flop. The values of last two scan cells are given as inputs to the XNOR gate. XNOR output is connected to multiplexer select input. For simplicity let us assume that the two scan cells have same values. XNOR output is 1 which enables the multiplexer and D flip flop will be updated by the phase shifter output. If the scan cells have different values, XNOR output will be zero and D flip flop holds the previous value. During scan mode, values of scan cells are given as feedback to the transition controller which reduces the switching activity by increasing the correlation between adjacent test vectors.

Table 1 shows the comparison of BIST units with and without transition controller [1] with assumed test pattern as 001010. It is obvious that the number of transitions is reduced from sixty three to thirty three.

Table.1 Comparison of BIST with and without transition controller

Cycle	Scan Chain Value	No Transition Controller		With Transition Controller			
		Scan chain values	*Tr.*	*Scan chain values*	*XN OR*	*FF o/p*	*Tr.*
-	001010	011001	-	011001	0	0	-
1	00101	001100	6	001100	1	1	6
2	0010	100110	9	100110	0	1	9
3	001	010011	11	110011	1	1	6
4	00	101001	13	111001	0	1	4
5	0	010100	14	111100	1	0	2
6	-	001010	10	011110	0	0	6
Total			63		33		

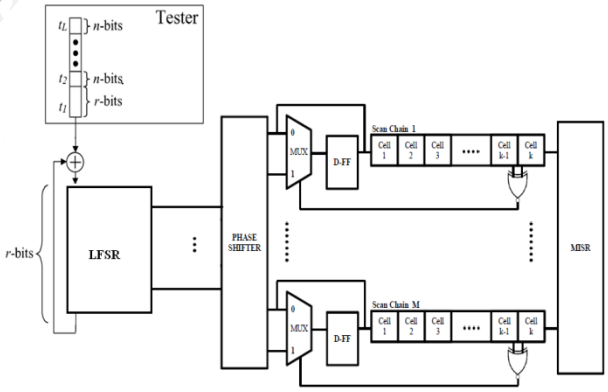

Figure.2 Proposed BIST architecture

IV. PARTIAL LFSR RESEEDING AND ENCODING

Partial LFSR reseeding is done using the tester block in Figure.2. The test patterns produced by LFSR are linearly dependent and deterministic. With an initial seed, we can pre-compute all other test patterns generated by the LFSR. LFSR may be of any size as per our requirements say r bits. An r bit LFSR should be initialized with an r bit seed. This makes the LFSR to run for several clock cycles equal to the scan length.

During next phase, the seed value is reduced to n bits (n<r) so it is a partial reseeding. Fewer bits are needed in addition for next test which can be shifted in from the tester. This allows n (number of bits coming from tester) to be smaller than r (size of the LFSR). After the first n clock cycles, the tester stops shifting in data and the LFSR simply cycles through its normal sequence of states until the scan chains are full.

In our work an encoding scheme [3] is used with partial reseeding. Encoding technique reduces power consumption as well as the number of specified bits. It makes use of the fact that number of specified bits in a test cube is always greater than the number of transitions.

Table.2 Encoding of test data

BLOCK	1	2	3	4
ORIGINAL	1XX0	X000	OXOX	XXX X
ENCODED	**0**1XXO	**1**-----	**1**-----	**X**XX XX

The proposed encoding algorithm divides the test cube into blocks and uses LFSR reseeding to produce only the blocks that contains transitions. LFSR reseeding is not used directly to encode the specified bits as in conventional LFSR.

For the blocks that do not contain transitions, the logic value fed into the scan chain is simply held constant. This approach reduces the number of transitions in the scan chains and in most cases also reduces the total number of specified bits that must be generated by the LFSR as compared with conventional LFSR reseeding.

A. ENCODING METHOD

The proposed encoding scheme encodes each test cube with two kinds of data: "hold flags" and "data bits." Each test cube is divided into several blocks, and each block has a 1-bit hold flag. The hold flag indicates whether a transition occurs in a block. There are three types of blocks.

1. Transition block (hold flag = 0). One or more transitions exist in the block. Either both 0 and 1 are present in the block (e.g, XX1X0X) or only 0 or 1 is present, but the last specified bit from a previous block was the opposite value.
2. Non transition block (hold flag = 1). No transition occurs in the current block. Only 0 or 1 is present in the block, and the last specified bit from a previous block is same (e.g., X0XX0X).
3. Don't care block (hold flag = X). No specified bits occur in the block all are don't cares.

The data bits in a block with hold flag 1 are kept constant from the last data bit in the previous block. Data bits are obtained directly from LFSR if the hold flag is 0. For X hold flag, the block can be treated either as transitional or non transitional. An example is shown in table.2.

Thus, the proposed encoding scheme reduces the number of specified bits that need to be generated using LFSR reseeding. In encoding test data the 1s in blocks 2 and 3 do not need to be generated directly by the LFSR but are rather generated as a by-product of the fact that the hold flags keep the input to the scan chain constant at 1.

Thus, test data compression can be achieved in this way. Moreover, no transitions will occur when generating blocks 2 and 3 because the hold flags are 1, thus keeping all the bits in the blocks constant. This would not be the case in conventional LFSR reseeding, where the Xs in blocks 1 and 2 get filled with random data, which may result in many more transitions. Thus, a reduction in the number of transitions can be achieved in this way.

B. CONVERSION PROCEDURE

It is possible to increase the number of non transition blocks by converting some transitions blocks into non transition blocks. There are two requirements that must be satisfied in order to convert a transition block into a non transition block. The first is that it cannot contain both specified 0s and specified 1s. The second is that the last bit of the previous block must be an X. Two examples of this are shown in table.3.

Table.3 Conversion example

BLOCK	1	2	3	4
ORIGINAL	X01X	X0X0	XXXX	111X
ENCODED	0X010	1-----	0XXX1	1---

Block 2 is initially a transition block even though it only contains specified 0s because the last specified bit in block 1 was a 1. However, the very last bit of block 1 is a don't care, so a "conversion procedure" can be used to specify that don't care as a 0 and thereby convert block 2 into a non transition block. Even though this conversion required adding an extra specified data bit, the net result is still a reduction in the total number of specified bits because now block 2 is a non transition block; thus, none of its data bits need to be generated by the LFSR. This same conversion procedure can also be used to convert block 4 in Figure.3, into a non transition block.

By increasing the number of non transition blocks, the conversion procedure can help to reduce both test storage (since it can reduce the total number of specified bits) and test power (since it can reduce the number of transitions by enabling all the Xs in the converted non transition block to be filled with the same logic value). (The last bit of blocks 1 and 3 are specified to convert blocks 2 and 4 into non transition blocks).

VI.RESULTS AND DISCUSSIONS

The efficiency of the work is analyzed using S27 benchmark circuit of ISCAS'89 family. Modelsim and Xilinx are the tools used for simulation and interpretation. Scan chain is formed with the flip-flops from S27 circuit.

Transition controller and Partial reseeder with encoding algorithm are implemented in conventional BIST.

Simulation results are shown below.

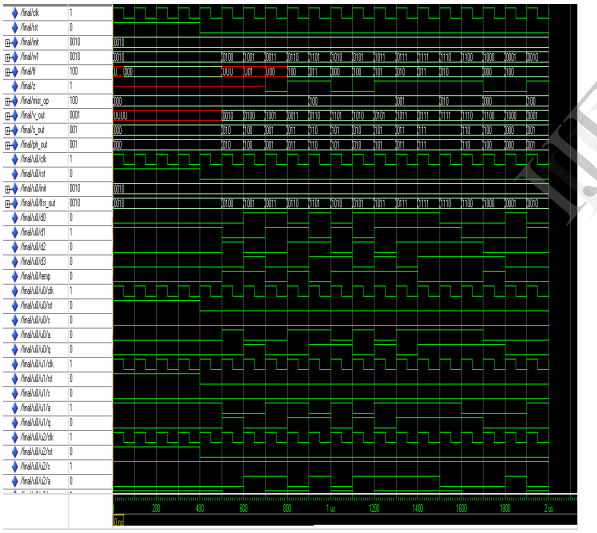

Figure.3 Conventional BIST

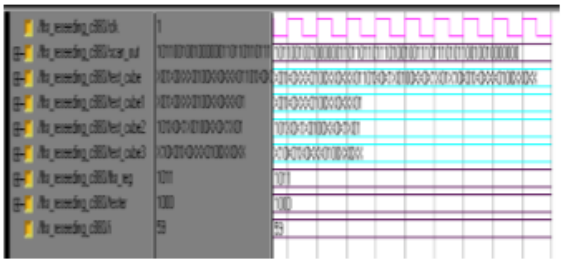

Figure.4 Partial LFSR reseeding

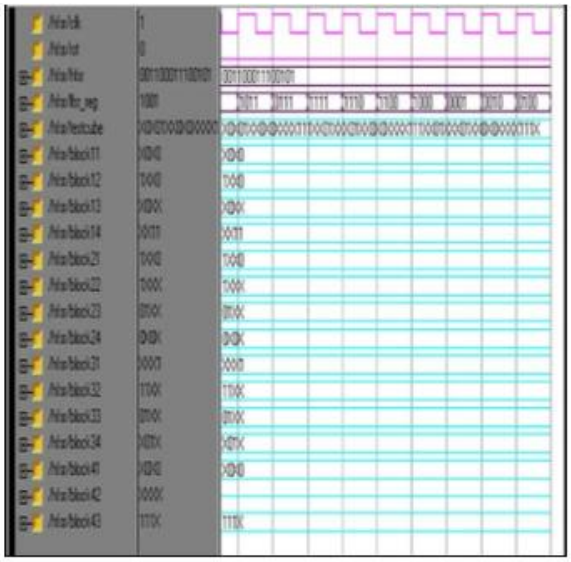

Figure.5 Test cube Encoding

Figure.6 Proposed LFSR Reseeding with Encoding

Simulation analysis of BIST with transition controller and overall result is under progress.

VII.CONCLUSION

BIST with transition controller and partial LFSR reseeding with encoding algorithm is a good solution for test power reduction, test data compression, speed enhancement and test coverage enhancement. The architecture improves the trade-off between test coverage and shift power. Shift power is reduced considerably with a negligible test coverage loss so that the high power dissipation effects in CUT can be reduced. Since the transition controller and

tester cover a negligible portion of chip area, the burden of area overhead can be avoided.

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