Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 5 Issue 05, May-2016

Binary-Weighted DAC using W-2W Current Mirror Topology

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***Abstract* — The paper presents an analysis and design of 3-bit, 4-bit and 6-bit Binary-Weighted CMOS Digital to Analog Converters (DACs). All the DACs are implemented using various CMOS technologies such as 180 nm, 90 nm and 45 nm with the supply of 1.8 V. The INLs, DNLs and Power dissipation of each DAC is compared and analyzed. As the transistor sizing is scaled down, the area occupied by DACs decreases; resulting in lower power dissipation. Even INLs and DNLs are decreased with transistor scaling. Thus, as the technology is scaled down, the design archives a good trade-off between low INL, DNL and Power dissipation.**

***Keywords*— DAC, INL, DNL**

I. INTRODUCTION

Progress of Very Large Scale Integration (VLSI) technology helps to implement many mixed-signal Integrated Circuits (ICs) in a single chip, including data conversion circuits [1-2]. DACs are at the beginning of the analog signal chain, which makes them very important to system performance [6-7].

A. W-2W Current Mirror Topology

The Binary-Weighted DAC is implemented using compact current mirror approach. Fig. 1 shows the binary weighted current mirror implementation using a *W-2W* topology. It utilizes the fact that two identical MOSFETs in parallel (i.e., the effective channel width is twice that of the single MOSFET) and series (i.e., the effective channel width is half that of the single MOSFET) can be combined, as seen in Fig. 2, where device M1and M2 has the same amount of current.

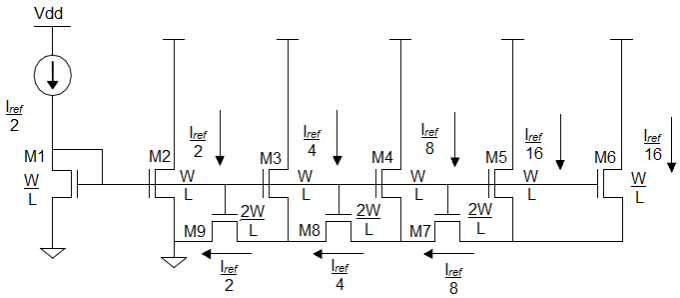

Figure 1. Binary-Weighted current mirror using *W-2W* topology [6].

The currents flowing in the remaining MOSFETs should sum to that of input the value or $I_{ref}/2$. By observing details in Fig. 2, the remaining MOS transistors can be merged into a MOS transistor with size identical to M1 or M2 (drain current is $I_{ref}/2$).

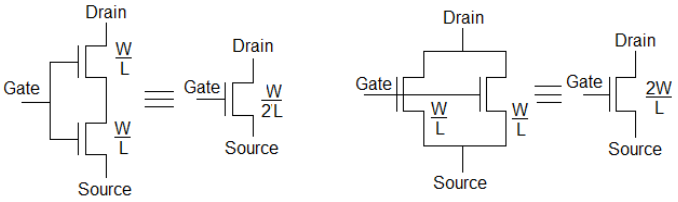

Figure 2. Combining a series and parallel MOSFETs [5].

The merit of the *W-2W* topology significantly reduces the area of the layout for higher bit resolution due to lesser number of MOSFET devices used when compared to normal binary weighted DAC. Assume a MOSFET as a DAC, then an area of the device can be approximated as in equation (1) [5], where η is the layout fill factor with $\eta < 1$.

$$A_i = \frac{1}{\eta}\sum_i W_i L_i \qquad (1)$$

The ratio of N-bit conventional DAC verses *W-2W* binary weighted DAC is given by equation (2), where factor $2N/\alpha$ is switch size and α is always > 1.

$$r = \frac{N(2^N - 1) + 2N/\alpha}{(3N - 1) + 2(N + 1)/\alpha} \qquad (2)$$

Identical size (W/L) MOSFET is utilized in the circuit. It obtains a symmetrical layout reducing the mismatch due to alterations in the process. In *W-2W* topology the devices M1, M2 and M3 operate with continual modifications, from the robust inversion region in the weak inversion region [7]. Fig. 3 shows that as the number of bits increases, then the layout, size ratio (conventional binary-weighted verses *W-2W* DAC) also increases.

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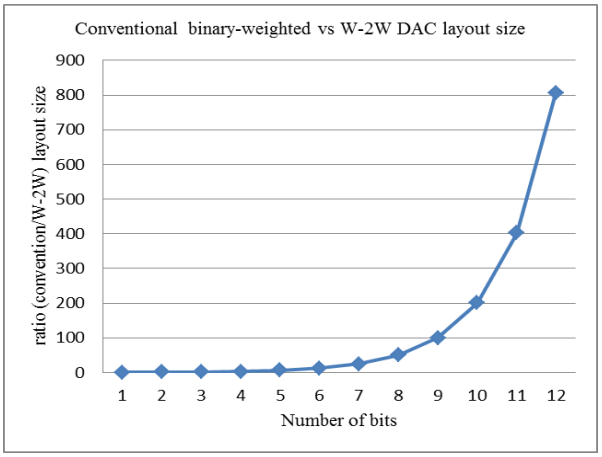

Figure 3. The ratio (r) of the approximated layout size for a traditional binary weighted and the *W-2W* DAC verses the number of bits.

B. INL and DNL

The *W-2W* DACs linearity equations are discussed in equation (3) and (4) [5]. In order to sum the errors as zero, the maximum positive and negative mismatch error is assumed at the current source corresponding to MSB (B_{N-1}) and the bits from B0 through B_{N-2} respectively. For an N-bit DAC equation (4) gives the worst case INL. Where ΔI_K is the mismatch in current source and $|\Delta I_K|_{max,\ INL}$ is the condition to keep the INL lesser than 0.5 LSB. The transition of the input from 0111…11 to 1000..00 gives the largest DNL at the midscale.

$$\left|INL_{max}\right| = \frac{\Delta I_K}{2}, \quad \left|\Delta I_K\right|_{max,\ INL} = \frac{I_{ref}}{2^N} \qquad (3)$$

$$\left|DNL_{max}\right| = \Delta I_K\left(1 - \frac{1}{2^N}\right), \quad \left|\Delta I_K\right|_{max,\ DNL} = \frac{I_{ref}}{2^{N+1} - 2} \qquad (4)$$

II. THE BINARY-WEIGHTED DAC

Fig. 1 shows that the addition of successive stages divides the input current by 2 consecutively, maintaining $I_{ref}/2$ as the overall sum of currents, which flows through device M1 and M2. 3-bit, 6-bit and 12-bit binary-weighted DACs are shown in Fig. 6, Fig. 8 and Fig. 10 respectively, where the current obtained from current mirror are digitally steered at the output node through the MOS transistor switches. The current drop in primary branch is equal to input current ($I_{ref}/2$), which is equivalent to the current DAC's Most Significant Bit (MSB), while the last two branches drops to $I_{ref}/2^N$.

The current sources can be matched better when the two pair of MOS switches is connected to the same inputs B0 and $\overline{B0}$. It has to be noted that the input current is equal to $I_{ref}/2$ as per the condition given in Section I, which is equal to MSB. Equation (3) gives the full scale or maximum output current. It is equal to $2\times I_{ref\ in}$ (or $I_{ref}/2$).

$$I_{FS(max)} = I_{ref} \qquad (5)$$

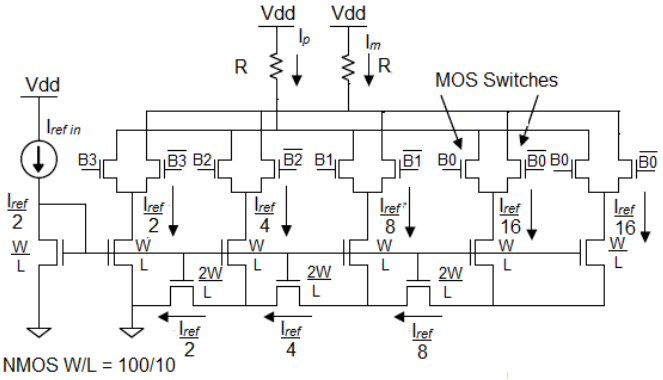

Figure 4. A 4-bit binary weight DAC using *W-2W* current mirror topology.

The inputs B0 –B3 are complemented using the inverter and given to the chip, as shown in Fig. 5.

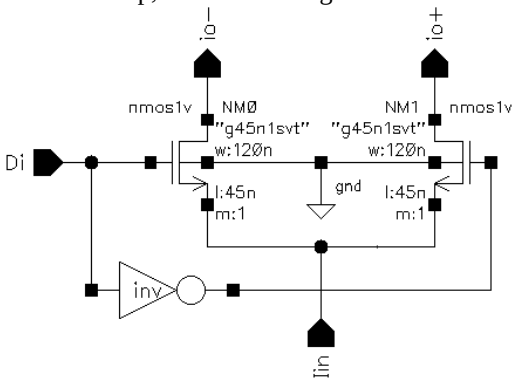

Figure 5. Inverter based scheme to provide differential input.

A. 3-bit DAC

The schematic diagram of 3-bit DAC in 45 nm CMOS technology is shown in Fig. 6. B0-B2 are the digital inputs, where i_{dc} (8 uA, input reference current source) and the differential output nodes Vout+ and Vout- are all off chip. The load capacitance C0 and C1 are used at the output node to reduce the glitches. The Fig. 7 shows the simulation results of 3-bit DAC.

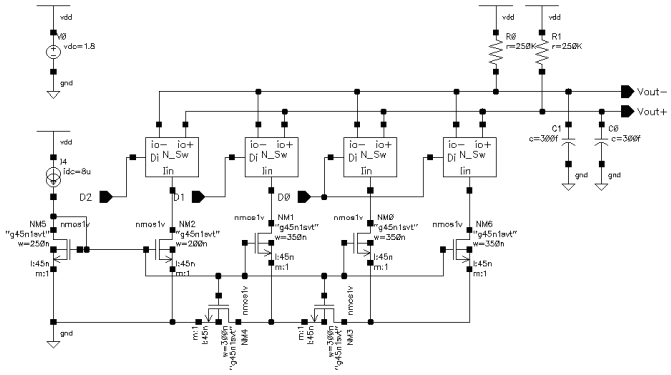

Figure 6. A 3-bit Binary-Weighted DAC.

International Journal of Engineering Research & Technology (IJERT)
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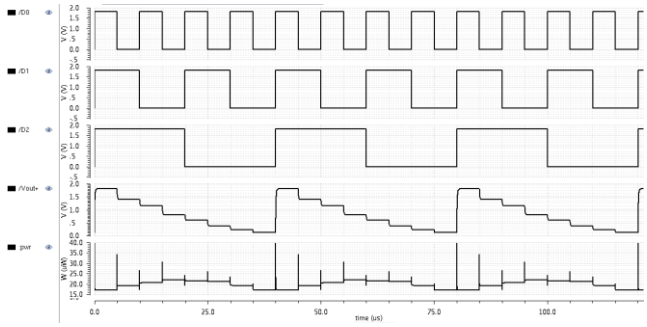

Figure 7. Simulation Results of 3-bit DAC.

Experimental results of 3-bit DAC in 180 nm, 90nm and 45 nm are performed and parameter INL_{max}, DNL_{max} and power dissipation are tabulated in Table I.

TABLE I. 3-BIT DAC PARAMETERS

CMOS Technology	Parameters		
	***INL**max*	***DNL**max*	***Power Dissipation***
180 nm	1.86 LSB	0.65 LSB	30.24 uW
90 nm	1.43 LSB	0.607 LSB	27.28 uW
45 nm	0.99 LSB	0.556 LSB	19.79 uW

B. 4-bit DAC

Fig. 8 and Fig. 9 shows the schematic and simulation results of the 4-bit DAC in 45 nm technology. Where B0-B3 is digital inputs and i_{dc} (16 uA) is the reference current source. The linearity errors increase due to increasing resolution, even power dissipation also increases. Linearity errors and power dissipation of 4-bit DAC in different CMOS technology has been performed and tabulated in Table II.

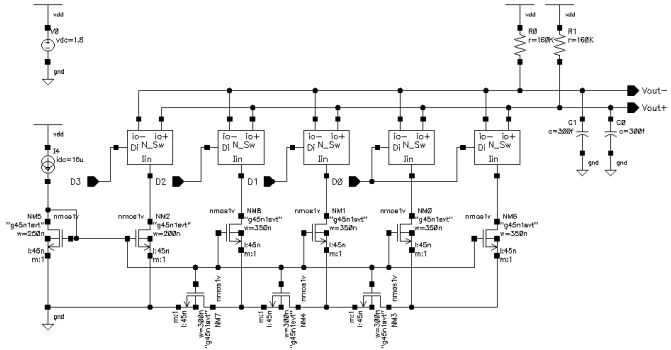

Figure 8. A 4-bit Binary-Weighted DAC.

The parameters INL_{max}, DNL_{max} and power dissipation slightly increase compared to 3-bit DAC.

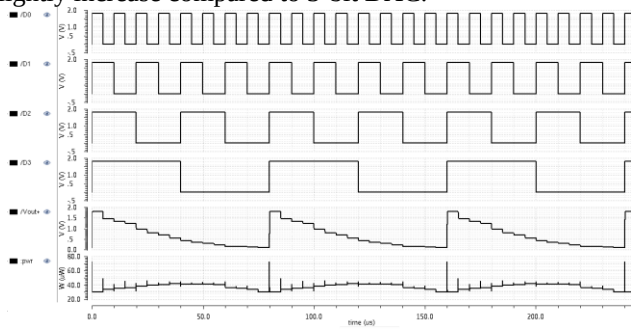

Figure 9. Simulation Results of 4-bit DAC.

TABLE II. 4-BIT DAC PARAMETERS

CMOS Technology	Parameters		
	***INL**max*	***DNL**max*	***Power Dissipation***
180 nm	2.0 LSB	1.216 LSB	54.72 uW
90 nm	1.2 LSB	1.180 LSB	53.77 uW
45 nm	1.0 LSB	0.983 LSB	37.22 uW

C. 6-bit DAC

Fig. 10 shows the schematic of 6-bit DAC in 45 nm CMOS technology and Fig. 11 shows simulation results. Where B0-B5 are digital inputs and i_{dc} (64 uA) is the reference current source. Parameter INL_{max}, DNL_{max} and power dissipation are tabulated in Table III. The parameters INL_{max}, DNL_{max} and power dissipation slighty increase compared to 3-bit and 4-bit DAC.

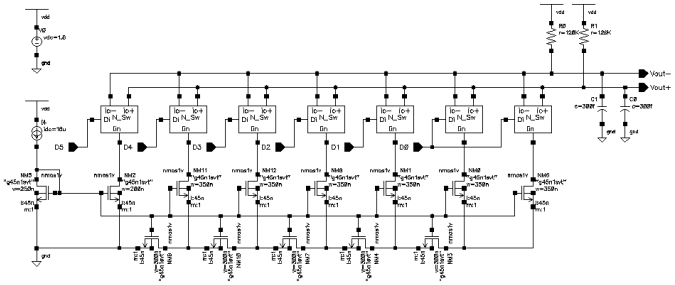

Figure 10. A 6-bit Binary-Weighted DAC.

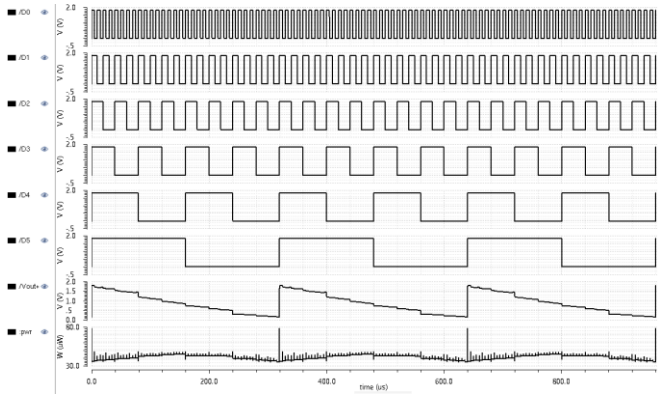

Figure 11. Simulation Results of 6-bit DAC.

TABLE III. 6-BIT DAC PARAMETERS

Technology	Parameters		
	***INL**max*	***DNL**max*	***Power Dissipation***
180 nm	4.658 LSB	3.10 LSB	223.8 uW
90 nm	4.541 LSB	3.071 LSB	215.2 uW
45 nm	4.203 LSB	2.932 LSB	40.76 uW

III. RESULTS AND DISCUSSION

The parameter INL_{max}, DNL_{max} and power dissipation increase with increasing resolution and decreases as technology is scaled down from 180 nm, 90 nm to 45 nm. Each parameter is plotted with respect to different CMOS technology as shown in Fig. 12, Fig. 13 and Fig. 14 respectively.

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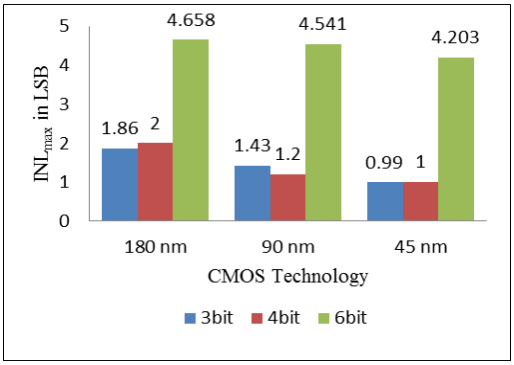

Figure 12. Resolution versus INL_{max} for various CMOS technology.

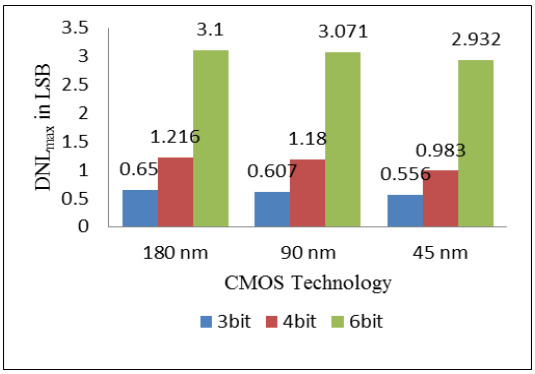

Figure 13. Resolution versus DNL_{max} for various CMOS technology.

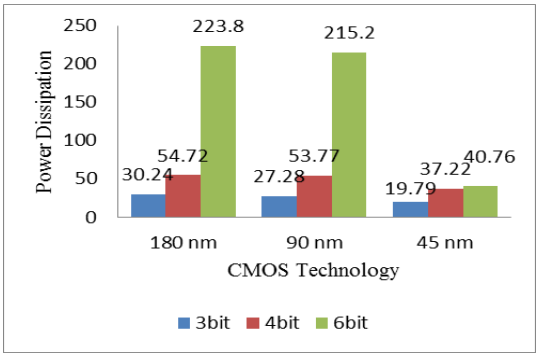

Figure 14. Power dissipation versus resolution for various CMOS technologies.

IV. CONCLUSION

3-bit, 4-bit and 6-bit *W*-2*W* DAC topologies were discussed and test results presented using various CMOS technologies such as 180nm, 90 nm and 45 nm with the supply of 1.8V. The corresponding maximum DAC INLs and DNLs are discussed and power dissipation of each DAC is compared and analyzed. As the CMOS technology is scaled down, the area occupied by DACs decreases; resulting in lower power dissipation. Even INLs and DNLs are decreased with transistor scaling.

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