# Balancing The Capacitor Voltage In NPC - APF Using Pulse Width Modulation Control

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*Abstract* — **The Neutral Point Clamped (NPC) voltage source inverter (VSI), without a separately supporting dc link is used to maintain the two dc-link capacitor voltages in a balanced condition. In this paper, balancing of the capacitor voltages for these two capacitor voltage source possibilities are determined and pulse width modulation technique is proposed to independently balance the capacitor voltages. This technique considers the average energy effect of each capacitor voltages. The technique minimizes the voltage rating overheads of the hardware, reduces the voltage ripple and attenuates the negative effects associated with dc-link voltage oscillations. It increases the power handling capability and reduces voltage and current harmonics. The proposed scheme was simulated by using MATLAB Simulink.**

*Index Terms* — **DC-link voltage ripple, Neutral Point diode Clamped (NPC), Pulse Width Modulation (PWM).**

## I. INTRODUCTION

The Neutral Point Diode Clamped (NPC) voltage source inverter (VSI) is a common structure in medium and high power industrial applications. It avoids the complexity associated with the series connection of semiconductor switches. It causes a low voltage stress on semiconductor switches thus increasing the power handling capability and produces lower current / voltage harmonics.

One three-level NPC inverter is used to balance the voltages of the two series connected capacitors across the dc link. The three-level NPC VSI structure without an external dc supply is shown in Fig. 1. This voltage oscillation causes adverse effects, such as low frequency harmonics in the output line-to-line voltages, the bridge devices and capacitors must withstand higher varying voltage stresses. Methods to eliminate the voltage ripple have been proposed both with Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Modulation (SVM). When the three level NPC VSI is used as an Active Power Filter (APF) to improve the power quality at the point of common coupling, as shown in Fig. 1, the dc-link capacitors are independent. A correctly controlled APF can reduce harmonics, compensate reactive power, and balance the ac source currents.

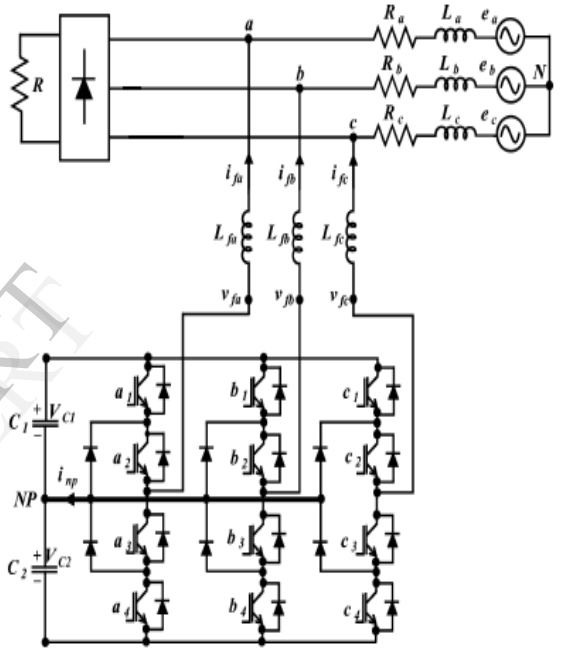



Fig. 1. Three-level NPC active power filter.

Control of the independent dc-link capacitors in multilevel APF inverters has been extensively researched and capacitor sizing due to the transient load changes has also been considered. Capacitor voltage balance is almost achieved, but with voltage ripple. This accentuates the imbalance and becomes more serious when the instantaneous power difference between the supply and the load is more significant.

## II. PULSE WIDTH MODULATION

PWM inverters are gradually taking over other types of inverters in industrial applications. PWM techniques are characterised by constant amplitude pulses. The width of these pulses is, however, modulated to obtain inverter output voltage control and to reduce its harmonic content. The different PWM techniques are

- Single – Pulse Modulation
- Multiple – Pulse Modulation
- Sinusoidal – Pulse Modulation

In PWM inverters, forced commutation is essential. The three PWM techniques listed above differ from each other in the harmonic content in their respective output voltages. Thus, choice of particular PWM technique depends upon the permissible harmonic content in the inverter output voltage.

In industrial applications, PWM inverter is supplied from a diode bridge rectifier and an LC filter. The inverter topology remains the same for single–phase inverter and three–phase inverter. But now the devices are switched on and off several times within each half cycle to control the output voltage which has low harmonic content.

The advantages of PWM control are

- The output voltage content can be obtained without any additional component.
- With this type of control, lower order harmonics can be eliminated or minimized along with its output voltage control.
- The filtering requirements are minimized as higher order harmonics can be filtered easily.

The main drawback of this method is that the SCRs used in this method must have very low turn-on and turn-off times (inverter-grade SCRs), therefore they are very expensive.

## III. PROPOSED SINUSOIDAL PULSE WIDTH MODULATION

In this method of modulation, several pulses per half cycle are used in the case of multiple-pulse modulation (MPM). In MPM, the pulse width is equal for all the pulses. But in sin M, the pulse width is a sinusoidal function of the angular position of the pulse in a cycle. For realizing sin M, a high-frequency triangular carrier wave $A_c$ is compared with a sinusoidal reference wave $A_m$ of the desired frequency. The intersection of $A_c$ and $A_m$ waves determines the switching instants and commutation of the modulated pulse. Here, $A_c$ is the peak value of triangular wave and $A_m$ that of reference, or modulating, signal.

The carrier and reference waves are mixed in a comparator in order to produce the PWM triggering pulses as shown in Fig. 2.

When sinusoidal wave has magnitude higher than the triangular wave, the comparator output is high, otherwise it is low and it is shown in Fig. 3. The comparator output is processed in a trigger pulse generator in such a manner that the output

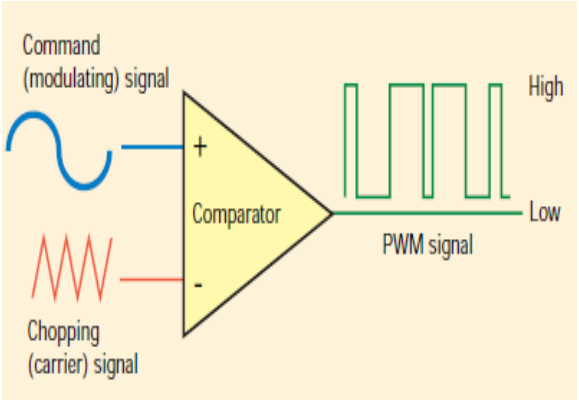



Fig. 2. Generation of PWM pulses.

voltage wave of the inverter has a pulse width in agreement with the comparator output pulse width.

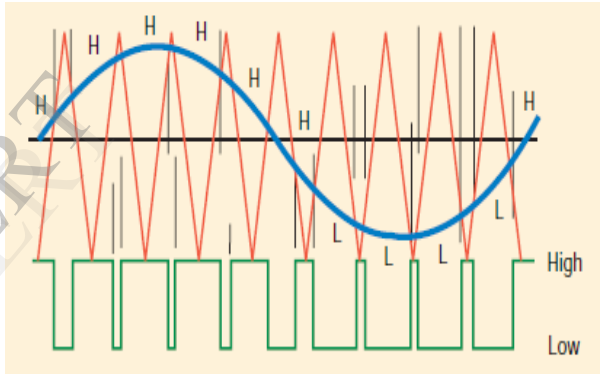



Fig. 3. Low and High comparator output.

When triangular carrier wave has its peak coincident with zero of the reference sinusoid, there are $N = \frac{f_c}{2f}$ pulses per half cycle. In case zero of the triangular wave coincides with zero of the reference sinusoid, there are (N – 1) pulses per half cycle.

The ratio of $A_m / A_c$ is called the modulation index (MI) and it controls the harmonic content of the output voltage waveform. The magnitude of the fundamental component of output voltage is proportional to MI, but MI can never be more than unity. Thus the output voltage is controlled by varying MI.

If $P_m$ is the width of the $m$th pulse, the rms value of output voltage is obtained by the equation $E_L = E_{dc}\left(\sum_{m=1}^{N_p} \frac{P_m}{\pi}\right)^{1/2}$. Harmonic analysis of the output modulated voltage wave reveals that sin M has the following important features:

- For MI less than one, largest harmonic amplitudes in the output voltage are associated with harmonics of order $f_c/f \pm 1$ or $2N \pm 1$, where N is the number of pulses per half cycle. Thus, by
- increasing the number of pulses per half cycle, the order of dominant harmonic frequency can be raised, which can then be filtered out easily. If N=5, therefore harmonics of order 9 and 11 become significant in the output voltage. It may be noted that the highest order of significant harmonic of a modulated voltage wave is centered on the carrier frequency $f_c$.

It is absorbed from above that as N is increased; the order of significant harmonic increases and the filtering requirements are accordingly minimized. But higher value of N entails higher switching frequency of thyristors. Thus a compromise between the filtering requirements and inverter efficiency should be made.

- For MI greater than one, lower order harmonics appear, since for $MI > 1$, pulse width is no longer a sinusoidal function of the angular position of the pulse.

The switches in the voltage source inverter can be turned on and off as required. In the simplest approach, the top switch is turned on if turned on and off only once in each cycle, a square wave waveform results. However, if turned on several times in a cycle an improved harmonic profile may be achieved.

In the most straightforward implementation, generation of the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave as depicted schematically in Fig. 4. Depending on whether the signal voltage is larger or smaller than the carrier waveform, either the positive or negative dc bus voltage is applied at the output. Note that over the period of one triangle wave, the average voltage applied to the load is proportional to the amplitude of the signal (assumed constant) during this period.

The resulting chopped square waveform contains a replica of the desired waveform in its low frequency components, with the higher frequency components being at frequencies of a close to the carrier frequency. Notice that the root mean square value of the ac voltage waveform is still equal to the dc bus voltage, and hence the total harmonic distortion is not affected by the PWM process. The harmonic components are merely shifted into the higher frequency range and are automatically filtered due to inductances in the ac system.

When the modulating signal is a sinusoid of amplitude Am, and the amplitude of the triangular carrier is Ac, the ratio m=Am/Ac is known as the modulation index. Note that controlling the modulation index therefore controls the amplitude of the applied output voltage.

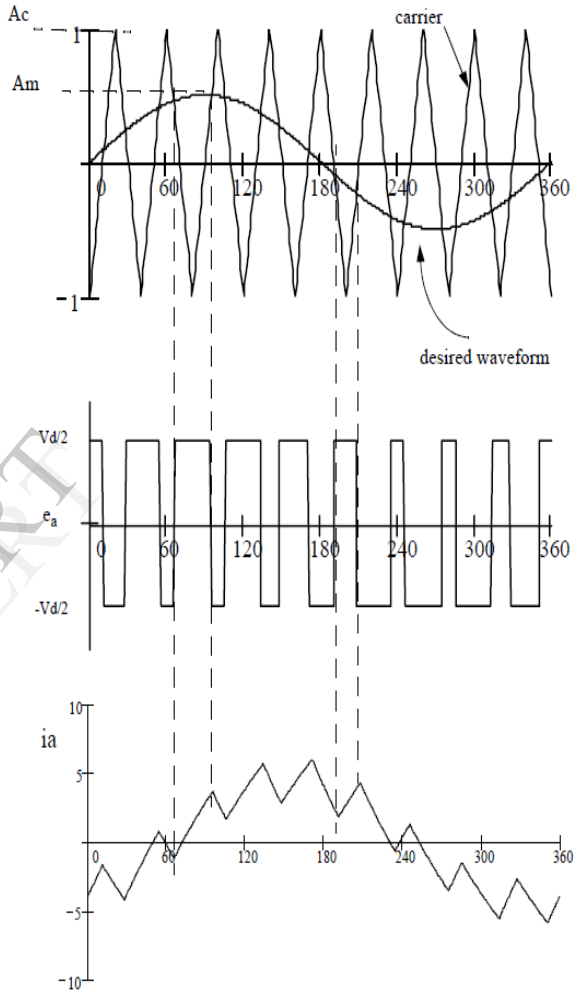



Fig. 4. Principle of SPWM

With a sufficiently high carrier frequency (see Fig. 5 drawn for fc/fm = 21 and t = L/R = T/3; T = period of fundamental), the high frequency components do not propagate significantly in the ac network (or load) due the presence of the inductive elements. However, a higher carrier frequency does result in a larger number of switching's per cycle and hence in an increased power loss.

Typically switching frequencies in the 2-15 kHz range are considered adequate for power systems applications. Also in three-phase systems it is

advisable to use $\frac{f_c}{f_m} = 3k, (K \epsilon N)$ so that all three waveforms are symmetric.

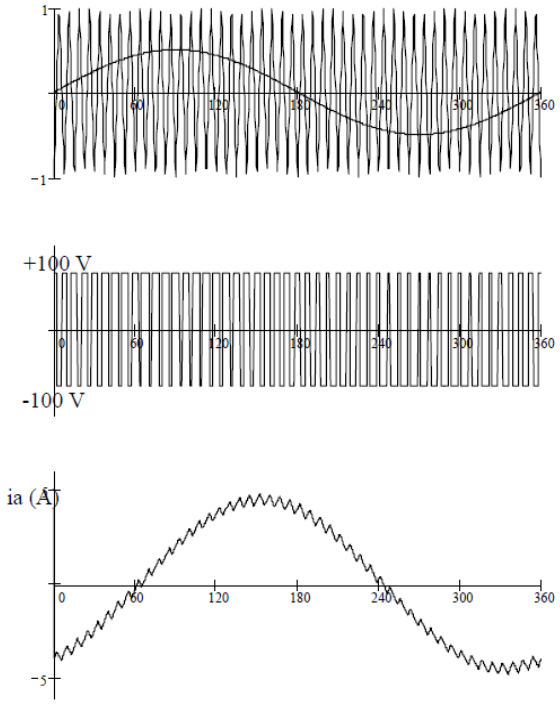



Fig. 5. SPWM with $f_c/f_m = 48, L/R = T/3$

Note that the process works well for $m \leq 1$. For $m > 1$, there are periods of the triangle wave in which there is no intersection of the carrier and the signal as in Fig. 6. However, a certain amount of this "over modulation" is often allowed in the interest of obtaining a larger ac voltage magnitude even though the spectral content of the voltage is rendered somewhat poorer. Note that with an odd ratio for $f_c/f_m$, the waveform is anti-symmetric over a 360 degree cycle. With an even number, there are harmonics of even order, but in particular also a small dc component. Hence an even number is not recommended for single phase inverters, particularly for small ratios of $f_c/f_m$.

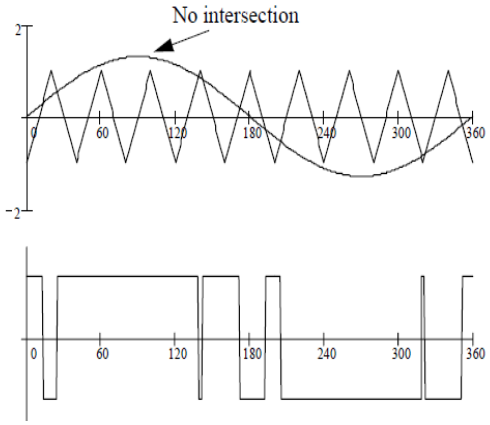



Fig. 6. Over modulation m=1.3

**SPWM Spectra:**

Although the SPWM waveform has harmonics of several orders in the phase voltage waveform, the dominant ones other than the fundamental are of order n and n±2 where $n = f_c/f_m$. This is evident for the spectrum for n=15 and m = 0.8 shown in Fig. 7. Note that if the other two phases are identically generated but 120° apart in phase, the line-line voltage will not have any triplen harmonics. Hence it is advisable to choose $\frac{f_c}{f_m} = 3k, (K \epsilon N)$, as then the dominant harmonic will be eliminated.

It is evident from Fig 7. b), that the dominant 15th harmonic in Fig. 7.a) is effectively eliminated in the line voltage. Choosing a multiple of 3 is also convenient as then the same triangular waveform can be used as the carrier in all three phases, leading to some simplification in hardware.

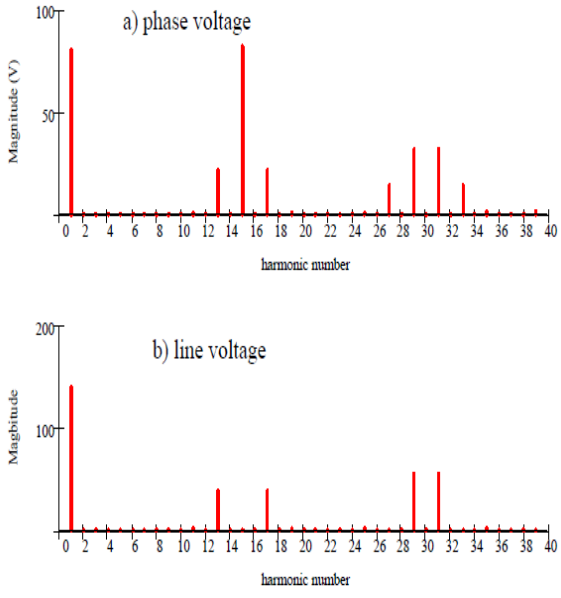



Fig. 7. SPWM Harmonic Spectra: n=15, m=0.8

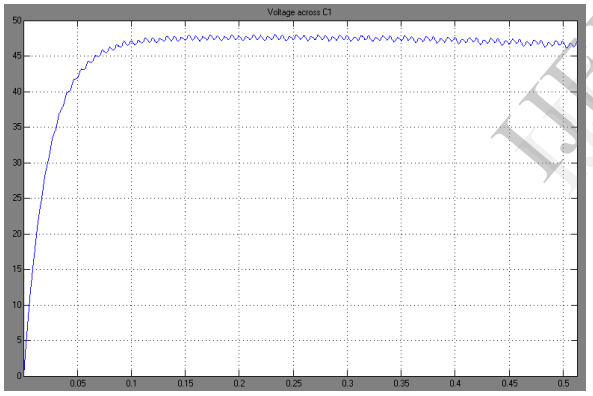
It is readily seen that as the $(pwm(\theta))^2 = E^2$ where E is the dc bus voltage, that the rms value of the output voltage signal is unaffected by the PWM process. This is strictly true for the phase voltage as triplen harmonic orders are cancelled in the line voltage. However, the problematic harmonics are shifted to higher orders, thereby making filtering much easier. Often, the filtering is carried out via the natural high-impedance characteristic of the load.

## IV. SIMULATION RESULTS

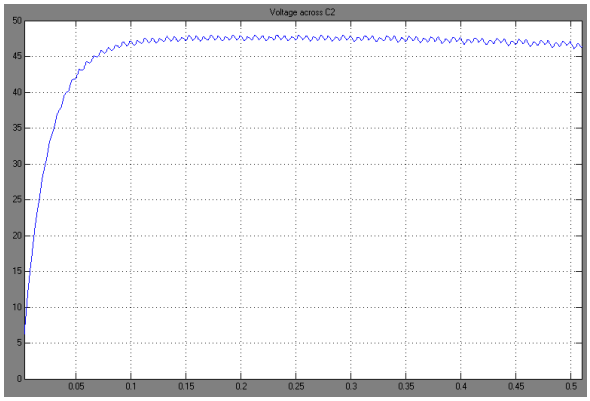
Two scenarios are implemented with balanced source side impedances. The balanced three phase rectified bridge with resistive load is shown in Fig. 1. The other adds a single phase rectified load to the balanced three phase rectified load in order to make an unbalanced non-linear load.

### A. *Capacitor Voltage under Balanced Load*

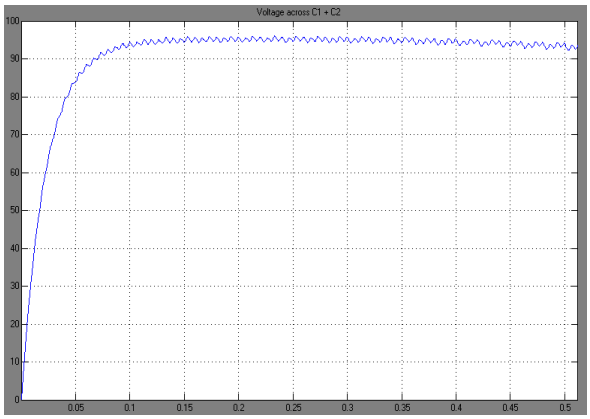
The simulation result of capacitor voltages in APF under balanced three phase rectified bridge with resistive load are shown in Fig. 8.



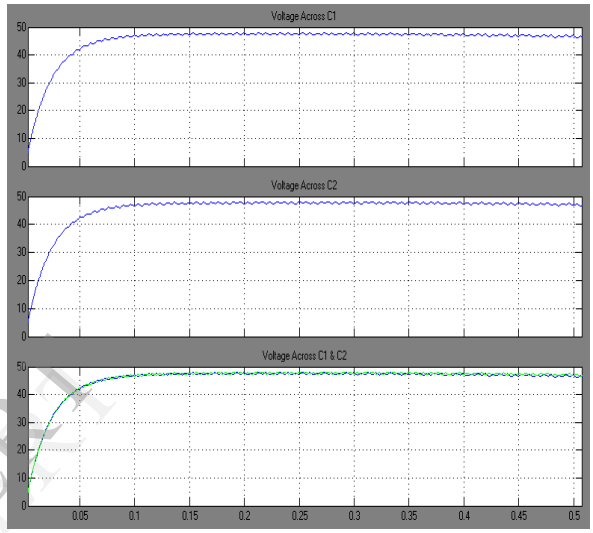

(a) Voltage across C1




(b) Voltage across C2




(c) Voltage across C1 + C2

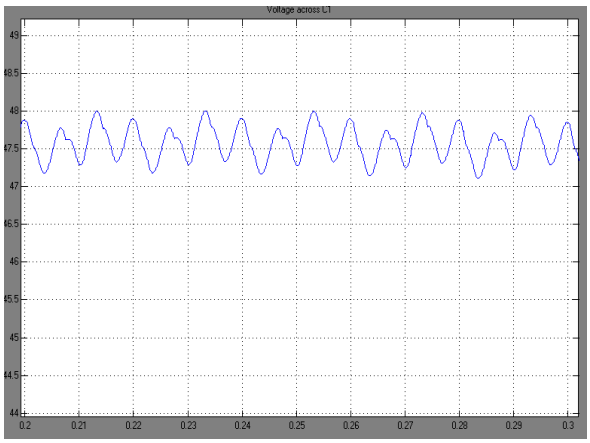



(d) Voltage across C1, C2 and C1+C2

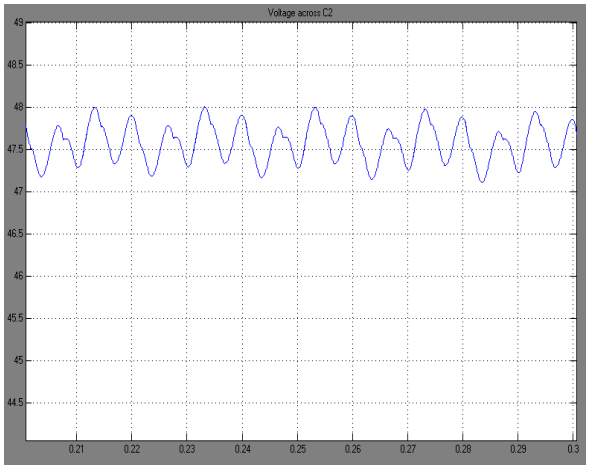
Fig. 8. Capacitor voltages under balanced load

### B. *Capacitor Voltage Spikes under Balanced Load*

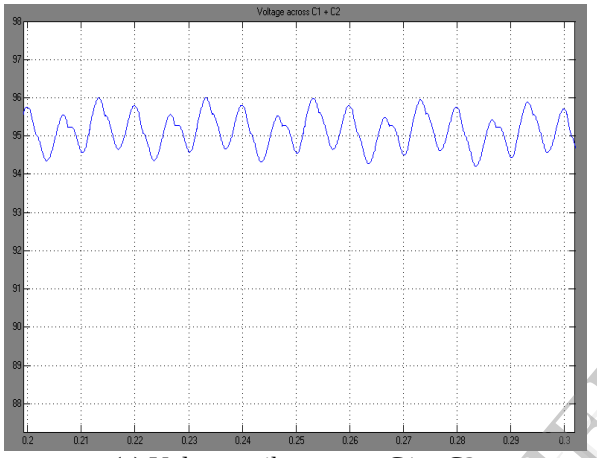
The capacitor voltage spikes in an APF under balanced three phase rectified bridge with resistive load are shown in Fig. 9.



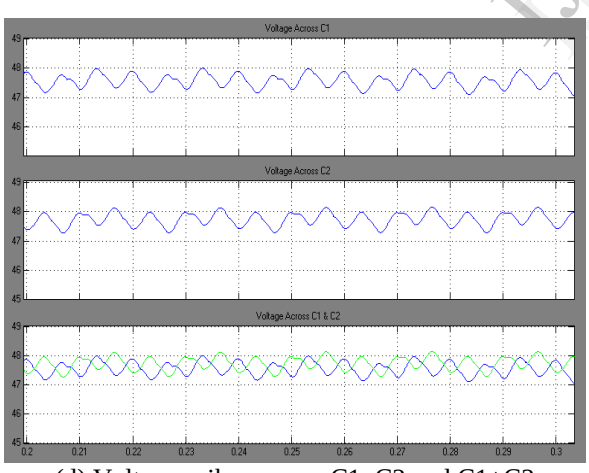

(a) Voltage spikes across C1




(b) Voltage spikes across C2




(c) Voltage spikes across C1 + C2




(d) Voltage spikes across C1, C2 and C1+C2

Fig. 9. Capacitor voltage spikes under balanced load

C. *THD value for Balanced Load*

The THD value of line current for both balanced load without APF and balanced load with APF is shown in Fig. 10 and Fig. 11.

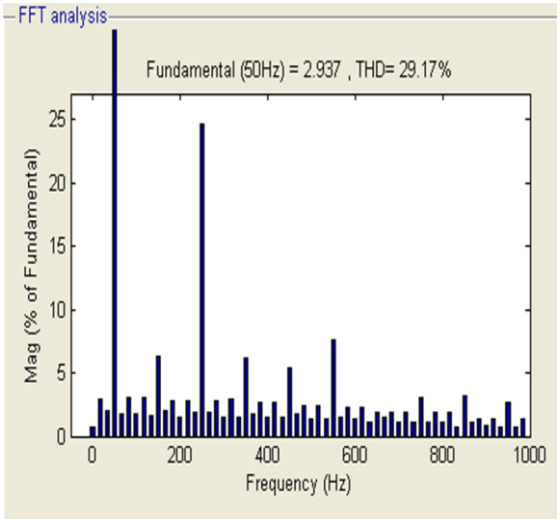



Fig. 10. THD value for balanced load without APF

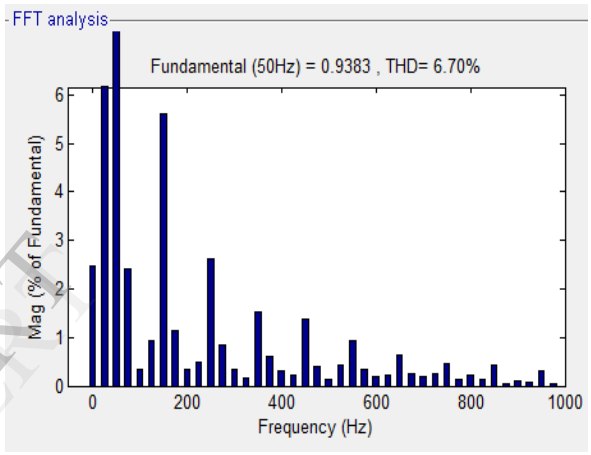



Fig. 11. THD value for balanced load with APF

D. *Evaluation of the Proposed Method*

The accuracy of the proposed technique is a switching frequency ($f_s$) dependent. The technique is evaluated only by APF current direction and capacitor voltage difference is considered (similar to symmetric modulation in [3] but when applied to APF). The relation between the maximum capacitor voltage difference under unbalanced load conditions and switching frequency is shown in Fig. 12.

As the switching frequency increases, the current values sampled at the beginning of each switching cycle better approximate the average current in the switching period. The capacitor balancing accuracy of this algorithm remains acceptable at a 2.5-kHz switching frequency.

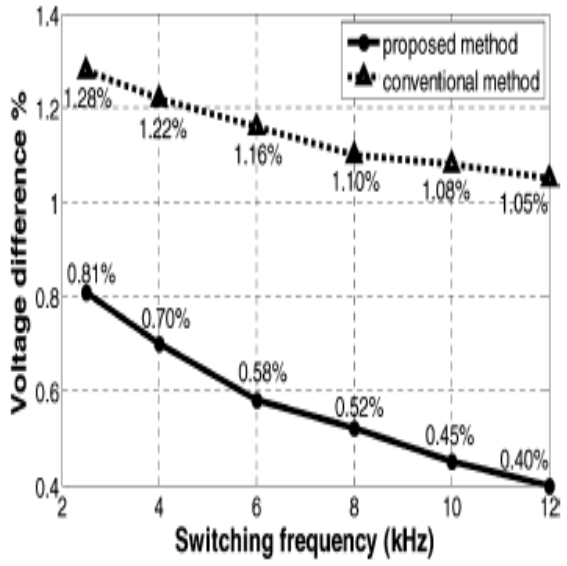



Fig. 12. Evaluation of the proposed method.

## V. CONCLUSION

The new technique is to balance the capacitor voltages of the three level NPC - APF. The technique considers the average energy effect of each capacitor in each modulation cycle, thus giving the balanced results. The proposed scheme maintains almost constant capacitor voltage. It is to be noted that the voltage across the capacitors has been well balanced and the value of THD was found to be 6.70%. The proposed technique reduces hardware ratings, reduces capacitor voltage ripple, and attenuates the negative effects associated with voltage oscillations. This technique can also applicable for unbalanced three phase rectified bridge with resistive load.

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