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Asymmetrical Multilevel Inverter with Low THD

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***Abstract*—Multilevel inverter is a new family of converters for DC-AC conversion for medium and high voltage and power applications. In this paper a new topology has been proposed with lesser number of switches for the generation of nearly sinusoidal output voltage [1]. This is an asymmetrical 15 level multilevel inverter topology with less number of switches. The THD of the output across the load is less which promotes to better activity of the inverter and as a result overall efficiency of the system increases. The output results and FFT analysis of asymmetrical 15 level multilevel inverter topology are ascertained by utilizing MATLAB/SIMULINK software.**

Index terms— MLI, Asymmetrical, Pulse width modulation technique, Switching scheme, Total Harmonic Distortion.

I INTRODUCTION

As of late the propensity to produce power from renewable energy sources is expanding. Simultaneously the power rating of photograph voltaic power plants, wind turbines and renewable equipment expanded quickly.

A circuit which changes over DC power into AC power at wanted output voltage and frequency is an Inverter. The AC output voltage could be fixed at fixed or variable frequency. The controlled turn on and turn-off or by constrained commutated thyristors relying upon the applications could achieve this change. thyristors should be utilized for high power output. For low and medium voltage applications Square wave or Quasi square wave voltages might be adequate and for high force applications low distorted sinusoidal wave structures are required. For this low distorted sinusoidal wave structures staggered inverters are utilized, as they produce almost sinusoidal waveform which has low THD and low dv/dt proportion which will be more in a conventional inverter [4] . Because of the popularity for medium power converters and high-power converters staggered inverters are a convenient and intriguing test with regards to the field of intensity hardware [3]. The zones of enthusiasm for the present analysts are the new staggered topologies that can give lower THD and high productivity, particularly at high force levels. New thoughts and research have been given and inquired about by specialists.

The progression in the field of intensity electronic has improved the use of high-power medium voltage drive applications in the mechanical field. The dv/dt and the harmonics should be limited by the presentation of more levels in the yield voltage so as to show signs of improvement execution of medium voltage and high-power electric drive [6]. The output voltage produced from the multilevel inverter is at high frequency and low switching frequency with low distortions.

II PROPOSED TOPOLOGY

The proposed topology is modeled so as to acquire lesser THD with reduced number of switches for fifteen level multilevel inverter. This topology requires three dc voltage sources and thirteen switches to synthesis 15 levels across the load. This is an asymmetrical 15 level MLI topology using sinusoidal pulse width modulation technique. In this asymmetrical MLI, the dc source magnitudes are unequal and it is designed by binary form of voltage such as V_{dc},$2V_{dc}$ and $4V_{dc}$.The THD of the output waveform decreases as the number of levels increases. The overall efficiency of the system increases as the THD of output across load diminishes. This prompts the better activity of inverter. In this topology the THD of the system is very much reduced.

The configuration of proposed topology is shown in fig.1

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III CIRCUIT DIAGRAM

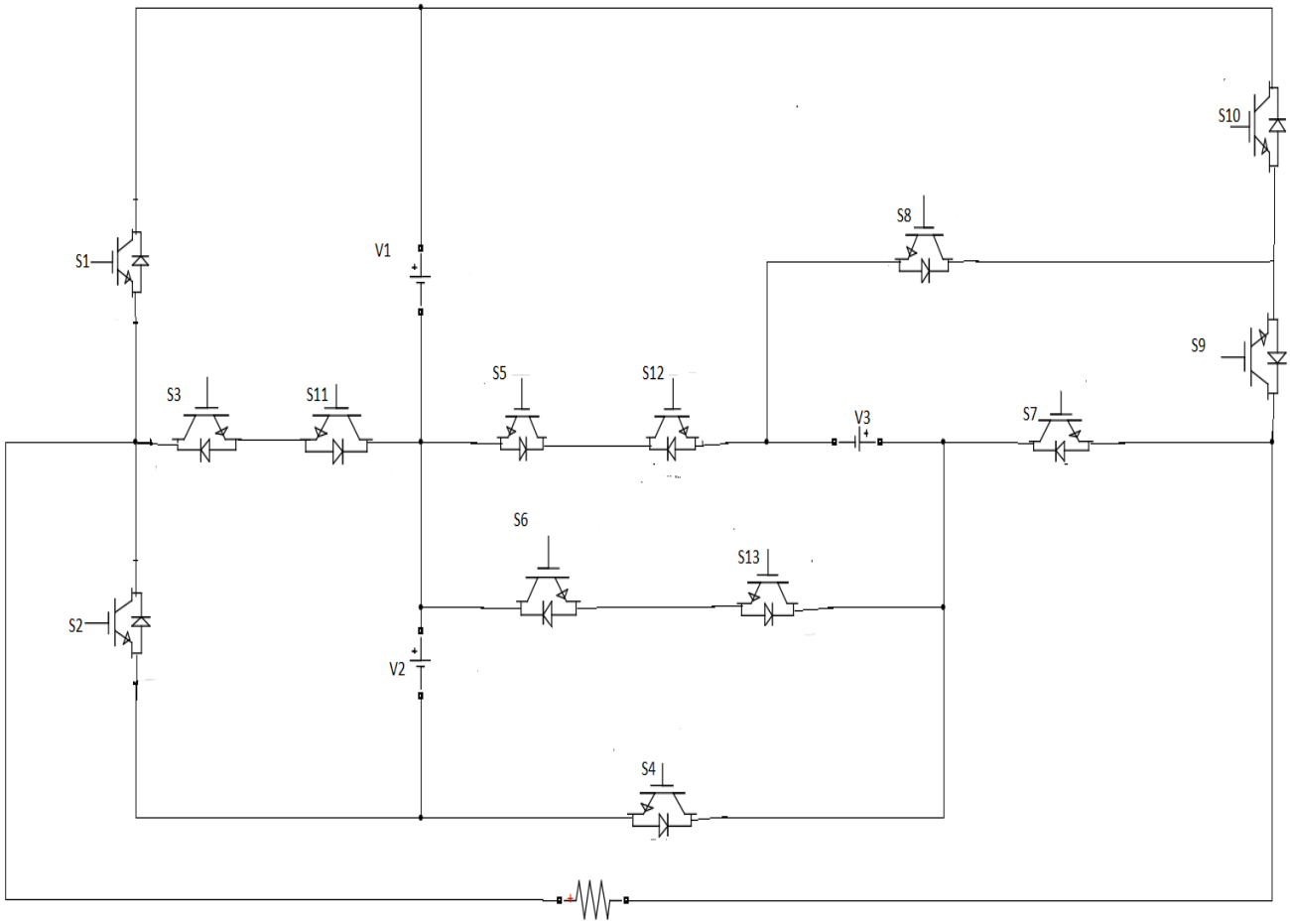

Fig.1 Circuit diagram for the proposed topology

IV SWITCHING SCHEME

Pulse width modulation (PWM) is a modulation technique utilized in most communication system for ciphering the amplitude of the signal right width or duration of another signal usually a carrier signal.

A Multilevel inverter control scheme can be classified according to switching frequencies as fundamental switching frequency control and high switching frequency PWM control. The sinusoidal pulse width modulation technique is generally well known among all and broadly utilized in modern applications [2]. It is basic and more adaptable than SVM technique. SPWM technique uses several carrier waves and one reference wave per phase. The number of carrier waves used will be (n-1) where n is number of levels. The switching strategy comes under level shift pulse width modulation technique. The SPWM level shift can be further be classified as:

1.Phase disposition (SPWM-PD)

2.Phase opposition and disposition (SPWM-POD)

3.Alternate Phase opposition and disposition (SPWM-APOD)

Advantages of multicarrier PWM techniques

1. Easily extensible to high number of levels.
2. Easy to execute.
3. To distribute the switching signals accurately so as to limit the switching losses.
4. To compensate unbalanced dc sources.

Out of these techniques of SPWM we have used Phase opposition and disposition technique in the switching scheme to trigger the gate circuit as it has most reduced line-to-line harmonic voltage distortion is achieved by it. To build a 15 level output waveform through the LS-SPWM strategy 14 carrier waves are required. Here in this, positive seven carrier waveforms are out of phase with negative seven carrier waveforms

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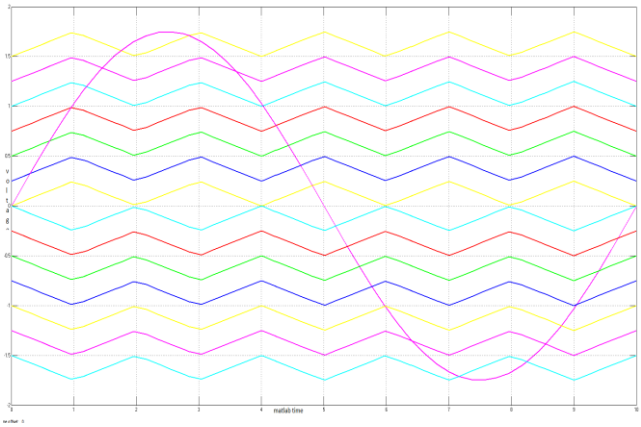
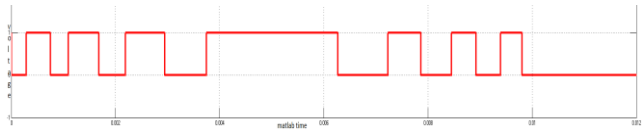


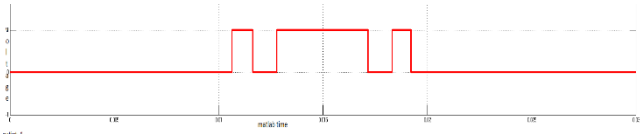
Fig 2 Schematic arrangement of the SPWM-POD strategy with carrier and sinusoidal reference wave

V SWITCHING PULSES

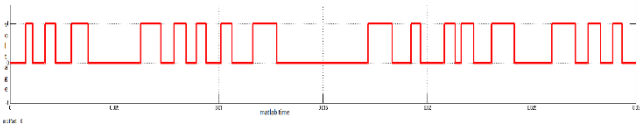
The switching sequence for every 13 switches utilized in the fifteen-level inverter configuration is appeared in following diagrams



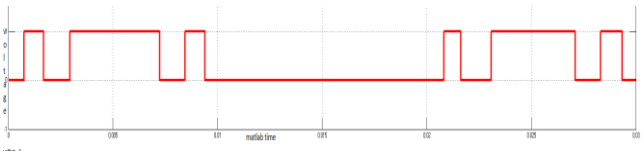
Switching pulse for S1



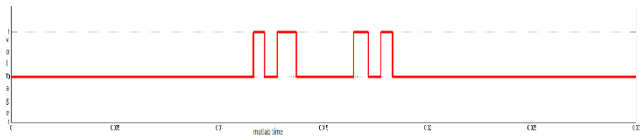
Switching pulse for S2



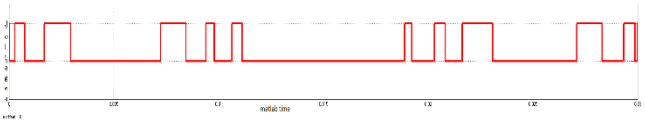
Switching pulse for S3



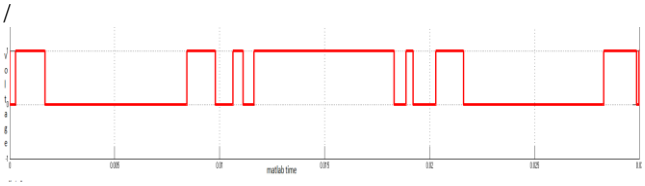
Switching pulse for S4



Switching pulse for s5

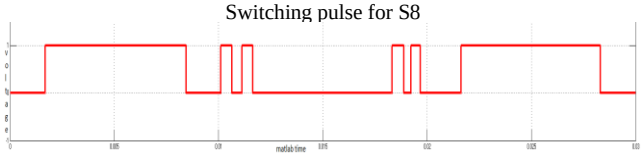


Switching pulse for s6

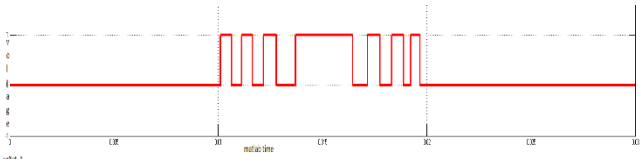


Switching pulse for s7

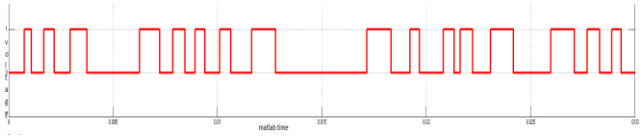
Switching pulse for S8



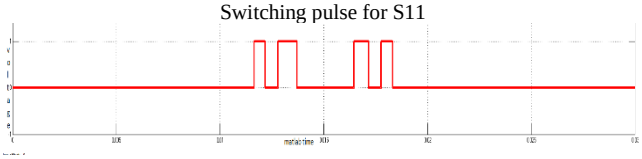
Switching pulse for S9



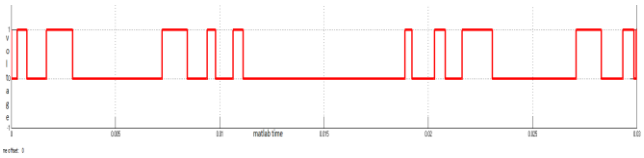
Switching pulse for S10



Switching pulse for S11



Switching pulse for S12



Switching pulse for S13

VI MATHEMATICAL MODELLING

By utilizing this topology, the number of levels synthesized can be increased by increasing the no of sources. As the number of levels increases the no of switches used also increases. The higher the no of levels, the lower the no of switches used for synthesizing these levels compared with

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the no of switches used for the lower levels [5]. Generalized formulas have been proposed for these topologies for obtaining the voltage levels and the no of switches used as the no of sources increased. In this manner, The number of levels that can synthesized using the proposed topology is

$$N=2^{(n+1)}-1 \qquad (1)$$

Where N represents the number of levels and n represents the voltage sources.

The number of switches used that can be used for the topology is

$$S=5n-2 \qquad (2)$$

Where S represents the switches

and n represents the voltage sources used.

VII VOLTAGE STRESS

A significant parameter which determines the expenses of the multi-level inverter is the blocking voltage of the power switches as well as the DC voltage sources. If the proposed inverter requires a variety of blocking switches then the cost of the inverter is too high. The voltage blocking depends on the topology of the inverter. Power switches are used to open and close a circuit. At the point when a circuit is opened, current moving through it is interfered. Change in current with small change in time(di/dt) will be very high. This causes the switches to melt or fuse. The maximum voltage that each switch experiences at its OFF state with out being damaged is called voltage stress.

The voltage stress across each switch is given in the below

Switch	Corresponding voltage stress
S1	V_1+V_2
S2	V_1+V_2
S3, S11	V_3
S4	V_2+V_3
S5, S12	V_2+V_3
S6, S13	V_1+V3
S7	V_3
S8	V_3
S9	V_1+V_2
S10	$V_1+V_2+V_3$

VIII SWITCHING TABLE

Utilizing appropriate switching combinations we acquire the desired output level of the 15 levels multilevel inverter .The output waveform contains fifteen voltage levels with both positive and negative half cycles along with a zero level . Switching sequence for the proposed topology is indicated the underneath table 1

V_1=1volt; V_2=2volt; V_3=4volt 1=TURN ON and 0=TURN OFF.

Voltage	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13
1V	1	0	0	0	0	1	1	0	0	0	0	0	1
2V	0	0	1	1	0	0	1	0	0	0	1	0	0
3V	1	0	0	1	0	0	1	0	0	0	0	0	0
4V	0	0	1	0	0	1	0	1	1	0	1	0	1
5V	1	0	0	1	0	1	0	1	1	0	0	0	1
6V	0	0	1	1	0	0	0	1	1	0	1	0	0
7V	1	0	0	0	0	0	0	1	1	0	0	0	0
-1V	0	0	1	0	0	0	0	0	1	1	1	0	0
-2V	0	1	0	0	0	1	1	0	0	0	0	0	1
-3V	0	1	0	0	0	0	0	0	1	1	0	0	0
-4V	0	0	1	0	1	0	1	0	0	0	1	1	0
-5V	0	0	1	0	0	0	1	1	0	1	1	0	0
-6V	0	1	0	0	1	0	1	0	0	0	0	1	0
-7V	0	1	0	0	0	0	1	1	0	1	0	0	0
0V	1	0	0	0	0	0	0	0	1	1	0	0	0

Table 1. switching sequence for the proposed topology

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IX SIMULATION RESULTS

In this paper MATLAB/SIMULINK is utilized for simulation. In SIMULINK the 15 level inverter circuit is simulated and result of output voltage and THD are shown in following figures. The output waveform has 7 levels in both positive and negative half cycle that include zero level that happen twice in a cycle. This voltage level are achieved with the help of three asymmetric voltage sources. The simulation results for the 15 level multi-level inverter is shown in the figure 3

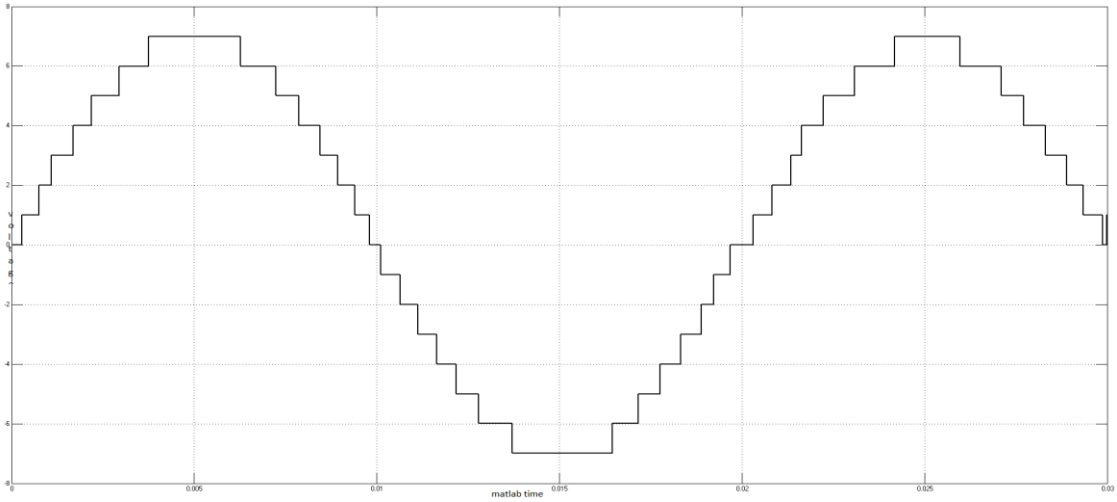

Fig 3: simulation result for the 15 level multi-level inverter.

X TOTAL HARMONIC DISTORTIONS

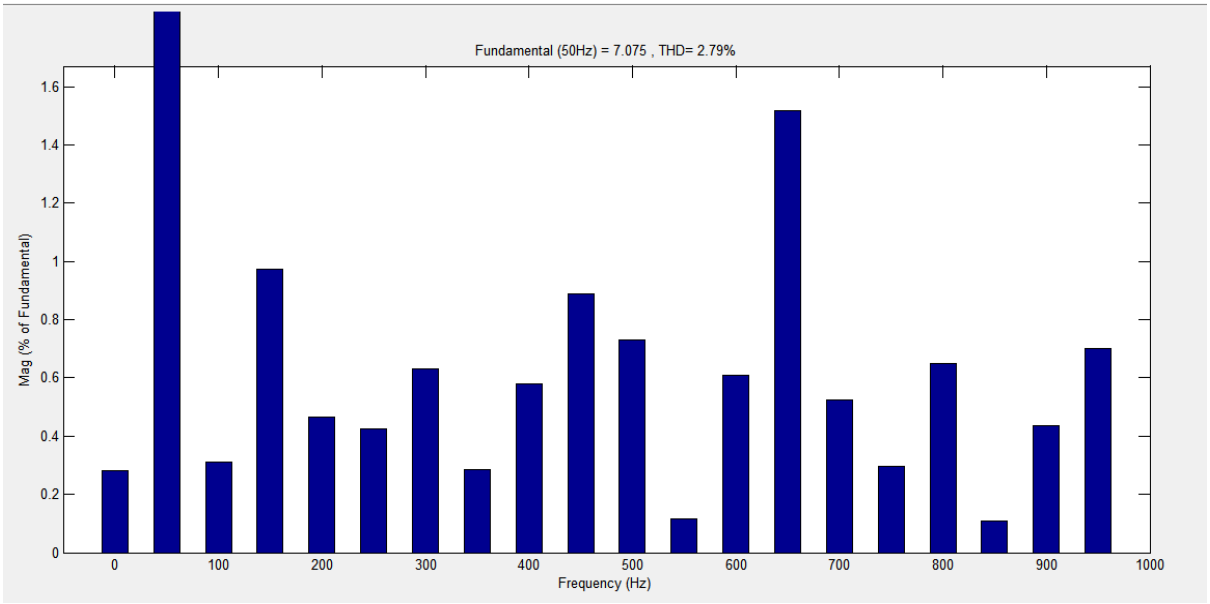

Fig 4.FFT analysis for proposed topology

The circuit simulation is done in MATLAB and the output current waveform is analyzed for THD utilizing FFT method. From the figure 4 we can conclude that the number of harmonics present in the output and the THD is found to be 2.79% for the fundamental frequency of50HZ.

XI COMPARISON OF THD FOR DIFFERENT CARRIER WAVES

Analysis which was done for different carrier waves such as triangular, trapezoidal, ramp and sawtooth and reverse sawtooth signal with a sine wave as reference at a fundamental frequency of 50hz.

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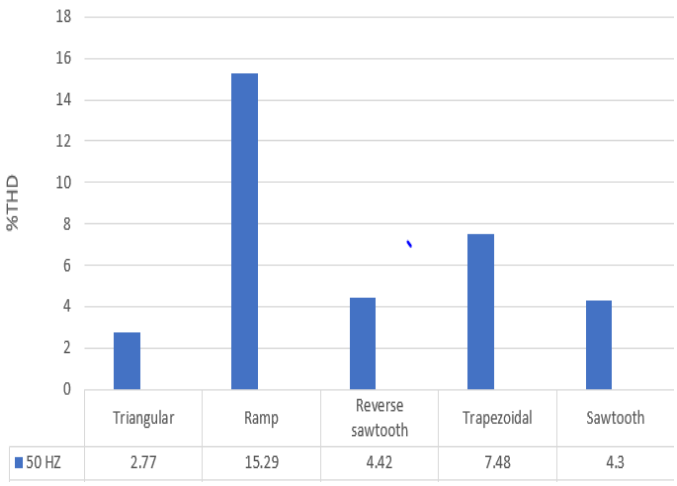

Fig 5. Comparison of THD'S for different carrier waves

The following chart provides the analysis of THD% for above simulation using different carrier waves at a fundamental frequency of 50Hz.we can conclude that the SPWM technique using triangular wave as carrier wave seems to be efficient. It is because the THD and harmonic elimination for the triangular wave is less as compared with the other waves as carrier signal.

XII COMPARISON OF THD FOR DIFFERENT MODULATION TECHNIQUES

Analysis is done for different modulation techniques with triangular wave as carrier and sine wave as reference for a fundamental frequency of 50hz. The following chart provides the analysis of THD % for above simulation. From the above analysis we can say that the scheme of SPWM-POD provides lower THD as compared to other two of the SPWM technique.

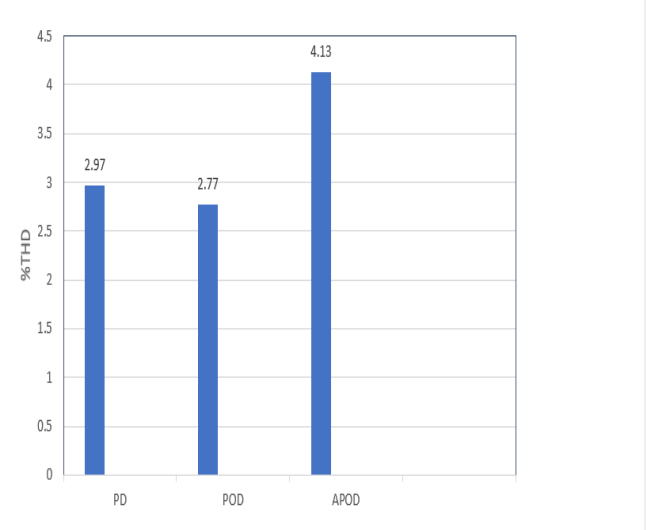

Fig 6. THD analysis for different modulation technique

XIII COMPARISON OF THIRD HARMONICS FOR DIFFERENT CARRIER WAVES

One of the significant impacts of power system harmonics is to increase the current in the system. This is simply because of the 3rd harmonics which causes the sharp increment in zero sequence current and this leads to increase in the current of neutral conductors due to which overheating of neutral wires, windings, losses in power generation and transmission. 3rd harmonics for various carrier waves of triangular, ramp, saw tooth reverse saw tooth and trapezoidal at a frequency of 50 Hz is done.

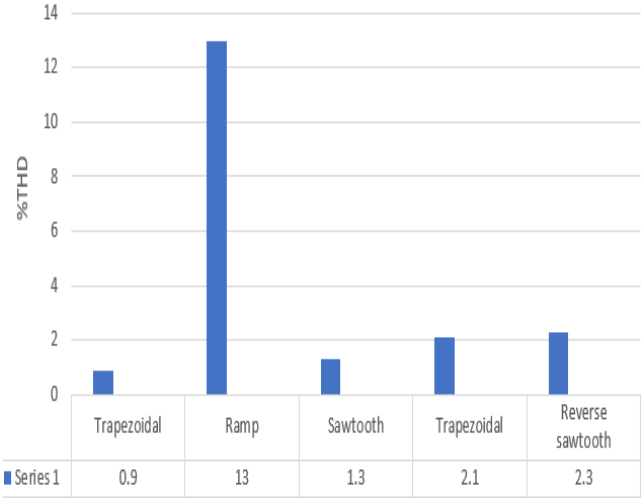

Fig7. Comparison of 3rd harmonics for different carrier waves.

Comparison of 3rd harmonics for with different carrier waves with sine wave as reference for fundamental frequency of 50hz. From the analysis we can conclude that 3rd harmonics are much lower in triangular as carrier wave

XIV COMPARISON OF 3RD HARMONICS FOR DIFFERENT MODULATION TECHNIQUES

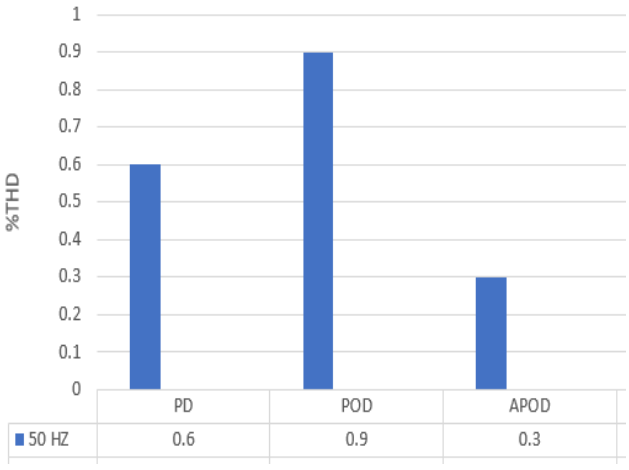

FIG 8. comparison of 3rd harmonics for different modulation techniques

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Here analysis is done for 50HZ for sinusoidal pulse width modulation techniques using triangular wave as carrier. Out of which third harmonics are much reduced in SPWM-APOD technique.

XV CONCLUSION

A new topology has been proposed for the 15level asymmetrical multi- level inverter with lower THD. They are broadly satisfactory for power application ranges in medium and high power due to their advantages. The main purpose of MLI is to provide limit over the total harmonic distortion (THD), electromagnetic interference (EMI), voltage stress on the switches and dv/dt problem and hence it is mostly preferred in recent concepts due to its benefits. SPWM technique used for producing low total harmonic distortion without the usage of the filter. The simulations are done in MATLAB/SIMULINK. Here the output has maximum output voltage of 7v for DC voltage values of 1,2 and 4 v respectively. For practical load purpose the DC voltages can be adjusted to get 230v. From the FFT analysis we can observe that the Total Harmonic Distortion (THD) is obtained as 2.79%. The simulation and experimental results show that the THD of the proposed inverter is considerably alleviated.

XVI FUTURE SCOPE

The number of levels got by this topology can be reached out by increasing the number of voltage sources. The THD of the output diminishes for expanding the number of levels. By combining the single-phase subsystem of 15 level multilevel inverter topology to 3 subsystems we can develop a 3-phase subsystem to run motors.

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