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ASIC Implementation of DADDA Multiplier

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***Abstract*—The demand of high speed processing has been increasing as a result of expanding computer and signal processing applications. Low power consumption is also an important issue in multiplier design. The objective of a good multiplier is to provide a physically packed together, high speed and low power consumption unit. The power consumption and the speed of the digital systems mainly depend on the multipliers that are adopted in those digital systems. To improve the performance of any processors the efficient algorithm of multiplication has to be used in that processor. The main objective here is to perform the area, power and speed analysis by complete ASIC implementation of 128 bit dadda Multiplier using compressors in cadence innovus 90nm technology tool. Here, we basically optimize the power, area and time consumed by the multiplier and thus enhancing the speed of execution. The technique used for optimizing the dada multiplier is compression technique where the compressors are used to reduce the number of partial product levels which often reduces the area consumed by partial products and again this dada multiplier is optimized in physical design using 90nm technology to give a better results. The simulation, synthesis and physical design of dadda multiplier is performed using cadence software.**

Keywords—Dadda; Multiplier; Xilinx; Cadence innovus; physical design; ASIC

I. INTRODUCTION

A Dadda multiplier is an efficient hardware implementation of a digital circuit that multiplies two unsigned integers, Dadda multiplier was invented by computer scientist Luigi Dadda in 1965. It is similar to Wallace tree multiplier, dada multiplier consumes less area when compared to Wallace multiplier and dada multiplier is faster than Wallace multiplier, the area reduction in dada multiplier is mainly due to reduce in partial product levels by using dadda compression technique. For 2 bit operand multiplication both dadda and Wallace tree multipliers have same number of partial product addition levels but when operand bit size increases for 4 bit, 8bit and more the partial product addition levels of dada multiplier greatly reduces compared to Wallace tree multiplier and also dada multiplier is faster. For example in 8x8 multiplication by using Wallace tree multiplier it requires 12 partial product addition levels but in proposed dada multiplier it requires only 4 partial product addition levels, so there is a area reduction in dadda multiplier and it also consumes less power. The Dadda multiplier using compression technique architecture comprises of

- Computation of partial product by using array of AND gates.
- Reduction of partial product by using half adder, full adder and compressors.
- Carry propagation adder for the summation of reduced partial products.

Here, the complete physical design of proposed dada multiplier is performed i.e the ASIC implementation of multiplier is made using cadence innovus 45nm technology tool, so due to reduction in the area of dada multiplier by reducing the number of partial product addition levels, the result of ASIC implementation of dada multiplier shows lesser area and low power consumed by proposed dadda multiplier. In the physical design or asic implementation there are different steps involved like floor planning, power planning, placement of standard cells and finally routing. After completing all these steps a complete asic implementation of dada multiplier is made.

II. DADDA MULTIPLIER

The chip designer must always focus on optimizing the power consumption, area and delay of overall circuit. Speed of the circuit changes with the speed/delay of the multiplier therefore a lot of research has been done to increase the speed of multiplier. So that delay of the overall circuit can be reduced. Dadda multiplier using compressors for partial product reduction is a high speed and area efficient multiplier and is therefore of great importance in high speed applications and low power consumption.

The basic dada multiplier is shown in figure1. Where, after the generation of partial products the number of partial product rows is reduced in the next level by using compression technique. After the completion of second level the number of rows in the second level is also reduced by using compression technique to get the third level. In the third level there are only three rows and finally these three rows are reduced to two rows in the last level. This compression technique greatly reduces the area and power that is consumed by the multiplier and also increases the speed.

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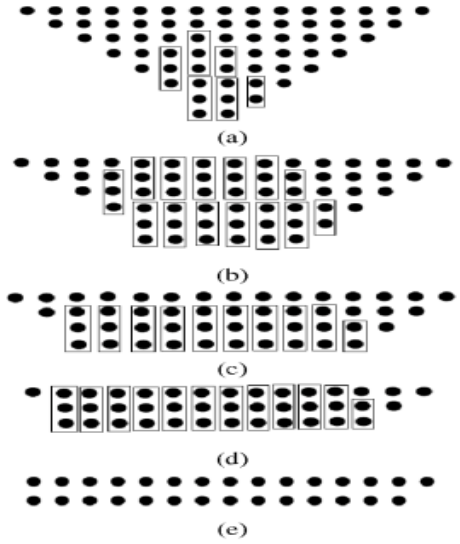

Fig. 1: Dadda multiplier partial product stage

III. PROPOSED 128 BIT DADDA MULTIPLIER USING COMPRESSOR

The architecture of proposed dada multiplier consists of less number of half adder and full adder to perform partial products addition. In this dadda multiplier, partial products are generated through AND gates and they are arranged in order as shown in the figure 2. The procedure for generating reduced number of partial products by dada multiplier using compression technique is as follows:

- In the first level of partial product the column with more than four partial products are separated first.
- The number of partial products in the separated column is reduced to four products compressors and full adders.
- In the second level the column with four products and three products are reduced to two by using half adders and compressors.
- Finally we are getting columns with two partial products.

In the final stage, it requires effective digital adder structure for doing binary addition process. So the carry propagation adder is used to get the final result of multiplication.

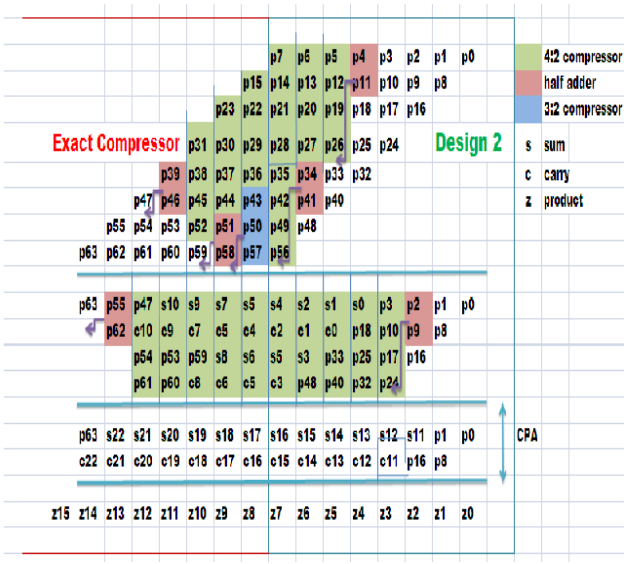

Fig.2.: Proposed dadda multiplier using compressors

IV. ADDERS

A. *Half Adder*

The half adder is an example of a simple, functional digital circuit built from two logic gates. The half adder adds two one-bit binary numbers (AB). The output is the sum of the two bits (Sum) and the carry (Carry).

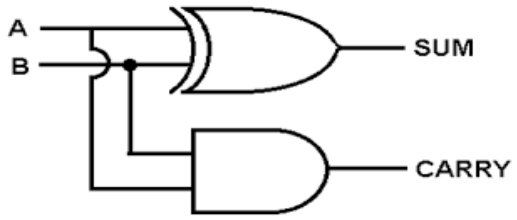

Fig.3: Half Adder

$$\text{Sum} = A \wedge B \quad (1)$$

$$\text{Carry} = A \& B \quad (2)$$

B. *Full Adder*

A full adder is a logical circuit that performs an addition operation on three one-bit binary numbers. The full adder produces a sum of the three inputs and carries value.

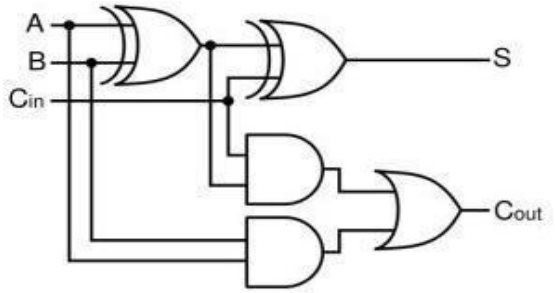

Fig.4: Full Adder

$$S = A \wedge B \wedge Cin \quad (3)$$

$$Cout = (A\&B)|(B\&Cin)|(Cin\&A) \quad (4)$$

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V. FOUR TWO COMPRESSOR

The four two compressor consists of five inputs and two outputs which mainly used for partial product addition

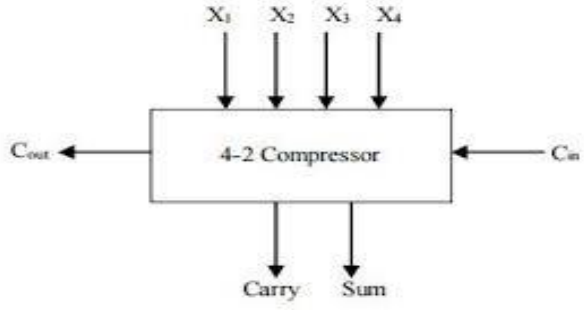

Fig. 5: Four-Two Compressor

VI. VERILOG SIMULATION RESULTS

The figure 6 shows the simulation results of the dada multiplier which multiplies two binary numbers and provides the exact result of multiplication by using compression technique of dadda multiplier where A and B represents two input operands and C represents the output. The simulation is performed using nclaunch simulator.

Fig.6: Simulation of Dadda multiplier

VII. CADENCE RESULTS

The figure7 represent the schematic of dadda multiplier, it is the result obtained the synthesis of verilog code. The tool used for the synthesis of verilog code is genus tool. After synthesis of verilog code by using genus tool, the power and area report of complete schematic is generated and also netlist file will be generated which is the input for physical design.

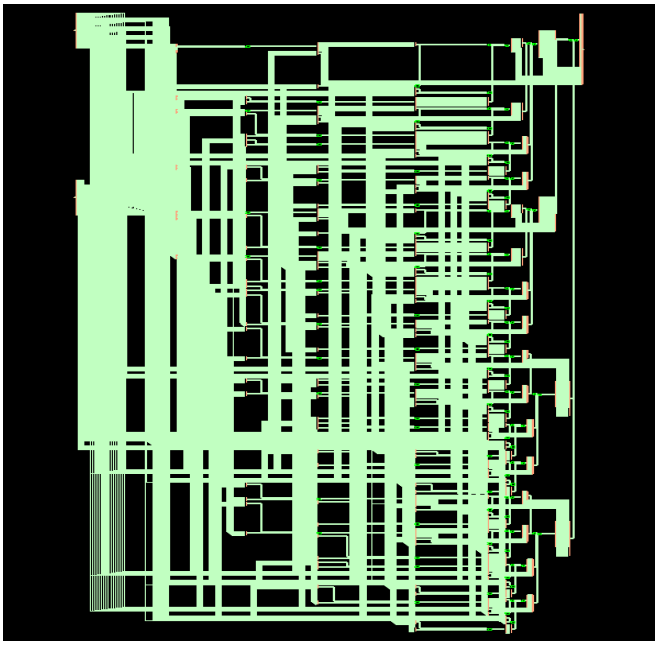

Fig.7: RTL Schematic of 128 bit dada multiplier using Cadence.

The figure 8 represents the floorplanning of 128 bit dadda multiplier, after performing the synthesis, the netlist will be generated according to the schematic. where this netlist is the input for the physical design of proposed dadda multiplier. The physical design is performed by using a tool called cadence innovus with 90nm technology. In floor planning, first the design is imported and then the power planning is made by adding power rings and power grids.

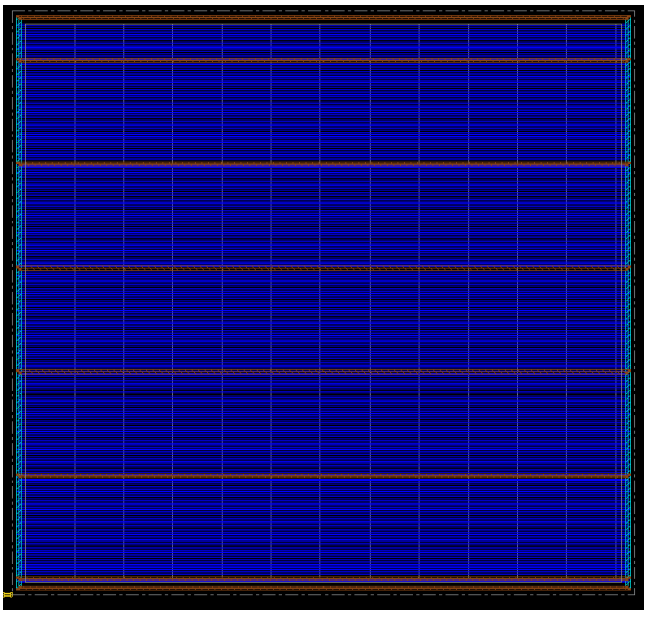

Fig.8: Floor planning of 128 bit dadda multiplier

The figure 9 shows the complete placement of standard cells after floorplanning. In this step all the standard cells will be placed and also the pin assignment will be made. To perform complete placement the netlist file generated during synthesis and technology files are imported.

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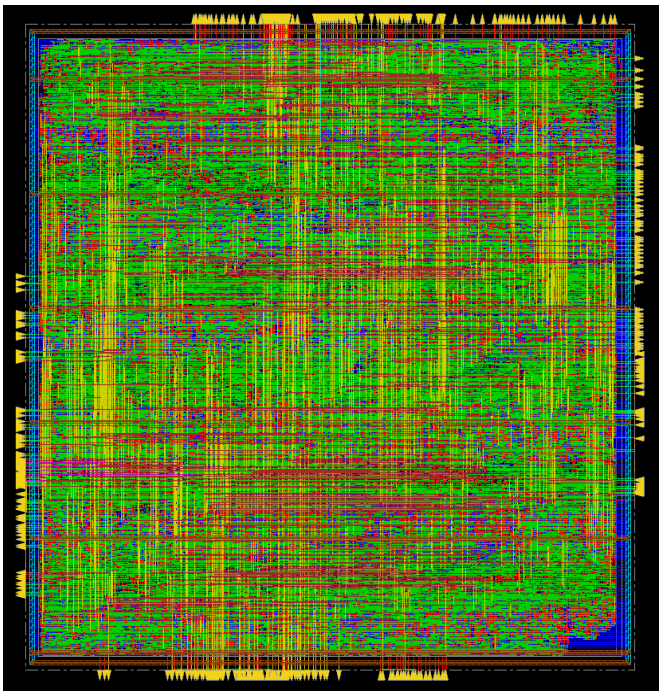

Fig.9: Final placement of 128 bit dadda multiplier

The figure 10 represents the routing of standard cells which is performed after placement.

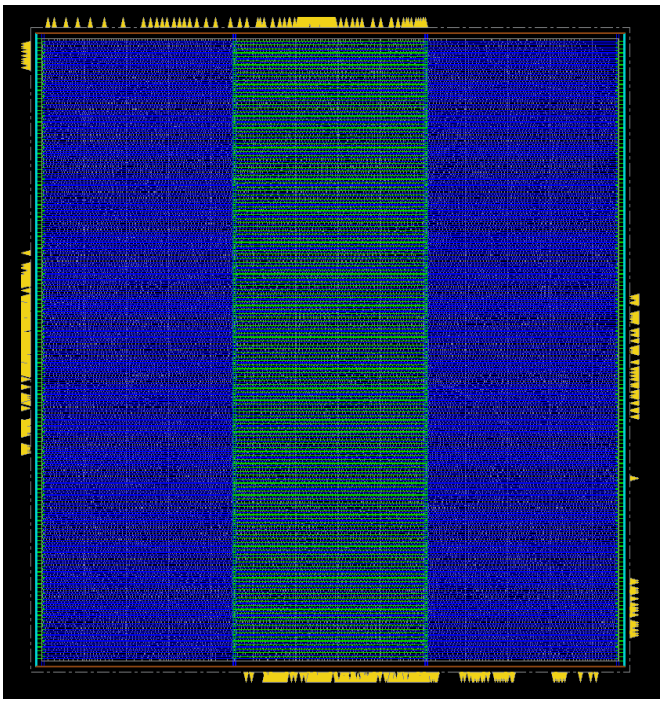

Fig.10: Routing of 128 bit dadda multiplier

The figure 11 shows the changes in the delay when area is optimized among different multipliers. As shown in figure 9 dadda multiplier consumes less time when compared to other multipliers this is achieved by using compression technique in partial product addition.

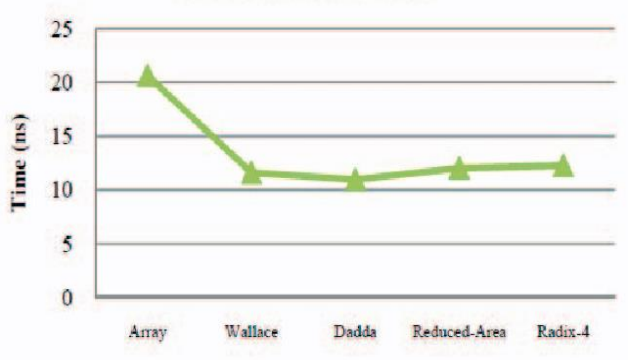

Fig. 11: Delay changes when area optimized among different multipliers.

VIII. REPORT

A. AREA(Cell) Report

Generated by: Genus(TM) Synthesis Solution 17.22-s017_1
Module: Dadda multiplier
(balanced_tree) Wireload mode: enclosed
Area mode: timing library

Table 1: Area analysis of dada multiplier

Instance	Cell count	Cell area um^2	Total area um^2
128-bit	40086	415409.411	415409.411
64-bit	9878	102282.921	102282.921
32-bit	2398	24788.474	24788.474
16-bit	564	5808.450	5808.450
8-bit	122	1329.116	1329.116

B. Gate Report

Generated by: Genus(TM) Synthesis Solution 17.22-s017_1
Module: Dadda multiplier
(balanced_tree) Wireload mode: enclosed
Area mode: timing library

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Table 2: Area analysis of inverter and logic cells

Type	Instance	Area um^2	Area%
Inverter	2433	5524.613	1.3
Logic	37653	409884.798	98.7
Total	40086	415409.411	100.0

Table 3: Each gate area of dadda multiplier

Gate	Instances	Area(um^2)
ADDFX1	15958	314043.849
ADDHXL	2837	34357.205
AND2X1	319	1448.707
AOI21XL	385	1748.439
AOI2BB1XL	319	1931.609
CLKINVX1	2433	5524.613
CLKXOR2X1	128	1065.715
NAND2XL	469	1419.944
NOR2XL	16769	50769.824
OA21X1	396	2697.592
OA21XL	31	211.175
OAI21XL	42	190.739

C. Power Report

Generated by: Genus(TM) Synthesis Solution 17.22-s017_1
Module: Dadda multiplier
(balanced_tree) Wireload mode:enclosed
Area mode: timing library

Table 4: Power analysis of dadda multiplier

Instance	Cells	Leakage power(w)	Dynamic power(w)	Total power(w)
128-bit	40086	0.00188	0.0367	0.0386
64-bit	9878	0.00046	0.0082	0.0087
32-bit	2398	0.00011	0.0017	0.0019
16-bit	564	0.000026	0.00034	0.00037
8-bit	122	0.0000064	0.000058	0.000065

IX. CONCLUSION

In this paper an 128-bit Dadda Multiplier using compression technique is designed using Verilog code. The simulation, synthesis and physical design of the binary dada multiplier is performed using Cadence software with 90nm technology. The total power consumed by complete physical design of the proposed binary dada multiplier is 0.0386 watt which shows that the power consumed is greatly reduced when compare to the excising multiplier. In this proposed system the area and power consumption of 8-bit,16-bit,32-bit,64-bit and 128- bit dadda multiplier is analyzed which gives better results compare to existing multipliers.

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