Area-Efficient VLSI Implementation for Parallel FIR Digital Filter Structures of symmetric convolutions based on Fast FIR Algorithm

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ABSTRACT

A New parallel FIR Filter structures is proposed in this paper. It based on fast-finite impulse response (FIR) algorithms, which are advantageous to symmetric convolutions of even length in terms of the hardware cost. Under this condition using number of taps is multiple of 2 or 3. The proposed parallel FIR Filter architectures benefit are the inherent nature of symmetric coefficients are used. It is reducing half number of multipliers in the sub filter section at the expense of increase in additional adders in preprocessing and postprocessing blocks. Exchanging multipliers with adders is beneficial because adders weigh less than multipliers in terms of silicon area, and moreover, the increase in adders in preprocessing and postprocessing blocks stay fixed, do not increasing the length of the FIR filter, and

the number of reduced multipliers increases along with the length of the FIR filter.

Overall, the proposed new parallel FIR structures can lead to significant hardware savings for symmetric convolution in even length from the existing FFA parallel FIR filter; specifically the length of the filter is large.

INDEX TERMS

Digital signal processing (DSP), fast FIR algorithms (FFAs), parallel FIR, symmetric convolution, very large scale integration (VLSI).

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1. INTRODUCTION

The parallel FIR digital filer can be used for high performance and low power (supply voltage with reduced) applications. Finite- impulse response (FIR) digital filters are mostly used fundamental devices performed in DSP systems, ranging from wireless communications to video and image processing.FIR filter operate in high frequencies in some applications such as video processing, but cellular wireless communication used in high throughput with a low-power circuit such as multiple-input multiple-output (MIMO) systems in some other application. Additionally, the much higher order FIR filter is unavoidable for narrow transition band characteristics are required. In the

other hand, DSP applications are used in parallel and pipelining process. Both two techniques can reduce the power consumption by lowering the supply voltage, sampling speed does not increase in this type. Parallel processing in the digital FIR filter will be discussed in this paper. Due to its linear increase in the hardware implementation cost bring the increase in the block size *L*, the parallel processing technique loses its advantage to be employed in practice implementation. The past [1]-[9] papers proposing way to reduce the complexity of parallel FIR filter. In [1]-[4], handle in polyphase decomposition in main part. The small-sized parallel FIR filter structures has first derived and then the larger block-sized can be constructed by cascading or iterating small-sized parallel FIR filtering blocks. In [1]–[3] introduced in Fast FIR algorithms (FFAs) that can be implement an *L*-parallel filter using approximately (2*L* − 1) sub filter blocks, each of length N/L. FFA structures are successfully break the constraint that the hardware implementation cost of a parallel FIR filter has a linear increase along with the block size L. the required number of multipliers are reduced to (2N-N/L) from L x N. In [5]–[9], the fast linear convolution is utilized to more advanced the small-sized filtering structures and then a long convolution is decomposed into several short convolutions, i.e., larger block-sized filtering structures can be build in iterations of the small-sized filtering structures.

Whatever, in both categories are comes to symmetric convolutions, the symmetry of coefficients has not been taken into consideration for the design of FIR structures yet, which can lead to a extensive saving in hardware cost. In this paper, we will discuss symmetric convolutions based on even length and provide new parallel FIR digital filter Architectures based on FFA consisting of advantageous polyphase decomposition, which can further reduce amounts of multiplications in the sub filter section by exploiting the inherent nature of the symmetric coefficients, compared with the existing FFA based on parallel FIR filter structures. This brief description is organized as follows.

A brief introduction of FFAs is presented in Section 2. In Section 3, the Symmetric convolution based proposed FFA structures are presented. In Section 4, shown in the Comparison table. Finally given the conclusion in section 6.

2. FAST FIR ALGORITHM (FFA)

Consider the general formulation of a *N*-tap FIR filter

$$y(n)=\sum_{i=0}^{N-1}h(i)x(n-i),\qquad n=0,1,2,\ldots,\infty \quad (1)$$

Where {h(i)} are length-N FIR filter coefficients and {x(n)} is an infinite-length input sequence. Then, the polyphase decomposition representation of a traditional L-parallel FIR filter can be expressed as

$$\sum_{p=0}^{L-1}Y_p(z^L)z^{-p}=\sum_{q=0}^{L-1}X_q(z^L)z^{-q}\sum_{r=0}^{L-1}H_r(z^L)z^{-r} \quad (2)$$

Where

$$X_q(z)=\sum_{k=0}^{\infty}z^{-k}x(Lk+q),$$

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Hr(z) = $\sum_{k=0}^{\frac{N}{L}-1} z^{-k} h(Lk+r)$, and

$$Y_p(z) = \sum_{k=0}^{\infty} z^{-k} y(Lk+p),$$

For p, q, and r = 0, 1, 2,. . ., L − 1.

A. 2 × 2 FFA (L = 2)

From equation (2), a two-parallel FIR filter can be expressed as [1], [3]

Y0 =H0X0 + z−2H1X1

Y1=H0X1+z−2H1X0. (3)

However, equation (3) can be written as

Y0 =H0X0 + z−2H1X1,

Y1 = (H0 + H1) (X0 + X1) − H0H0 − H1H1. (4)

The two-parallel (*L* = 2) FIR filter implementation using the FFA obtained from equation (4) is shown in Fig. 1.

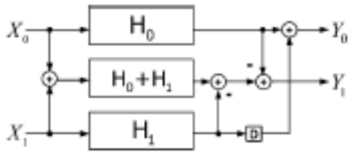

Fig.1 Two- Parallel FIR filter implementation using the FFA.

B. 3 × 3 FFA (L = 3)

The same approach, a three-parallel FIR filter using FFA can be expressed as [1], [3]

$Y_0=H_0 X_0 - Z^{-3} H_2X_2+Z^{-2} x [(H_1+H_2) (X_1+X_2)- H_1X_1]$

$Y_1= [(H_0+H_1) (X_0+X_1) – H_1X_1] - (H_0X_0-(H_0X_0- Z^{-3}H_2X_2)$

$Y_2= [(H_0+H_1+H_2) (X_0+X_1+X_2)] - [(H_0 + H_1) (H_0+X_1)-H_1X_1] – [(H_1+H_2) (X_1+X_2) - H_1X_1]$ (5)

The implementation obtained from above equation and it is shown in Fig. 2.

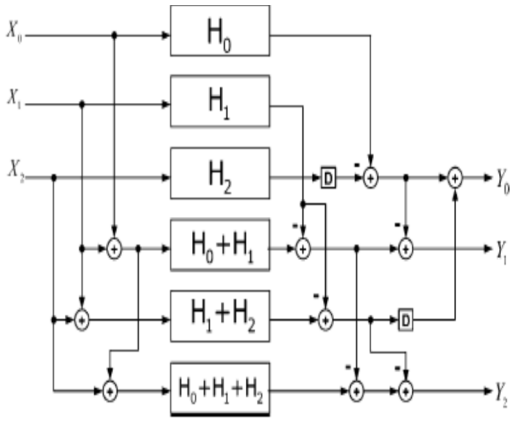

Fig.2. Three-parallel FIR filter implementation using the FFA.

3. PROPOSED STRUCTURES FOR SYMMETRIC CONVOLUTIONS

To using the symmetry of coefficients, the main idea is to handle the polyphase decomposition to earn as many subfilter blocks as possible, which contain symmetric coefficients so that half the number of multipliers with in a one subfilter block can be utilized for the multiplications of whole taps. Therefore, for an N-tap L-parallel FIR filter the total amount of saved multipliers would be the number of sub filter blocks that have symmetric coefficients times half the number of multiplications in a single sub filter block (N/2L).

3.1 SYMMETRIC CONVOLUTION BASED FFA (L=2)

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From equation (4), a two-parallel FIR filter can be written as

Y0={1/2[(H0+H1)(X0+X1)+(H0-H1)(X0-X1)]-H1X1}+Z-2H1X1,

Y1=1/2[(H0+H1)(X0+X1)-(H0-H1)(X0-X1)] (6)

When it using the set of even symmetric coefficients, (6) can gain one more sub filter block have symmetric coefficients than (4), the existing FFA two parallel FIR filter. The fig.3 are derived in Equ (6) and architecture are shown in the below diagram.

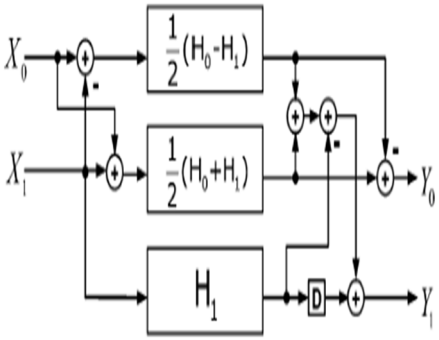

Fig.3 Proposed Two- Parallel FIR filter implementation using the FFA

3.2 SYMMETRIC CONVOLUTION BASED FFA (L=3)

With the same approach, from (5), a three-parallel FIR filter can be written as (7). The implementation of the proposed three-parallel FIR filter shown in the Fig. 4. The number of symmetric coefficients N is the multiple of 3, the proposed three-parallel FIR filter structure presented in (7) give four subfilter blocks with symmetric coefficients in total, compare the existing FFA parallel FIR filter structure has only two ones out of six subfilter blocks. Fig. 5 can also be comparison figure; the shadow blocks stand for the subfilter blocks which contain symmetric coefficients.

The N-tap three-parallel FIR filter, proposed structure is symmetric convolution based structure can save N/3 multipliers from the existing FFA structure. Whatever, again the process of proposed three-parallel FIR structure also brings an overhead of seven additional adders in preprocessing and postprocessing blocks

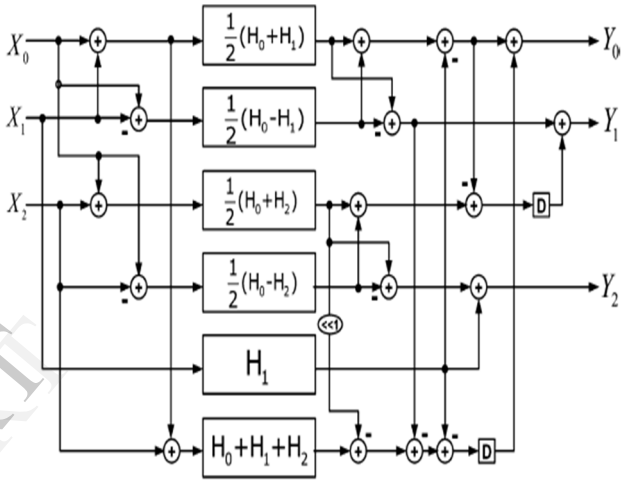

Fig.4 Proposed Three- Parallel FIR filter implementation using the FFA

3.3 PROPOSED CASCADING FFA

The proposed cascading process for the larger block-sized proposed parallel FIR filter is introduced in [1]. However, a small change is adopted here for lower hardware consumption. As we can see, the proposed parallel FIR structure enables the of multipliers in parts of the subfilter blocks but it also gives more adder cost in preprocessing and postprocessing blocks. When cascading process for the proposed FFA parallel FIR structures is larger parallel block factor L, the increase of adders can also larger. Therefore, other

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than applying the proposed parallel FIR filter structure to all the decomposed subfilter blocks, the existing FFA structures which have more compact operations in preprocessing and postprocessing blocks are worked for those subfilter blocks that contain no symmetric coefficients, whereas the proposed parallel FIR filter structures are still applied to the rest of subfilter blocks with symmetric coefficients. The implementation of the proposed cascading process in the four-parallel FIR filter (L=4) is shown in the Fig .5. The proposed four-parallel FIR structure gain three more subfilter blocks containing symmetric coefficients than the existing FFA one, which means N-tap FIR filter can save the 3N/8 multipliers, at the cost of 11 additional adders in preprocessing and postprocessing blocks. By this cascading process, parallel FIR filter structures have larger block factor L can be realized. The proposed six-parallel FIR filter structure earns 6 more symmetric subfilter blocks, the N-tap FIR filter can save equivalently N /2 multipliers, than the comparison of existing FFA , with the overhead of additional 54 adders. Also, the proposed eight-parallel FIR filter structure will lead to seven more symmetric subfilter blocks, the N-tap FIR filter can save equivalently 7N /16 multipliers, than the existing FFA, with the expense of additional 54 adders.

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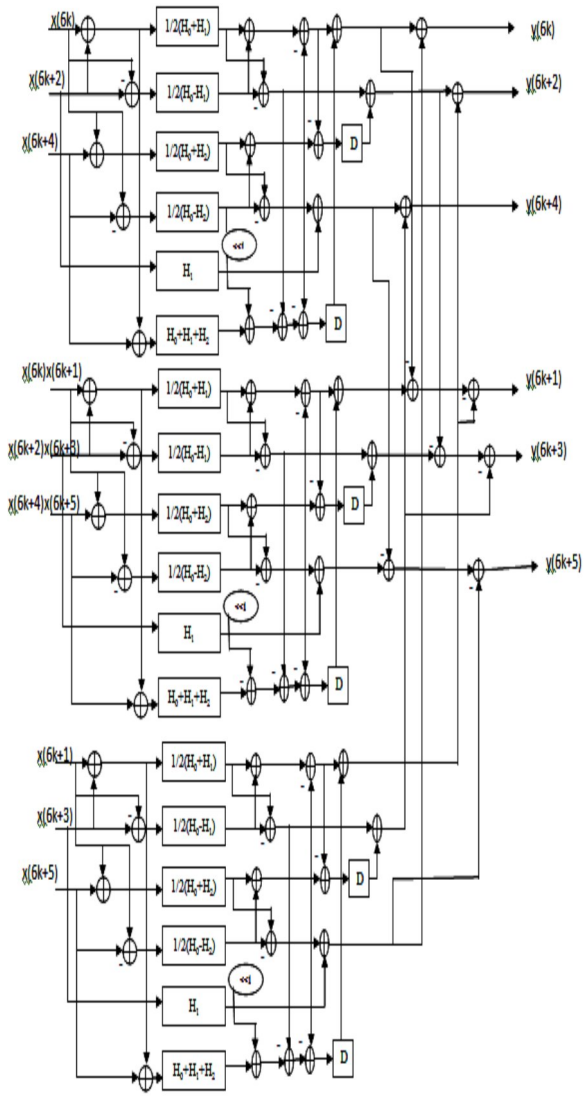

Fig.5 Proposed Six- Parallel FIR filters implementation using the FFA.

CONCLUSION

In this paper proposed new parallel FIR filter structures, which are advantageous to symmetric convolutions of even length in terms of the hardware cost. Under this condition using number of taps is multiple of 2 or 3.multipliers are the main part in hardware consumption for the parallel FIR filter implementation. The proposed

parallel FIR Filter architectures benefit are the

Table 1: Comparision of AREA

	Non-Symmetric 6-Parallel Structure for 24-tap Fir Filter (area utilized)	Symmetric 6-Parallel Structure for 24-tap Fir Filter(area utilized)
Number of Bonded IOBs	81%	81%
Total Number of 4 input LUTs	60%	51%
Number of occupied slices	65%	55%
Peak Memory Usage	176 MB	172 MB

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inherent nature of symmetric coefficients are used. It is reducing half number of multipliers in the sub filter section at the expense of increase in additional adders in preprocessing and postprocessing blocks. Exchanging multipliers with adders is beneficial because adders weigh less than multipliers in terms of silicon area. moreover, the amount of increased adders stays still when the length of FIR filter becomes large, the number of reduced multipliers increases with the length of FIR filter. Since, the larger of FIR filter is can save the proposed structures from existing FFA structures, with reduce hardware cost.overall,in this paper , we have provided new parallel FIR structures consisting beneficial polyphase decompositions dealing with symmetric convolutions dealing with symmetric convolutions comparatively better than the existing FFA structures in terms of hardware consumption

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