Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 10 Issue 01, January-2021

Area Efficient High Speed Multi Operand Adder using 22nm Strained Silicon CMOS Technology

J Swathi[1], Dr. K. Kalai Selvi[2]
[1]Student, M.E -VLSI design, SNS College of Technology, Tamil nadu, India
[2]Dean, Dept. of ECE, SNS College of Technology, Tamil nadu, India

Abstract **- In this proposal work, the ripple carry adder (RCA)-based binary tree adder (BTA) is analysed to find the possibilities for area minimization. Based on the analysis, critical path of carry is taken into the new logic implementation and the corresponding design of RCA are proposed for the BTA. The RCA is designed for m bits (m=8,16,32 bits) offers better efficiency in terms of area, delay than the existing RCA. Using this RCA design, the multi-operand adder (n=8,16,32) BTA structure is proposed. The synthesis is done at 22nm Cmos technology. Result reveals that the proposed BTA-MOA provides the efficient results in area minimization and also delay efficient structure for multipliers and other applications. Therefore, this binary tree adder based multi-operand design can be a better choice to develop the efficient digital systems for signal and image processing applications.**

Key Words: Ripple Carry Adder, Binary Tree Adder, Multi Operand Adder, AOI Gates, OAI Gates

1.INTRODUCTION

Multi-operand adders are important for arithmetic design blocks especially in the summation of partial products of hardware multipliers. Multi-operand adders are required for building multipliers where multiple partial products must be added up to have the multiplication result. Since most of the power is consumed at the arithmetic blocks, especially at multipliers, lower power devices with lower switching noise is desirable [2].

The operands considered for addition can be single bit or of multiple bits, thus the input and output of the adder can be in multiple bits [3]. Multi-operand adder can be represented simple by an architecture comprising of a compressor tree, which reduces the partial sum and propagated carry [3]. There are numerous types MTA but the adders used in this work are Array tree adder, Wallace tree adder, Balanced delay tree adder and Overturned-stairs tree adder. For any arithmetic functioning unit, adders are the most important components because of its resource consumption and the delay involved in processing. Adders also form a part of multipliers which is another resource intensive component of arithmetic circuits [3]. The simplest MOA is a binary tree adder (BTA), designed by connecting two-operand adders in binary tree configuration for the addition of multiple operands [5]. The delay and energy efficiency of the Binary tree adder structure depends on the performance of adders used in the structure. There are numerous types of adders such as ripple carry adder (RCA), carry-look-ahead adder (CLA), parallel prefix adder (PPA), carry-select adder (CSLA) and carry-skip adder (CSKA), which can be used to develop the BTA structure, where each adder has its own tradeoffs between area, delay and energy consumption.

Among all adders, RCA has less area and energy with higher delay, whereas other adders (fast adders) having less delay with higher area and energy. On the other side, area and energy are the two major constraints in most of the systems which demand the addition of a large number of operands. The Binary tree adder employed in these systems should be area and energy efficient.

2. LITERATURE SURVEY

Multi-operand summation, which is widely used in block designs and fast functions. The research is done in different angles for realization of highly efficient multi-operand addition for medical IoT field devices. The conventional adders used in the multipliers and filters for summation of the intermediate results tends to area and delay occurrence. Multi-operand addition and compressor trees can be used more efficiently for decimal operations, which will reduce the delay without much overhead in area [1]. For enhancement of area consumption, delay and power, different multiplication techniques such as add and shift method and Wallace tree (WT) multiplier are used for the multiplication [6].

However, the adder structures suggested for CLA and PPA [7-14] are efficient in terms of delay but they occupy a large area and consume more energy, whereas the structure suggested for RCA in [15,16] involves less area and energy with higher delay. Therefore, the carry selects scheme-based adder [17] has been suggested to achieve the performance between RCA and CLA. Plus, Carry Select Adder is maybe the fastest adders utilized in numerous information processing. It is evident that there is extension for lessening the area and power utilization in the CSLA [18,19].

To significantly reduce the area and power of the CSLA, the design uses a simple gate-level alteration. 8, 16, 32, and 64 bits square-root CSLA (SQRT CSLA) architecture depending on changes have been developed and compared with the regular SQRT CSLA architecture. In [20], binary to the excess-1 converter-based logic design approach is suggested for the implementation of CSLA to reduce the area and power. Besides, the Australian computer scientist Chris Wallace has developed another type of efficient MOA known as Wallace tree adder (WTA) [15]. In this Wallace tree adder, operands could be reduced to two words by using the carry-save adders and finally these two words are added together by another two-operand adder to compute the result of addition [15]. The carry-save adder is designed using full adders (FAs) and it introduces only one FA delay. BTA is more popular than Wallace tree adder and used in numerous applications due to

International Journal of Engineering Research & Technology (IJERT)
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its simple and regular structure but its delay is a major concern.

3.EXISTING WORK

It is found that there is no notable attempt made in the literature for the delay refinement of RCA-BTA. Therefore, to explore the possibilities for delay minimisation of RCA-BTA structure, the critical path delay analysis is presented [5]. It is observed that most of the work proposed in the literature is mainly focused on to improve the design metrics of fast adders which can enhance the performance of the WTA structure. From [5], it is clear that the WTA has less delay in comparison to RCA-BTA but its structural irregularity needs the redesign of WTA for different values of N. On another hand, the BTA structure is simple and regular, which can easily be designed for any value of N. Although, the delay of RCA-BTA can be improved by the minimisation of RCA delay, whereas the WTA performance can be enhanced by the usage of an efficient fast adder at the final addition stage.

3.1 NEW LOGIC FORMULATION

The RCA design proposed in the work [5], depends on new logic of replacing the AOI gates and OAI gates in place of carry operation. Since, area is minimized but the delay analysis is done by critical path analysis by considering xor gates and the AOI/OAI gates used.

The area for the RCA in [5] is calculated by the following equation,

$$A_{RCA} = (m/2)\, A_{AOI-FA} + (m/2)\, A_{OAI-FA} \quad (1)$$

Similarly, the delay for the RCA [5] is given by following expression,

$$T_{RCA} = (m/2)\, T_{AOI} + ([m/2] - 1)\, T_{OAI} + 2T_{XOR} \quad (2)$$

The binary tree adder is designed using this RCA design and compared with other adders for its performance in terms of delay and power. The delay for the RCA -BTA is calculated by given expression,

$$T_{RCA-BTA} = 2T_{XOR} + (m-2)\, T_{AOI} + (\log_2 N - 1)(T_{AOI} + 2T_{XOR}) \quad (3)$$

4.PROPOSED WORK

The proposed RCA is based on existing work using new logic formulation, But the AOI/OAI gate's inputs depend on XOR gate, previous full adder carry, and also the AND gate.

In this paper the delay of OAI/AOI gates depends on all possible inputs to AOI/OAI gate. And for comparison it is proposed at various bit widths (m=8,16,32bits). the proposed ripple carry adder is used for binary tree structure for adding multiple operands, as (N=number of operands, N=8) eight operands with each operand of 16 bits.

The Multi-operand structure proposed is RCA-based BTA, where the adder designs are synthesised in Synopsys Design Compiler using H-spice simulation software at 22 nm CMOS. Power used as supply voltage is reduced to 0.8v. The proposed RCA design provides better efficiency in terms of area, delay and energy than the existing RCA.

4.1 DELAY ANALYSIS

The delay analysis is done on the critical path on which carry is carried out. The path includes the delay of XOR gate, AND gate and AOI/OAI gates. In the previous work only XOR gate and AOI/OAI gates, where in the practical AND gate delay is also added for full adder.

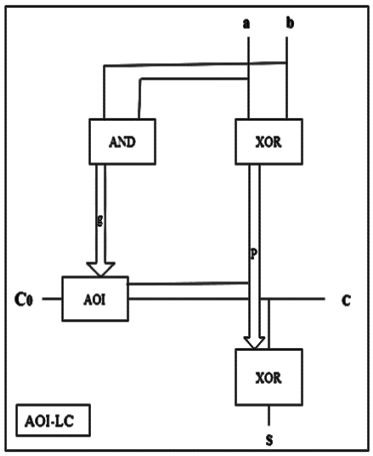

Fig.1 AOI-Full Adder

The AOI gate in fig.1 has the inputs of (g , p , c),thus delay of three circuits decides the delay in critical path.

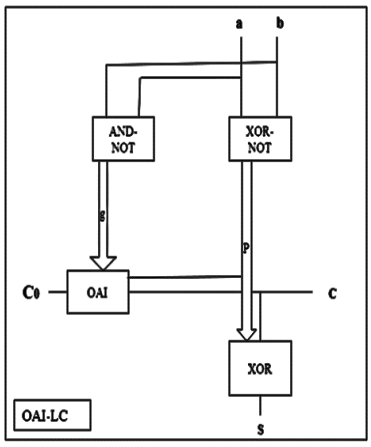

Fig .2 OAI-Full Adder

The OAI gate in fig.2 is the complement of AOI circuit, where the inputs to the OAI gate (g,p) are given as inverted. Since the output of AOI-FA is in inverted form. The OAI-FA is used next in series to AOI-FA. These two circuits are used in alternative manner. The delay in AOI/OAI -FA is calculated by following expression,

$$T_{AOI/OAI-FA} = T_{XOR} + T_{AND} + T_{AOI/OAI} \quad (4)$$

Where the $T_{AOI/OAI-FA}$, T_{XOR}, T_{AND}, $T_{AOI/OAI}$ are the delays of AOI/OAI adder, XOR gate delay, AND gate delay and AOI/OAI gate delay.

Since the circuits are designed in 22nm Cmos technology, they are consumption of area is reduced and circuits works efficient in terms of power and delay.

4.2 RCA DESIGN

The above AOI/OAI based Full adder is used for the RCA design. The fig.3 is 4-bit Ripple carry adder, similarly *m*-bit RCA is designed (*m=8,16,32 bits*) and their area and delay is calculated, it is shown in results section.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 10 Issue 01, January-2021

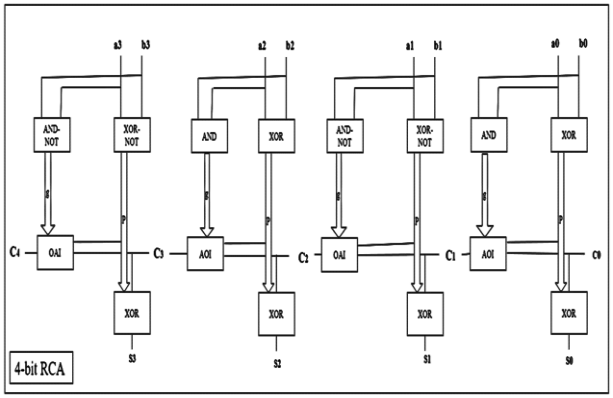

Fig .3 Four Bit RCA

The inputs are given simultaneously and each adder produces carry, the delay of each gate is calculated by the following general expression,

$T_{RCA} = (m/2)\ T_{AOI\text{-}FA} + T_{OAI\text{-}FA}$ (5)

The ripple carry adder delay is important since it is used for binary tree adder. The area is calculated using following general expression,

$A_{RCA} = (m/2)\ A_{AOI\ -\ FA} + (m/2)\ A_{OAI\ -\ FA}$ (6)

Where *m*-represents the number of bits, A is the area of particular gate.

4.3 BTA -MULTI OPERAND ADDER

The ripple carry adder designed is used to build binary tree adder (BTA), BTA is used in various applications. The BTA is designed using multiple operands as (a,b,aa,ab,ba,bb etc.,) ,the Multi-operand adder is defined by *N-bits* . where the *N* stands for number of operands. BTA structure is designed for (*N=8,16,32* Operands) each operand is of 16-bits.

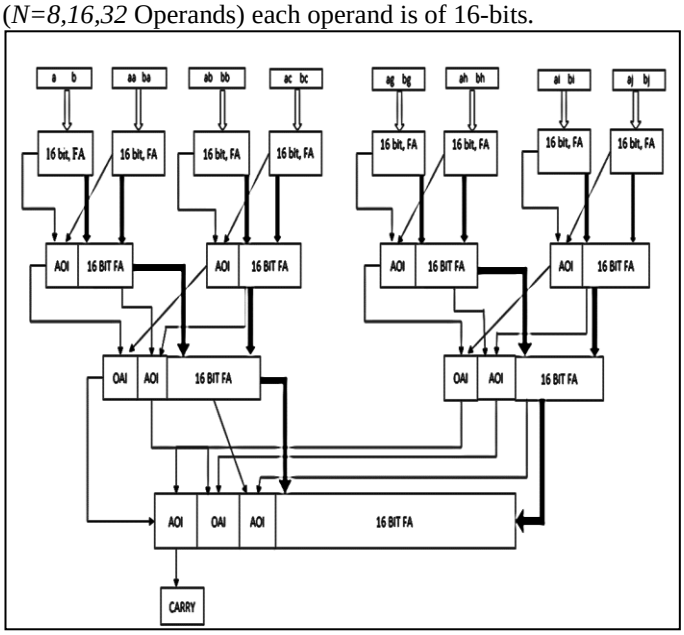

Fig .4 Proposed Structure N=16 Operands BTA

The delay for each structure is analysed and tabulated in terms of area and delay. In the fig.5 the light lines indicate the carry propagation and the dark lines is the sum propagation. The same structure is used for all binary tree, the stages is depending on N- value($\log_2 N$).

5. SYNTHESIS RESULTS

The synthesis of circuits is done using H-Spice simulation software, the result analysis shows circuits works efficiently in area and delay terms. The below table .1 gives the area and delay for each bit of Ripple carry adder.

Adder design	Bit width(m)	Area, μm^2	Delay, ns
RCA	8	1.211	17.3
	16	2.423	34.5
	32	4.846	69.5

Table .1 Results of RCA design

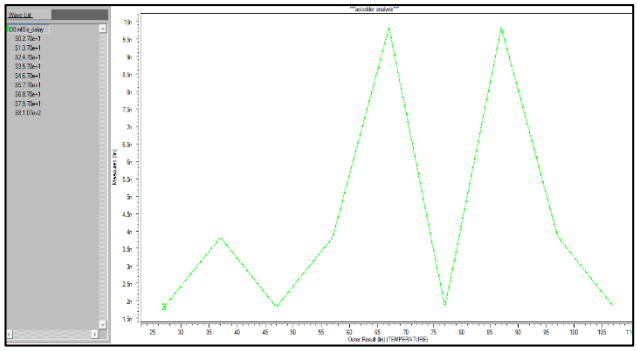

Fig .5 Delay Analysis Of AOI Adder

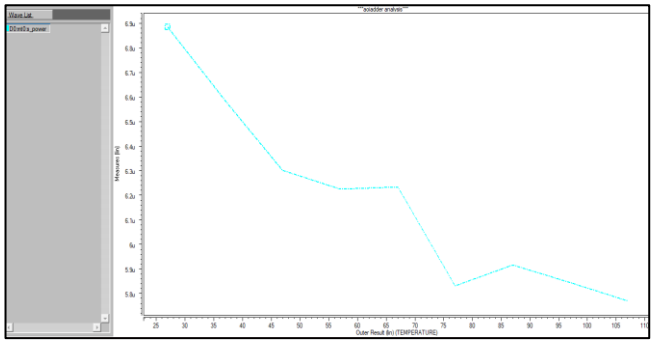

Fig .6 Power Analysis Of AOI Adder

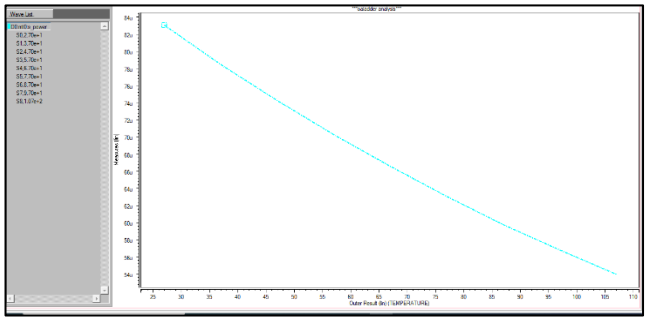

Fig .7 Power Analysis Of OAI Adder

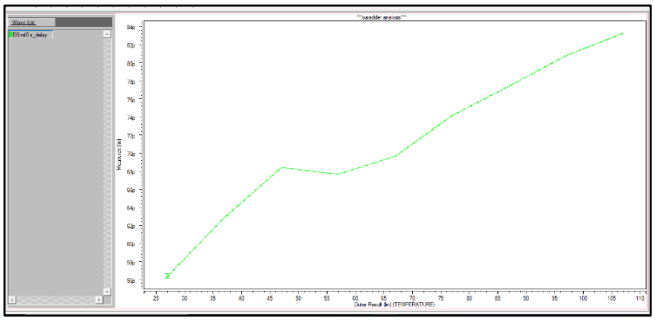

Fig .8 Delay Analysis Of OAI Adder

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 10 Issue 01, January-2021

The delay and area of the BTA design is also calculated in terms of micro-square meter, and delay in nano-seconds. The values defined in table .2 are approximate converted values.

Adder design	Bit width(N)	Area, μm^2	Delay, ns
Binary tree adder	8	27.24	34.99
	16	57.36	69.77
	32	117.75	174.55

Table .2 Results Of RCA -BTA Design

6. CONCLUSION

The RCA- BTA is widely used in Multi -operand adders due to its simplest structure that leads to area and energy efficient design. But, the long carry propagation path of RCA makes it poor in terms of delay performance. Therefore, the delay analysis of RCA-based BTA is presented in this paper. Based on the analysis on this work, the new logic formulation for RCA using complementary logic operations is derived and correspondingly the RCA design is proposed for the BTA for orders (*N=8,16,32)*.

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