Area & Dynamic Power Optimization of Cmos 1-Bit Full Adder Using Genetic Algorithm

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***Abstract*— A method to optimize the area and the power of 1-bit full adder using genetic algorithm is presented here. The full adder is analyzed for performance under different values of parameters. The circuit exhibits different characteristics for different values of load capacitance, frequency, width and length. The range of values for which the circuit works well are found and used as a input to the genetic algorithm to find the optimum set of parameters that should be used. The circuit under consideration is designed to be fabricated on .18u m technology. The resultant circuit has relatively high frequency, low dynamic power, optimized area and outputs which adhere to the satisfaction of the user. This method may be applied to other circuits as well to optimize their area and power.**

Keywords*— Full Adder, Low Power, Area optimization, Genetic Algorithm.

I. INTRODUCTION

Every aspect of our life may have a margin for optimization. Every situation that confront us may not be ideal and may require some changes. There is a scope of optimization in every daily life problem so as to maximize the results by utilizing our limited resources. Genetic algorithm is a technique that is based on the natural process of evolution and can be used for optimization. Darwin studied that a species may adapt itself one step closer to the environment with every upcoming generation. Only the fittest member of a particular generation will survive and reproduce to pass their characteristics to the next generation. While using genetic algorithm to solve complex search problems an initial population of chromosomes may be considered, each chromosome has a different fitness value. Only a few having

the required fitness value are selected to act as parents. Two parents may cross among themselves to produce an offspring. All the offspring together form the new population.

Here we are using the genetic algorithm to optimize the area and power of the VLSI circuits. As we know that area on the whole is dependent on the size of the components inside the circuits like transistors size (in terms of width and length), wire length or routing etc. The circuit under consideration has been developed on .18um technology using CMOS. When we vary the width and length of the CMOS transistors the area of the circuit starts changing accordingly. Reducing the width and length may give birth to some additional problems such as increase delay and it will decrease the speed of the device. There is a tradeoff between the W/L ratio and the delay.

We very well know that dynamic power dissipation dependent on three factors viz. load capacitance, frequency and supply voltage. We expect the genetic algorithm to find us the minimum value of every parameter for which the output is well within the acceptable limits. Here we confronted by the challenge of reducing the power dissipation at the cost of lower switching activity which can be considered as a decrease in the frequency of operation. Moreover when we try to reduce the supply voltage below a particular value it may harm the working of our logic circuit.

II. EARLIER WORK

Tarek. K darwish and Ahmed M. Shams designed a technique to generate low power cmos full adder circuit. They divided the full adder circuit into several smaller modules. These modules were redesigned to achieve lower power dissipation. Various modules were connected together to form low power cmos full adder. The problem with this method was the overhead involved in the design and analysis of each

module[1]. Amir Amirabadi and Ali Afzali Kusha tried to optimized power and delay of full adder circuit by using simulated annealing. A cost function of power and delay is computed using HSPICE and simulated annealing was implemented using MATLAB. The techniques helps in reducing the delay without allowing the power to increase significantly. Out of numerous simulated circuits it may be possible that some circuit may result in incorrect function, these circuits may be attributed a large cost [2]. 2002, Mohammed Sayed and Wael Badawy, proposed three new full adder circuits and compared thirty one others for power consumption. All the cells had different structures using XOR and XNOR gates. They tried to implement the circuit using .18, .25 and .35u m technologies. An additional buffer is used to generate the input signal, which is an extra overhead and might affect the power consumption of the circuit, but somehow this has not been taken into account [3]. Andew R. Conn and Paula K. Coulman tried to implement a circuit optimization tool that used augmented lagrangian formulation. This tool enables us to target delay, rise time fall time and area. Each of these can either be a constraint or an objective function. The w/l ratio may be changed and similar structure may be grouped together. Some of the circuits designed using this tool may not work according to the desired logic that is when a transition is to be measured it doesn't occur [4]. Yousef Mortazavi and Amir Amirabadi tried to optimize the sizing of digital adder circuits. The circuit is implemented on .35u m technology. The simulated annealing is employed to optimizing the size of full adder. The MATLAB code is used to implement the simulated annealing algorithm. So as to implement the suggested changes, the MATLAB code changes the parameters in the net list itself and thus reducing the number of steps involved in optimization. Out of numerous simulated circuits it may be possible that some circuit may result in incorrect function, these circuits may be attributed a large cost [5]. K. Navi and B. Mazloomniza proposed a full adder circuit with six transistors. They utilized multi valued logic for the operation of the circuit. The multi valued logic helps reduce the number of mos transistors and wiring requirement. In order to implement multi valued logic they made use of CML in this current is define to have logical levels that are integer multiple of reference current. The reduction in the transistor counts ultimately leads to the reduction of chip area. They have been able to achieve delays of as low as 150 pico seconds. [6]

III. SINGLE BIT FULL ADDER

The circuit under consideration is a simple one bit cmos full adder. It has three input (A, B & C) and two output sum and carry. In the three inputs two inputs A & B are the input variables (addend bits) and the third input C is the carry in. It performs binary addition between three inputs and generates corresponding sum and carry. Here we have used transistor level one bit full adder. [11]

The Boolean expression for full adder circuit is given as:

$$SUM = ABC+AB'C'+A'BC'+A'B'C$$

$$CARRY = ABC+ ABC'+A'BC+AB'C$$

Figure shows a basic CMOS full adder that was implemented using the cadence virtuso-4 tool. The Full adder circuit utilized 28 transistors. Fourteen of them are NMOS and the rest of them PMOS so as to complete the CMOS inverter structure. Our Full adder circuit is shown in the adjoining figure.

IV. DYNAMIC POWER

Dynamic power dissipation is caused by switching activities of the circuits. A higher operating frequency leads to more frequent switching activities in the circuits and results in increased power dissipation. The most significant source of

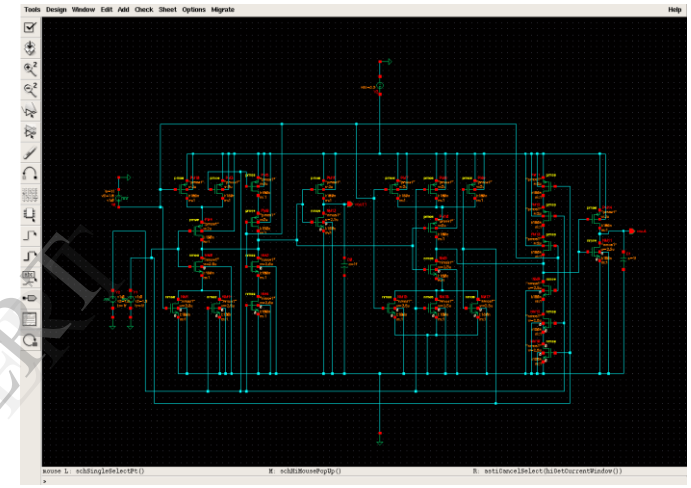

Figure-1: 1-Bit CMOS Full Adder Implemented On Cadence

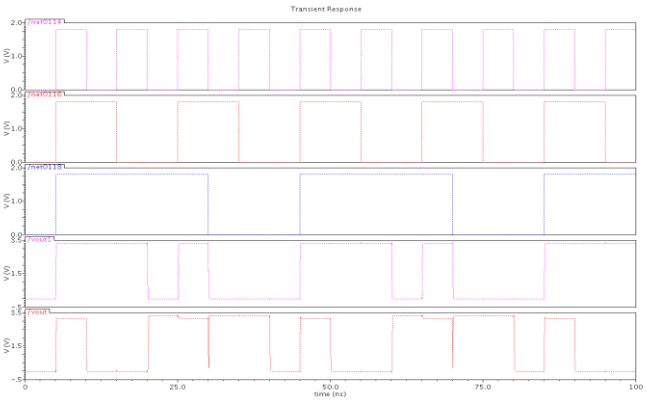

Figure-2: Output results of CMOS Full Adder

Dynamic power dissipation in CMOS circuits is the charging and discharging of capacitance. If we charge and discharge the capacitance at the frequency of f cycles per seconds, the dynamic power dissipation of the system is [4]

$$P = C_L V^2 f$$

Where C_L is the load capacitance, V is the supply voltage and f is the switching frequency.

V. AREA

In general the area on a integrated circuit can be considered to consist of two portion. First one is the area occupied by the components, second would be the space between the components that is used to lay interconnects. The channels (space occupied by interconnects) cover lesser space as compared to the space occupied by the components. So a general method to find the layout area is given by the following formula:

Area = width x length x number of transistors

VI. GENETIC ALGORITHM

The Genetic algorithm solves optimization problems by mimicking the principles of biological evolution, repeatedly modifying a population of individual points using rules modeled on gene combinations in biological reproduction. Due to its random nature, the genetic algorithm improves your chances of finding a global solution. It enables the user to solve unconstrained, bound-constrained, and general optimization problems, and it does not require the functions to be differentiable or continuous [7].

VII. RESULTS OBTAINED

The final set of dimensions for the optimized area as obtained by the genetic algorithm are 2.014u m, 180n m & 2.24u m, 180n m for nmos and pmos respectively, the value of area covered by the transistors in the circuit is 10.7205u m^2.

Similarly for dynamic power, optimized values obtained for capacitance and time period are 1p F and 9.354ns respectively. This means the value of frequency is 106.90 MHz. The optimized value for power is 1.16424422 mW. Here the operating frequency is quite high and the power dissipated is low.

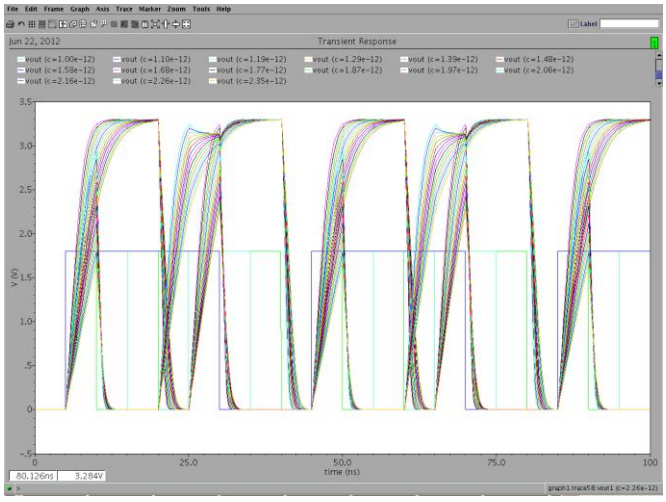

Figure-3: Parametric Analysis for Sum and carry

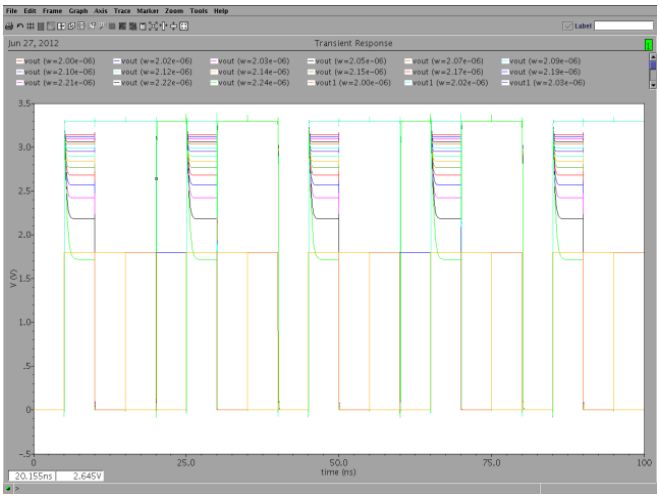

Figure-4: parametric analysis, when w=2um to 2.24um and l=180nm of PMOS

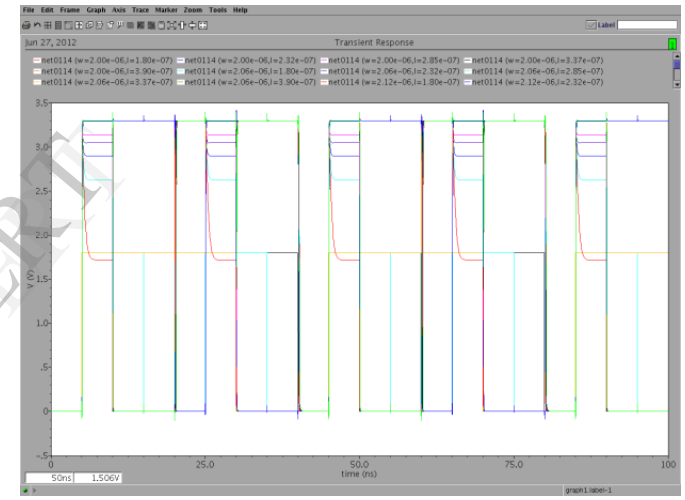

Figure-5: parametric analysis, when w=2um to2.24um and l=180nm to 390nm of PMOS

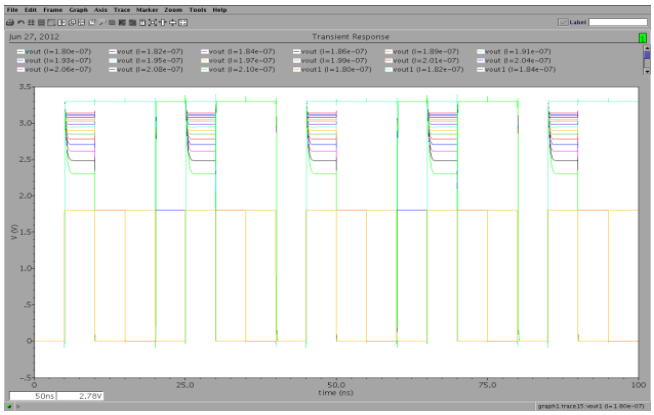

Figure-6: parametric analysis, when w=2.5um and l=180nm to 210nm of NMOS

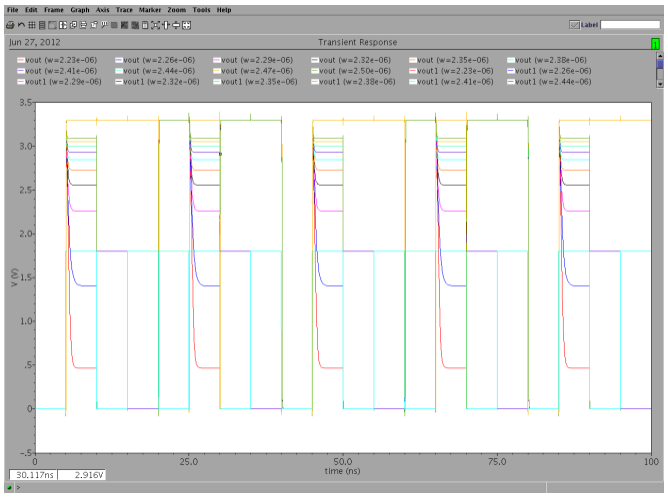

Figure-7: parametric analysis, when w=2.23um to 2.5um and l=180nm of NMOS

When we run the genetic algorithm in multi objective mode the optimized values obtained for capacitance and time period are 1pF and 8.865ns respectively. The optimized value for power is 1.228468 mW. The adjoining figure shows the results obtained through the genetic algorithm toolbox. Figure 10 & 11 shows the complete full adder layout in which none of the physical design rules are violated. This is checked by DRC (design rule checker), present in the tool itself.

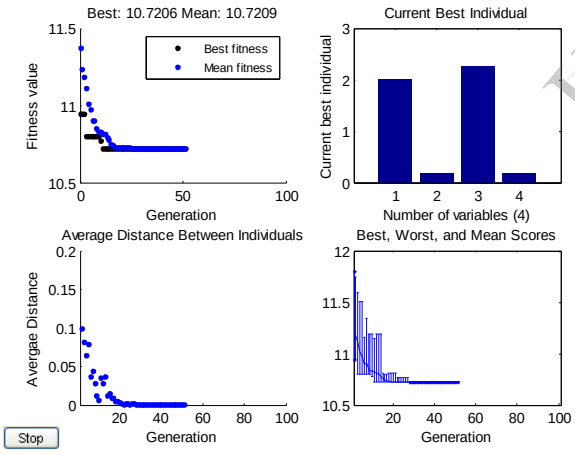

Figure-8: Execution of GA for optimized Area covered by the transistors

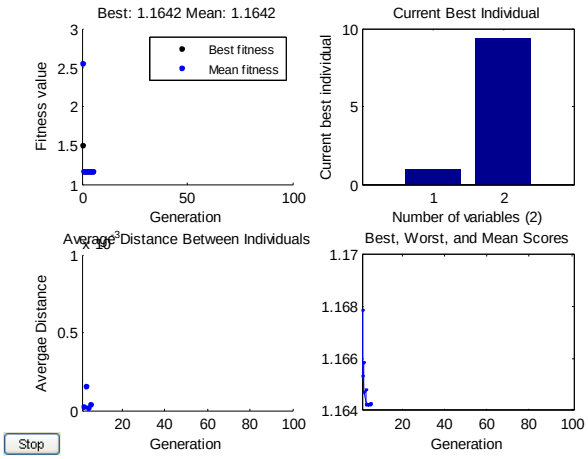

Figure 9: Execution of GA for Optimized Power

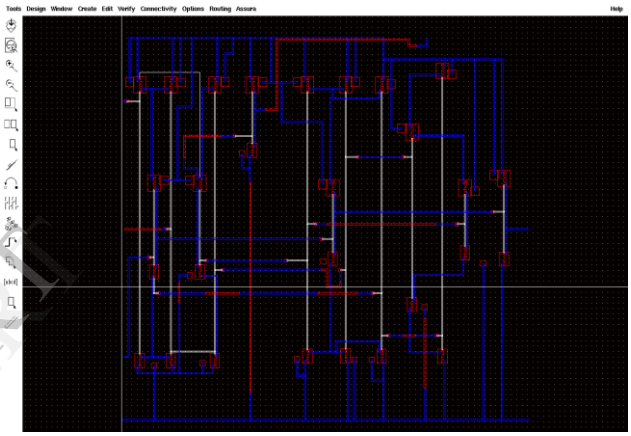

Figure-10 : final layout of full adder circuit

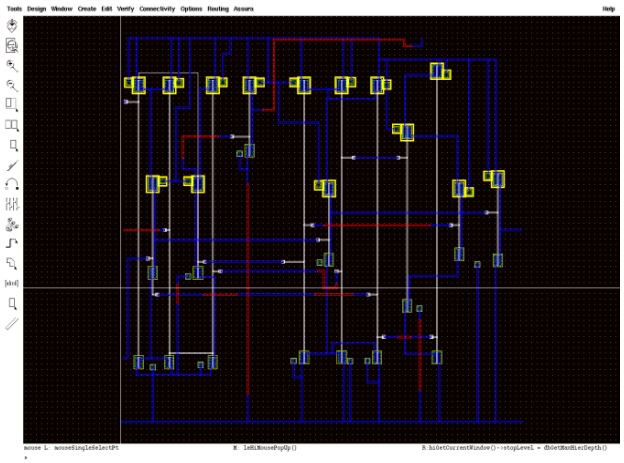

Figure-11: final layout of full adder circuit

IX. REFERENCES

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