International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 11, November-2014

Application of BIST Technology - A Review

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***Abstract* - The consumption of low power has become important in communication systems such as laptops, cellular phones etc. At the same time, design of modern technologies and packaging is difficult, and BIST (built-in-self-test) emerged as a solution for the VLSI testing problem. So, the reduction of energy consumption is the most interesting and challenging topic in electronic industry. BIST is a design for testability aimed at the detection of faulty components in a system by incorporating test logic on-chip. BIST is also known for its various advantages such as improved testability, speed of modules and support in system maintenance. Also BIST circuits are used in the current redistributions. This paper includes the reviews of BIST circuits with different implementation techniques.**

Keywords - Built-in-self-test, current redistribution.

I. INTRODUCTION

The dissipation in power has become a major objective in design of many application areas, such as wireless communications and high performance computing, that leads to the production of numerous low power designs. At the same time, power dissipation is also becoming a critical parameter during manufacture test, as the more power is consumed by the design than during functional mode of operation. As the throughput of test and manufacturing yield are often affected by test power and also most dedicated test methodologies have emerged over the past decade.

The present trends in the development of integrated circuitsand new advanced technologies enable integrationof complex digital and mixed-signal systems on a single chip.These complex systems, known as Systems-on-Chip (SOC), caninclude digital, analog, and RF circuits as well as MEMSstructures, micro sensors and another different core. No doubt,testability of the respective parts in such systems is greatlydecreased [1]. Standard test methods cannot be straightforwardlyused to test complex mixed-signal systems. Therefore,several automatic test equipment's (ATE), each dedicated toa particular core integrated in the system, would be needed. After discussing test power issues, promising low power test techniques to deal with nanometre system-on-chip (SOC) designs are presented. These techniques can be broadly classified into those that apply during scan testing and those that apply during scan testing and those that apply during built–in–self–test(BIST). Few of them are also applicable to test compression circuits or memory designs. In the literature, techniques that reduce power consumption during test application are generally referred to as power – conscious testing, power – aware testing, power – constrained testing, or low – power testing.

In [3]and [4] transient response analysis based test techniques wereproposed by converting the OpAmp into a voltage follower.With respect to the fault-free circuit, performance parameterslike overshoot and slew rate deviation were monitored todetect the faults in the OpAmp. In [5], an AC and DCcompacted testing technique was presented by monitoring andanalysing fault signatures through amplitude and offset ofvoltage signals.

II. PRELIMINARY WORKS

As on today we come across many techniques implemented on BIST using ADC and DAC. B.Kamalasoundari M.E. proposed the *Recursive Pseudo-Exhaustive Two-Pattern Generation Using BIST* i.e., Pseudo-exhaustive pattern generators for built-in self-test (BIST) provide high fault coverage of detectable combinational faults with much fewer test vectors than exhaustive generation. That can be given by following circuit diagram,

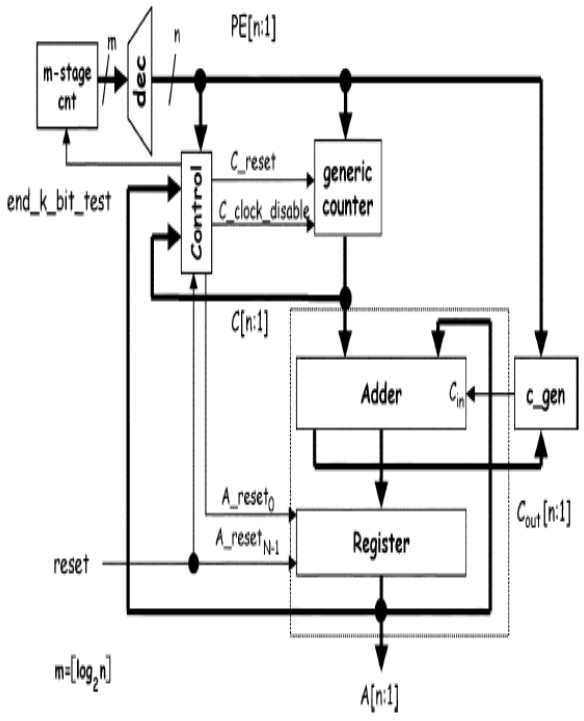

Fig.1. Recursive pseudo-exhaustive two-pattern generator

And also P. Pattunarajam*, G. NaveenBalaji proposed the *Economical scan-BIST VLSI circuits based on reducing testing time by means of ADP*i.e., Test power reduction done by Arbitrary Density Patterns (ADP) in which the effective usage of the WRP and TDP under adaptive control of clock is used. Weighted random patterns (WRP) and transition density patterns (TDP) can be effectively deployed to reduce test length with higher fault coverage in scan-BIST circuits. Analyse the effect of ADP on fault coverage. (Arbitrary density pattern = Weighted random pattern +Arbitrary density pattern).Adapt the scan frequency to the transition density for power constrained testing. This can be given by,

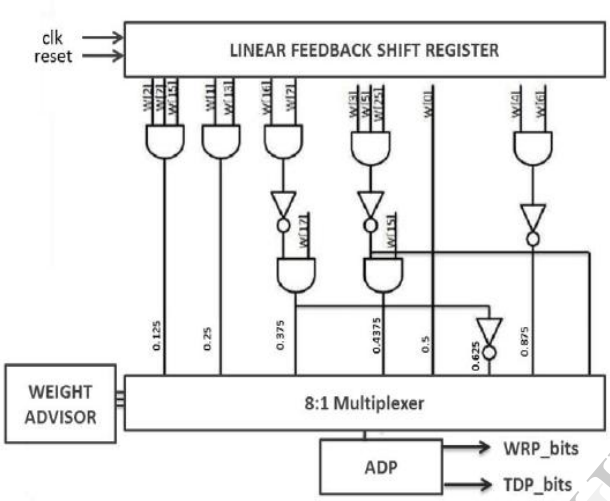

Fig.2. Block diagram of TPG

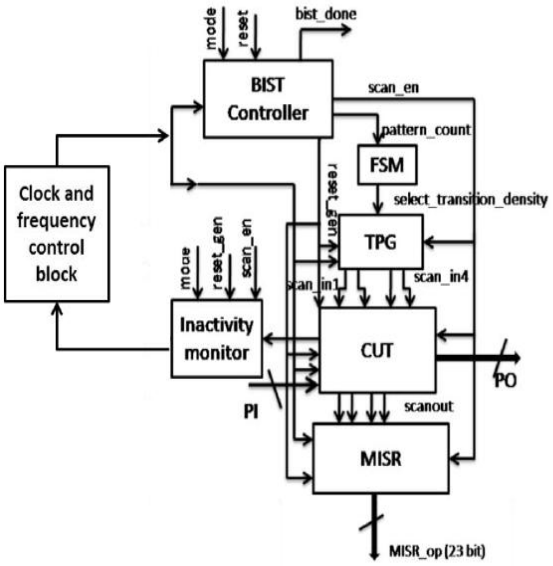

Fig.3. Implementation of one test per scan vector

For scan testing it is important to note that both power and test time contribute to the test cost as well as quality of the test. The lower transition density based vectors though need more number of vectors but the difference between numbers of the vectors needed to detect faults is small. Thus a lower transition density can be chosen deterministically to reach that partial coverage while speeding up the scan clock without crossing the power budget. Once the transition density is known the test application time can be further reduced by dynamically controlling the test clock keeping the test power controlled.

Again Jun Yuan and Masayoshi Tachibana proposed *A Two-Step BIST Scheme for Operational Amplifier* i.e.,this technique can particularly detect the capacitance variation in the compensation capacitor by combining the current-based test with the offset-based test to detect the physical defects in the OpAmp. This can be designed as follows,

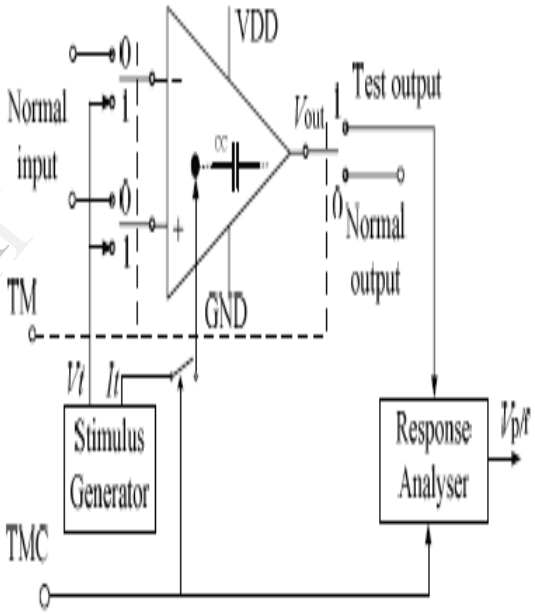

Fig.4. Defects in OpAmp

This is composed of a stimulus generator, response analyser and isolation circuits of analog switches controlled by external controlling signals TM and TMC. The whole test procedure is controlled by these two controlling signals. TM is the test mode start signal; TMC was designed to connect test current to the injecting node to form a test step current.The proposed BIST scheme can also be applied to test other amplifiers on the same chip with different window comparators.The disadvantages of this BIST scheme is large area overhead, but this situation would be improved in the multi-amplifier complicated circuits.

Further, Daniel Arbet, Viera Stopjakov´a, Juraj Brenku˘s, and G´abor Gyepes proposed*On-chip Parametric Test of R-2R Ladder Digital-to-Analog Converter and Its Efficiency* i.e., this deals with the investigation of the fault

detection in separated parts of a mixed-signal integrated circuit, example by implementing parametric test methods.For the operational amplifier, on-chip and off-chip approaches have been used to compare the efficiency. This can be implemented using the following design,

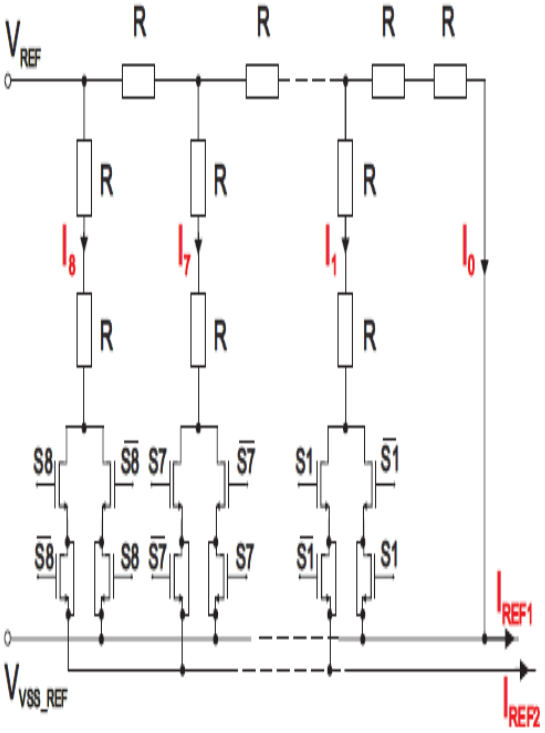

Fig.5. Circuit diagram of R-2R ladder

The R-2R ladder is a resistor network that uses a cascaded structure of current dividers, which generate binary-weighted currents in the respective branches.In ideal case, the dividing ratio should be 2:1 but because of resistors mismatch, in reality, the divisions will be imperfect.

The most probable fault in the resistor ladder is that the value of a resistor exceeds its tolerance band (parametric fault).These faults can be detected by the measurement and evaluation of current value in therespective current branches.This circuit also ensures that the differential current (difference of *IREF*1 and *IREF*2) will flow out to the circuit's output.This approach can test the resistor ladder in total eight steps, by shifting the logic 1 from MBS to LSB. This is implemented as follows,

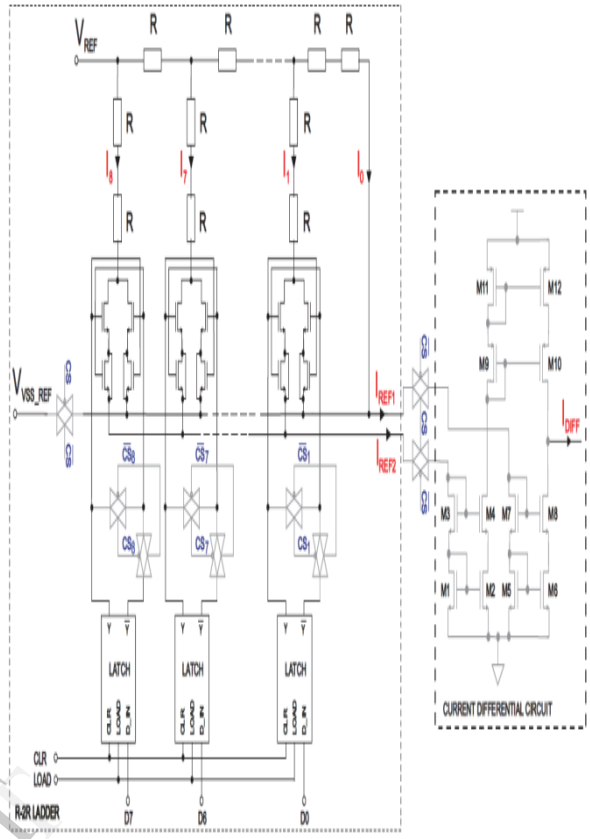

Fig.6. Circuit diagram of R-2R ladder with additional test behaviour (without control logic)

The main problem of this method is that current in the last branch is in order of nA, which is difficult to sense and measure with necessary precision. Therefore, this test technique might be limited to ladders that use resistors with the resistance value smaller than 10kΩ.Two different parametric test methods have been used for on-chip fault detection in the R-2R ladder digital-to-analog converter.

So, an experimental circuit, consisting of the DAC, the additional test hardware, and the control logic for switching the DAC between functional and test modes, has been designed in selected CMOS technology.The on-chip total fault coverage might be increased by measuring the amplitude of oscillation.

III. ADVANTAGES OF BIST OVER CONVENTIONAL TESTING

The automated test equipment (ATE) required for the conventional factory test of VLSI circuits usually includes highly specific test hardware and probing solutions.Most often this expensive equipment can only be used for one specific product and a reuse for higher level tests or during other test phases than factory test is not possible.As opposed to that, BIST-logic designed for a specific VLSI circuit can be extremely helpful for other test purposes like maintenance and diagnosis or start-up test.

Table 1.Comparison of generic BIST techniques for converters

Approach	Specification	Application	Pro	Con	Section
Histogram BIST	Offset error Gain error DNL INL (noise)	ADC Typically low resolution, high-speed ViC	Various stimuli Conventional technique	Area overhead Test time (Time/area trade-off) TSG missing Measurement accuracy Lack of dynamic performance parameter tests	3.1
DOT *OBIST*	DOT	Oscillation ViC	Vector free Area overhead	Lack of correlation to performance parameters	3.2.1 3.2.3
Functional OBIST	Conversion time Gain error DNL, INL	Low to medium resolution ADC ViC	Vector free Area overhead	Lack of dynamic performance parameter tests	3.2.2
MADBIST	SNR Gain tracking Harmonic distortion Frequency response Inter modulation distortion	ADC DAC DSP required	Full BIST	Area overhead	3.3.1
BIST for CODEC	Gain error Inter modulation distortion, Distortion, crosstalk	ADC DAC DSP required	Full BIST	Verification of BIST hardware Fault masking, or external DAC;	3.3.2
BIST for ΣΔ converter	SNR	ΣΔ ADCs DSP required	Dynamic performance test	Area overhead Limited test set	3.3.3
adcBIST™	Offset error Gain error 2nd & 3rd harmonics	ADC/DAC ViC	Digital only; Area overhead; Commercialised	No DNL or INL External DAC Potential test escapes	3.4.1
AUBIST	DOT	Differential ViC	Universal; Internal nodes; On-line	No specifications	3.4.2
Reconfiguration BIST	DOT	Identical cells ViC	Area overhead	No specifications No TSG	3.4.3
HBIST	DOT	Generic	Full BIST	Difficult ORA No correlation to performance parameters	3.4.4

Table 2.Advantages of BIST over conventional testing

	Conventional Test	BIST
probing	difficult	simple
testability	very low	high
cost of test equipment	high	few % area overhead
technology	may be critical	identical to CUT
test speed	problematic	„at-speed testing“
test time	often very high	low
total test cost	high	moderate
applicability	specific	reusable
automatic generation	stimuli only	complete

IV. RESULTS

Method used	Output
• Built-in Self-Test (BIST) scheme for Operational Amplifier (OpAmp)	Fault coverage of 98%
• The Circuit Under Test (CUT)	Fault coverage of 94.21%
• Defect-oriented test methodology for mixed analog-digital circuits	Fault coverage 93%
	Fault coverage to 99% for application of DFT
• Built-in self-test (BIST) for external support for testing	Linearity errors are detected in different situations

V. CONCLUSION

Built-in Self-Test (BIST) scheme is better than other techniques, but for DFT applications Defect-oriented test methodology gives batter approach.

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