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Analysis on a Symmetrical Three Phase Nine Level Inverter with Reduced Switches

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***Abstract*— In this paper presents symmetrical nine level cascaded multilevel inverter with reduction of switching component for various pulse width modulation technique and various references waveform. In conventional CHB inverters required high number of switching components, it appear to more complex control circuitry and bulky. The Proposed cascaded multilevel inverter output voltage level rising by using less number of switches driven by the multicarrier modulation techniques. This paper presents generalized structure, Operation, comparison with other conventional topology, Simulation results with MATLAB/SIMULINK and experimental results.**

Keywords—CHB,Symmetrical inverter,MATLAB/SIMULINK Software.

I. INTRODUCTION

Multi Level Inverter (MLI) offers a number of advantages when compared to the conventional multilevel inverter. The stepped approximation of the sinusoidal output waveform with higher levels reduces the THD harmonic distortion of the output waveform and the stresses across the semiconductor devices and also allows higher current/voltage and power ratings. The depreciates switching frequency of each individual switch of the inverter also decreased the switching losses and improves the efficiency of the inverter. Rathore et al. (2015) to propose a new optimal pulse width modulation strategy for a cascaded seven-level inverter such that maximum switching frequency is limited to rated fundamental frequency (50/60 Hz) and all power devices operate at identical switching frequency. Ruderman et al. (2015) simple smooth hyperbolic voltage THD above and below bound approximations for single phase and three phase inverters with nearest synchronous switching. Haw et al. (2015) the proposed algorithm increases the transient performance of the closed-loop system with only proportional controller and reduces the STATCOM reactive current ripples. Mokhberdoran et al. (2014) the proposed cascaded multilevel inverter has been examine in both symmetric and asymmetric operation modes. A great perfection in voltage levels with less number of switching devices has been obtained in both symmetric and asymmetric modes. Ajami et al. (2014) the proposed multilevel inverter results in reduction of switches devices, relevant gate driver circuits and also the installation area and inverter cost. Chattopadhyay et al. (2014) the concept has the capability of self-balancing during negative and positive cycles without any closed-loop control/algorithm, and it does not consume any power. Filho et al. (2013) this technique uses genetic algorithms to obtain switching angles offline for dissimilar dc source values. Belkamel et al. (2013) the selected inverter DC voltage sources, high-frequency PWM control methods can be effectively applied without loss of modularity. Low-frequency and sinusoidal PWM strategy were successfully applied. Farokhnia et al. (2012) the proposed inverter in reducing THD, when it is compared with the case of a multilevel inverter with constant DC sources. Kangarlu et al. (2012) to operate with high voltage and power, improved output waveform quality and flexibility which make them attractive and more popular. Farokhnia et al. (2011) an analytical algebraic technique based on formulating the line voltage THD of multilevel inverters with unequal dc sources is presented. Mekhilef et al. (2011) the high-voltage stage is made of a three-phase conventional multilevel inverter to reduce the cost and losses. The medium-voltage and low-voltage stages are made of three-level inverters constructed using cascaded H-bridge inverter. Hinago et al. (2010) proposed topology produces output maximum numbers of voltage levels in the same number of switching devices by using this conversion. The number of gate driving circuit is reduced, which leads to reduction of the size and power consumption in the driving circuits. The THD of the output waveform is also reduced.

II. PROPOSED TOPOLOGY

The main drawbacks of the conventional cascaded multilevel inverter is that when the voltage level increases, the number of switches increases and also the dc source required increases. In order to conquer this introduced a new topology of cascaded multilevel inverter. The advantage of this topology is that the number of switches required is reduced and also the number of dc sources. Figure 1 shows the new cascaded nine levels H-bridge multilevel inverter. The following output voltage levels required to generate nine

level voltage $+V_{dc}$,$+2_{Vdc}$, $+3V_{dc}$,$+4V_{dc}$ 0,$-V_{dc}$,$-2V_{dc}$,$-3V_{dc}$,$-4V_{dc}$.For $+V_{dc}$ the S1, S2, S4, S5 switches are ON. For +2vdc the S1, S2, S5, S7switches are ON. For $+3V_{dc}$ the S1, S2, S5, S6 switches are ON. For $+4V_{dc}$ the S1, S2 switches are ON. For $0V_{dc}$ the S1, S3 switches are ON. For $–V_{dc}$ the S3, S6, S7 switches are ON. For $-2V_{dc}$ the S3, S4, S6 switches are on. For $-3V_{dc}$ the S3, S4, S7 switches are ON. For $-4V_{dc}$ the S3, S4, S5, S6, S7 switches are ON. The switching combinations are shown in table 1.

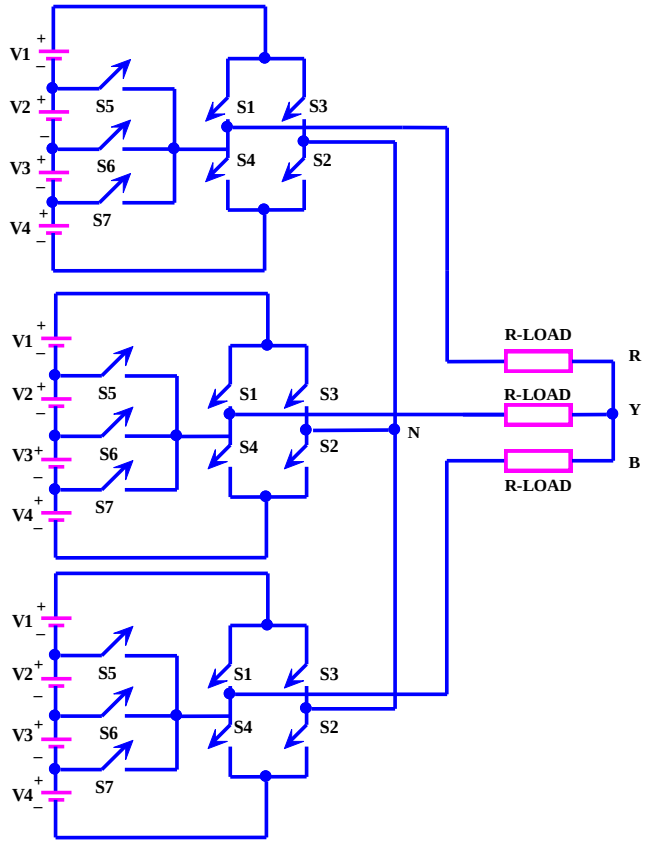

Fig. 1. Proposed Nine level inverter.

TABLE I. SWITCHING TABLE FOR PROPOSED NINE LEVEL INVERTER

S_1	S_2	S_3	S_4	S_5	S_6	S_7	OUTPUT VOLTAGE
1	1	0	0	0	0	0	$4V_{dc}$
1	1	0	0	1	1	0	$3V_{dc}$
1	1	0	0	1	0	1	$2V_{dc}$
1	1	0	1	1	0	0	V_{dc}
1	0	1	0	0	0	0	0
0	0	1	0	0	1	1	$-V_{dc}$
0	0	1	1	0	1	0	$-2V_{dc}$
0	0	1	1	0	0	1	$-3V_{dc}$
0	0	1	1	1	1	1	$-4V_{dc}$

III. PWM TECHNIQUES

Development of this PWM technique used to reduce the THD of the output. Increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics due to moved away the switching frequency carrier harmonics and sideband harmonics from the fundamental frequency component. The reference/modulating wave of multilevel carrier based PWM strategies can be sinusoidal PWM signal. The reference wave is concerned for CFD including amplitude, frequency and phase angle of the reference wave. The following techniques are employed in this study.

A. Variable Amplitude Phase Disposition (VAPD) PWM Strategy

In this strategy all the carriers have the same frequency and the adjustable amplitude (different or unequal amplitudes). All the carriers selected above and below zero reference line are in same phase. Carrier and reference wave arrangements are as shown in Fig. 2

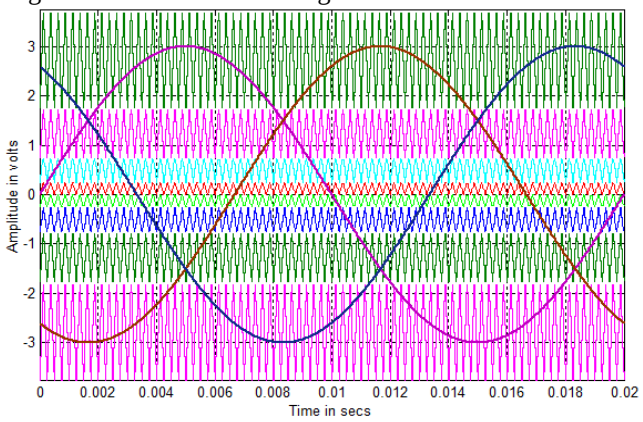

Fig. 2. Carrier arrangements for VAPDPWM

B. Variable Amplitude Phase Opposition & Disposition (VAPOD) PWM Strategy

In this strategy all the carriers have the same frequency and the adjustable amplitude (different or unequal amplitudes). But all the carriers selected above the zero value reference are in phase among them but in opposition (180 degrees phase shifted) with those below. Carrier and reference wave arrangements are as shown in Fig 3.

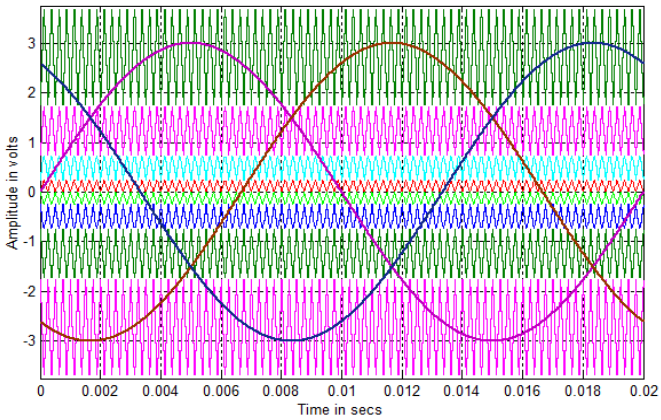

Fig. 3. Carrier arrangements for VAPODPWM

C. Variable Amplitude Alternative Phase Opposition & Disposition (VAAPOD) PWM Strategy

In this strategy all the carriers have the same frequency and the adjustable amplitude (different or unequal amplitudes). All the carriers are alternate in position which is shown in Fig. 4(D). There is phase shift of 1800 between adjacent carriers. Reference and carrier wave arrangements are as shown in Fig. 4.

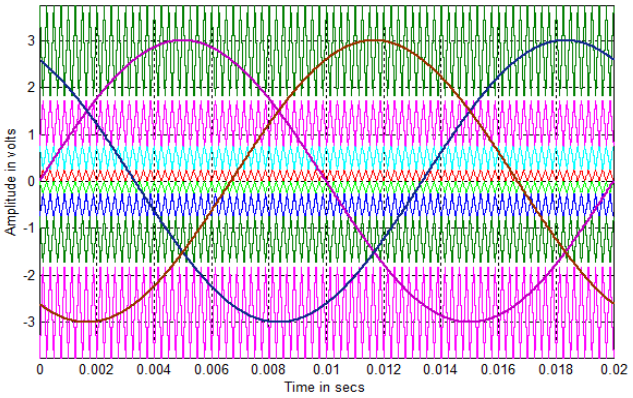

Fig. 4. Carrier arrangements for VAAPODPWM

D. Variable Amplitude Variable Frequency (VAVF) PWM Strategy

The number of switches for above and below devices of chosen MLI is much more than the intermediate switches in SPWM using constant frequency carriers. In order to equalize the number of switches for all the switches, variable frequency PWM technique is used as illustrated in which the carrier frequency of the intermediate switches is properly enhance to balance the numbers of switching for all the switches Fig. 5.

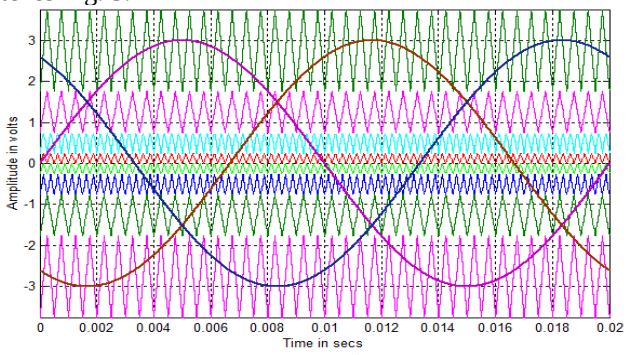

Fig. 5. Carrier arrangements for VAVFPWM

IV. Simulation Results

Simulation of proposed three phase nine-level symmetrical inverter with R load is carried out by MATLAB/ SIMULINK. Switching signals for Cascaded Multi Level Inverter (CMLI) are developed using PWM techniques are used for the references. The simulation is performed for different modulation indices (ma=0.6-1) and for all the PWM techniques. The corresponding % THD values and V_{RMS} of fundamental and peak amplitude voltage V_{PEAK} of inverter output for same modulation indices corresponding of FFT plots and they are shown in tables 2-7.Figures shows the simulated output waveforms for the phase voltage for a CMLI and corresponding FFT plots for sinusoidal reference chosen the one sample value of m_a = 0.8.Tables 2 – 7 obtain the performance measures such as %THD, V_{RMS} and V_{PEAK}. Figures 6 – 21 shows the three-phase output voltage (phase voltage) waveforms for sinusoidal references and its respective FFT plots. The following parameter values are used for simulation: V_{dc} = 100V and R=100 ohms, f_c =2000 Hz and f_m = 50Hz.

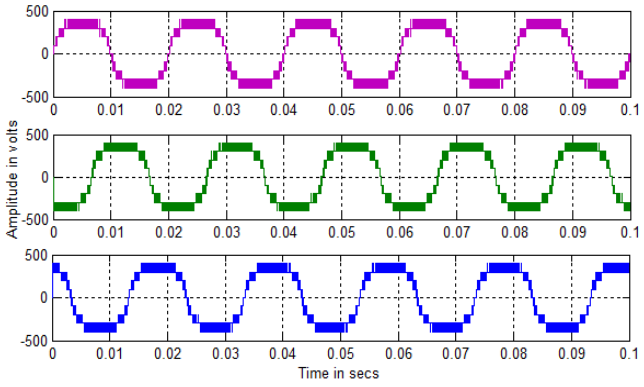

Fig. 6. Three-phase output waveform for phase voltage V_P of VAPDPWM technique

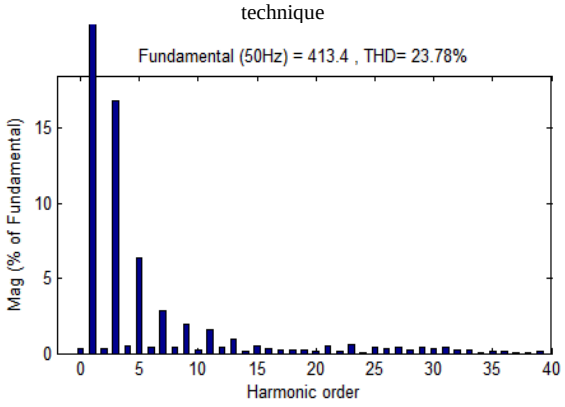

Fig. 7. FFT plot for phase voltage of VAPDPWM technique.

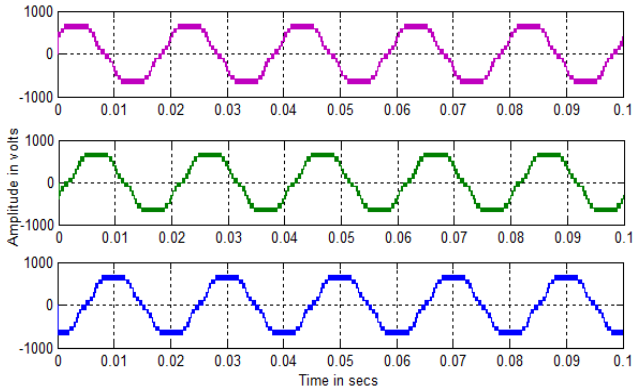

Fig. 8. Three-phase output waveform for line voltage V_L of VAPDPWM technique

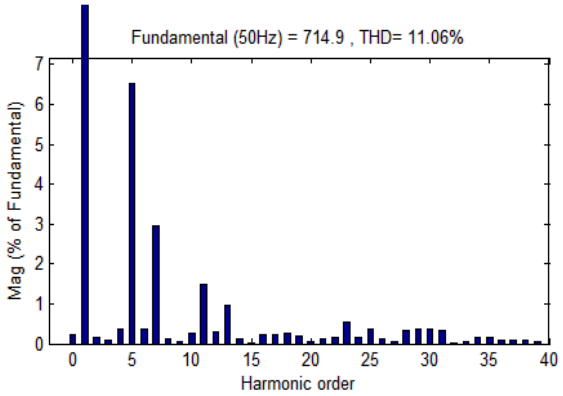

Fig. 9. FFT plot for line voltage of VAPDPWM technique

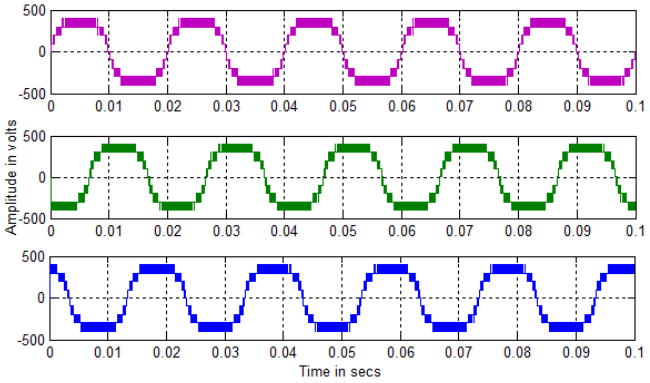

Fig. 10. Three-phase output waveform for phase voltage V_P of VAPODPWM technique

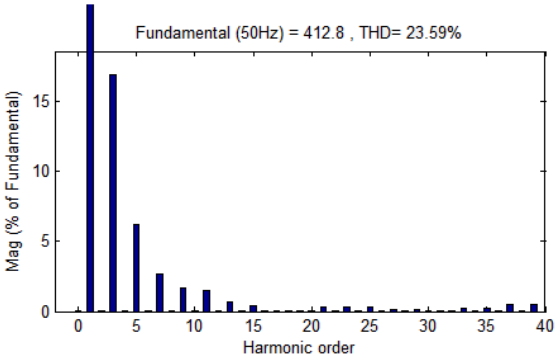

Fig. 11. FFT plot for phase voltage of VAPODPWM technique

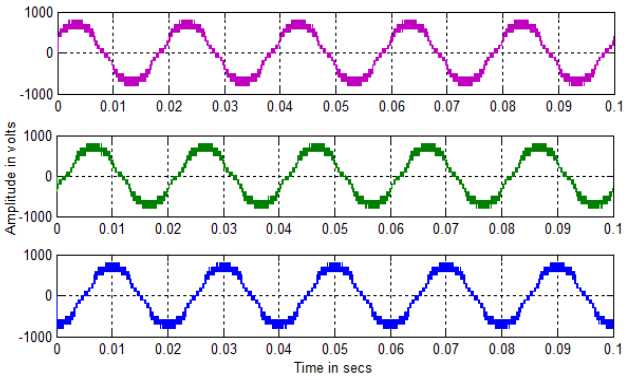

Fig. 12. Three-phase output waveform for line voltage V_L of VAPODPWM technique

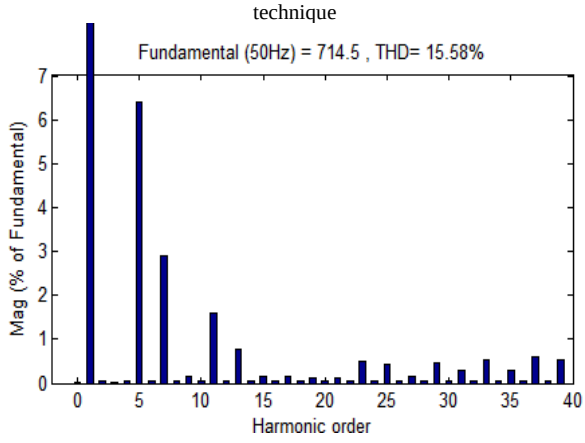

Fig. 13. FFT plot for line voltage of VAPODPWM technique

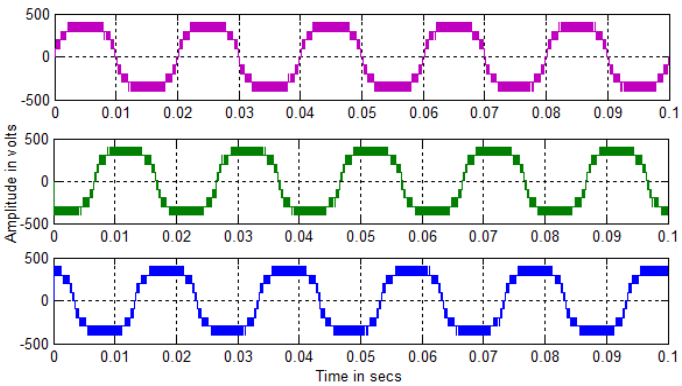

Fig. 14. Three-phase output waveform for phase voltage V_P of VAAPODPWM technique

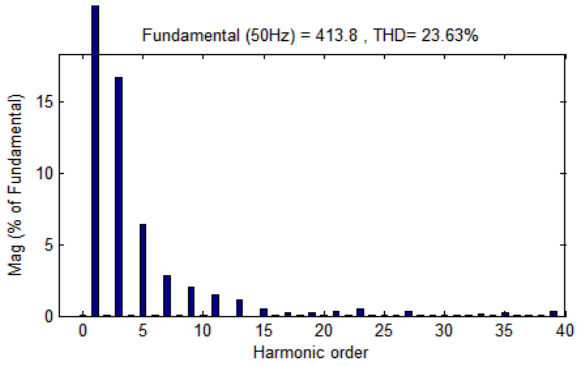

Fig. 15. FFT plot for phase voltage of VAAPODPWM technique

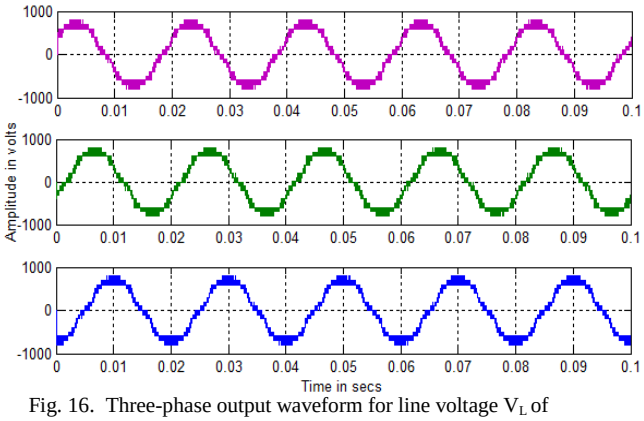

Fig. 16. Three-phase output waveform for line voltage V_L of VAAPODPWM technique

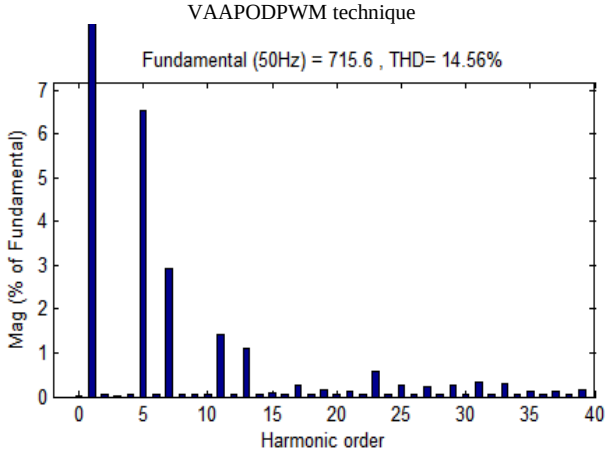

Fig. 17. FFT plot for line voltage of VAAPODPWM technique

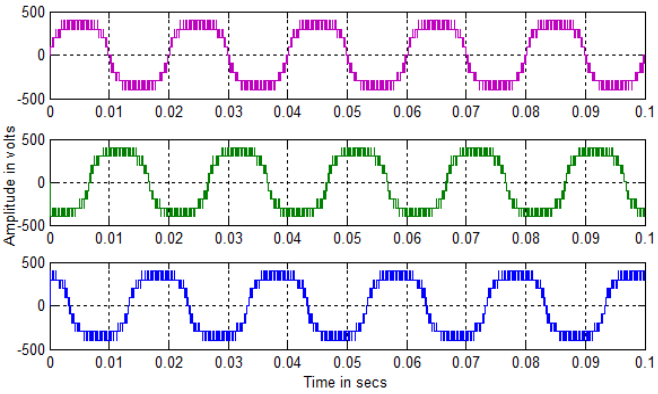

Fig. 18. Three-phase output waveform for phase voltage V_P of VAVFPWM technique

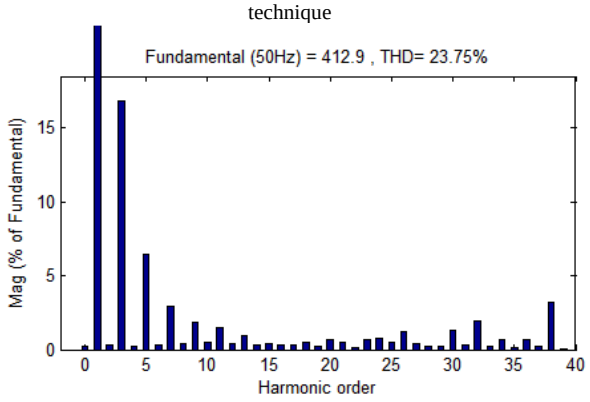

Fig. 19. FFT plot for phase voltage of VAVFPWM technique

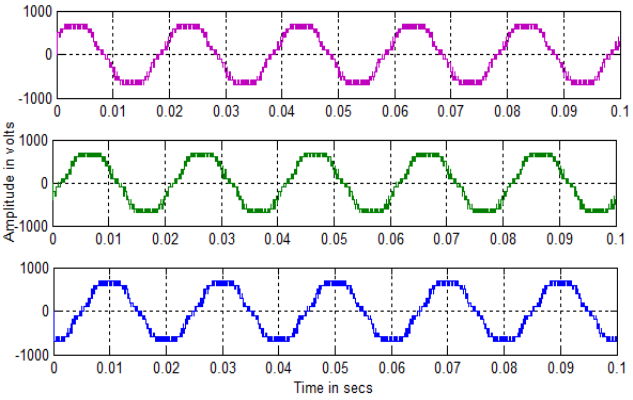

Fig. 20. Three-phase output waveform for line voltage V_L of VAVFPWM technique

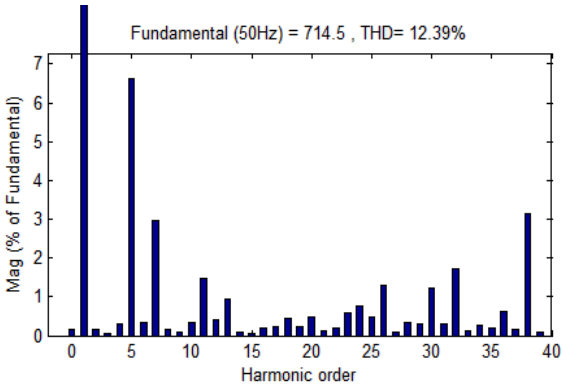

Fig. 21. FFT plot for line voltage of VAVFPWM technique

TABLE II. % THD FOR DIFFERENT MODULATION INDICES WITH PHASE VOLTAGE

m_a	VAPD	VAPOD	VAAPOD	VAVF
1	22.41	22.22	22.36	22.57
0.9	23.49	23.36	23.47	23.42
0.8	23.78	23.59	23.63	23.75
0.7	23.31	23.13	23.26	23.36
0.6	22.04	22.05	21.90	22.10

TABLE III. V_{RMS} FOR DIFFERENT MODULATION INDICES WITH PHASE VOLTAGE

m_a	VAPD	VAPOD	VAAPOD	VAVF
1	320.5	321	319.9	320.3
0.9	306.3	306.2	306.4	306.4
0.8	292.3	291.9	292.6	292
0.7	276.5	276.9	276.2	276.5
0.6	260.6	260.8	260.3	260.5

TABLE IV. V_{PEAK} FOR DIFFERENT MODULATION INDICES WITH PHASE VOLTAGE

m_a	VAPD	VAPOD	VAAPOD	VAVF
1	453.3	453.9	452.4	452.9
0.9	433.2	433	433.3	433.3
0.8	413.4	412.8	413.8	412.9
0.7	391	391.6	390.6	391
0.6	368.6	368.8	368.2	368.3

TABLE V. %THD FOR DIFFERENT MODULATION INDICES WITH LINE VOLTAGE

m_a	VAPD	VAPOD	VAAPOD	VAVF
1	11.64	12.92	13.84	12.25
0.9	10.98	14.90	14.64	11.93
0.8	11.06	15.58	14.56	12.39
0.7	11.17	15.56	13.60	12.43
0.6	10.76	14.69	12.64	11.93

TABLE VI. V_{RMS} FOR DIFFERENT MODULATION INDICES WITH LINE VOLTAGE TABLE STYLES

m_a	VAPD	VAPOD	VAAPOD	VAVF
1	555	555.1	554.2	554.6
0.9	530.4	530.3	530.2	530.6
0.8	505.5	505.3	506	505.2
0.7	478.7	479.7	478.6	478.6
0.6	451.2	451.3	451	451

TABLE VII. V_{PEAK} FOR DIFFERENT MODULATION INDICES WITH LINE VOLTAGE

m_a	VAPD	VAPOD	VAAPOD	VAVF
1	785	785.1	783.7	784.4
0.9	750	749.9	749.8	750.4
0.8	714.9	714.5	715.6	714.5
0.7	677	678.4	676.9	676.9
0.6	638	638.2	637.8	637.8

V. CONCLUSIONS

It is observed from Tables 2 and 5 that VAPDPWM methods provide output with relatively low distortion for all the references. VAPOD with sinusoidal references is found to perform better since it provides relatively higher fundamental RMS output voltage (Tables 3 and 6).Table 4 and 7 provide peak value for all modulating indices.

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