# **Analysis of the Single-Phase Split-Source Inverter** by using Different DC-AC Topology

<sup>1</sup>Omkar G. Londhe <sup>2</sup>Mrs. Saba L. Shaikh

<sup>1</sup>M. Tech (Power System) Student, Walchand College of Engineering, Sangli, India. <sup>2</sup> Assistant Professor (Departmet of Electrical Engg.), Walchand College of Engineering, Sangli, India.

Abstract: This paper explores the working of the Single Phase Split-Source Inverter (SSI), using an unconventional onedirectional dc-ac inverter setup. We have used two typical cathode diodes in a single unit in this configuration. The features behind utilizing the three different carrier signals and their differences are discussed with single phase SSI. Also, a novel control strategy, Modified sine pulse width modulation (M- SPWM) technique is introduced. Also this paper discusses the MATLAB model with its simulation results of 1- KVA single phase SSI.

Index terms: Sine pulse width modulation (SPWM), Modified SPWM (M-SPWM), Split-Source Inverter (SSI), Voltage source Inverter (VSI).

#### INTRODUCTION

Single stage inverters have witnessed a widespread adoption over the past decade to substitute standard two stage topology inverters. This architecture has advanced in terms of reducing circuit difficulty and physical size as a way of increasing the performance of overall system. Advantages of this topology are as follows:-1)DC link voltage continuous; 2) continuous dc current input; 3) for higher voltage gains it gives low voltage stresses; (4) passive component count is less; (5) use of only additional input diode (6) for basic operation standard modulation technique used similarly as the VSI; and (7) no additional boosting states are required. Three different carrier signals are discussed which are the triangular, trail-edge and lead-edge saw tooth carriers with the single phase SSI modulation and their characteristics are highlighted. In this configuration, single-phase operation allows to use dual common-cathode diodes in one unit as a replacement of using separate two diodes. This helps to achieve less parasitic inductance in these diodes' commutation direction. Furthermore it results into fewer voltage spikes at the output across the various switches and increasing the overall efficiency of the inverter.

#### WORKING PRINCIPLE AND CONTROL II. **STRATEGY**

The working of split source inverter topology for single phase is as shown in Fig.1 Similar to the three phase topology. Since the conventional 4-switch bridge is used, four switching states are considered to accomplish the process of boosting inside the inversion one. When at least one of the upper leg switch or both switches are ON, i.e.  $S_{xU}$ or S<sub>vU</sub>, the inductor L is charging. Meanwhile, when both the lower switches ON, where inductor discharges and capacitor C charge. This state is called as zero state, where both the switches from lower leg are switched OFF.

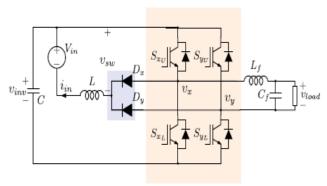


Figure 1: Single-phase SSI configuration in one unit, with two typical common cathode diodes.

Using standard sine pulse width modulation (SPWM) technique the above switching states can be achieved as shown in Fig. 3. Inductor L charges when carrier signal is higher than the envelop specified by max(v\*x, v\*y). If the carrier signal is lower than the envelope specified by max(v\*x, v\*y), inductor L discharges into C through antiparallel diodes of the lower leg. Because the envelope specified by max(v\*x, v\*y) oscillates continuously, this results in charging and discharging of inductor L with oscillating duty cycle. Therefore, there is an increase in the low frequencies at the dc-side voltage and current. Also, it increases the voltage stress across the switches.

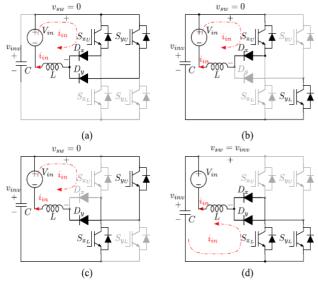


Figure 2: Four switching states by using SPWM technique: a)'11' 'Zero State' b)'10' 'Active State' c)'01' 'Active State' d)'00' 'Zero State'.

ISSN: 2278-0181

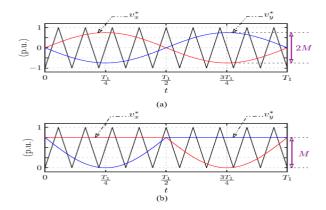


Figure 3: (a) SPW modulation technique; (b) M-SPW modulation technique.

Thus, we implement Modified SPWM (M-SPWM) technique which has a constant charge and discharge period of inductor L and by setting minimum reference signal value at the minimum carrier signal value it gives lower voltage stresses.

# III. MODULATION USING DIFFERENT CARRIER SIGNALS

As shown in Fig. 2 and 4(a) for single phase SSI, diode  $D_x$  is always conductive and  $D_y$  commutes at various values of current for half fundamental period. This can be demonstrated during a single switching process with three separate states as below.

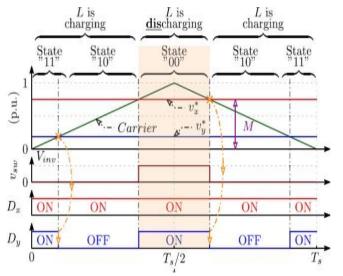


Figure 4: (a) The modified SPWM (M-SPWM) scheme using the triangular carrier for one switching cycle.

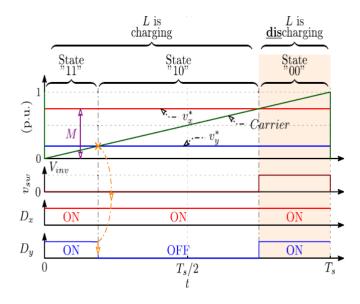


Figure 4: (b) The modified SPWM (M-SPWM) scheme using the trailedge saw tooth carrier for one cycle of switching.

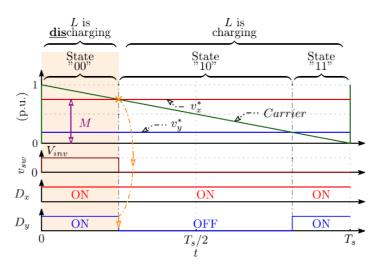


Figure 4: (c) The modified SPWM (M-SPWM) scheme using the lead -edge saw tooth carrier for one cycle of switching.

The first OFF turn depends on the lower envelope intersection point defined by min(v\*x, v\*y) with the carrier signal, which occurs with different current values during the charging process. Meanwhile the second turning OFF happens at the end of the discharge process with a constant current value equal to half the actual minimum value of the inductor, Because it also depends on the intersection point of the upper constant envelope min(v\*x, v\*y) identified by the carrier signal. In addition, additional conductive losses occur in other switches because of reverse recovery current. It is worth noting that this commuting current in the diodes corresponds with the commuting current in the switches. Reducing this current effect would help minimize switching losses. The figure 4(c) shows that in each switching cycle D<sub>y</sub> turns OFF once. Hence, saw tooth carrier reduces the number of commutation by half compared with

Vol. 9 Issue 07, July-2020

triangular carrier signal. Comparing Fig 4(b) and (c), when we use leading-edge saw tooth carrier, as the input current reaches the lowest value lowest possible turning OFF current of the commutation diode (D<sub>v</sub>) results.

Hence, the following features exists as we use the saw tooth carrier:1) Commutation numbers are reduced to half 2) The lead-edge saw tooth carrier helps to achieve minimum possible commutation current; and 3) Since the differential output is not same, the need requirement for output filter is greater Therefore, saw tooth carrier switching frequency should be doubled to maintain a constant differential output voltage for the final part, and similar output filters should be used. Finally, due to commutation of diodes at lowest possible value of current there is slight increase in the efficiency of the inverter when lead-edge saw tooth carrier is used.

## IV. SIMULATIONS AND EXPERIMENTAL RESULTS **MATLAB Simulated Power Circuit Diagram**

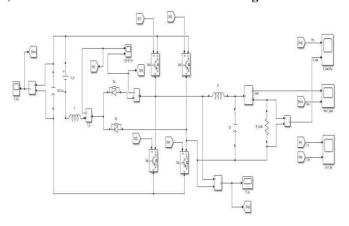


Figure 5: (a) MATLAB Simulation of Power circuit diagram for single phase split-source inverter.

### **MATLAB Simulated Control circuit Diagram**

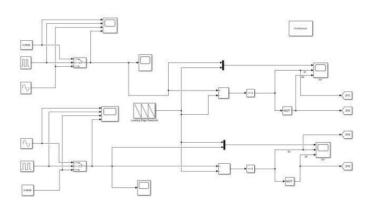


Figure 5: (b) MATLAB Simulation of Control circuit diagram for Single Phase Split -source Inverter.

#### Specification and Designed Parameters of Single c) phase SSI

Table 1 Specification and Design Parameters

<b>(V</b> )	(A)	<b>(V)</b>	(A)	(Hz)	(Hz)	<b>(V)</b>	M (p.u)	L (mH)	C (mf)
80	12.5	110	11	50	50	235.6	0.6604	0.3	2
120	8.3					275.8	0.5649		

#### Results:

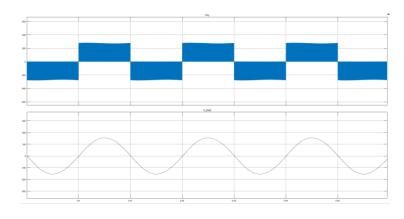


Figure 6(a) Simulation results using lead-edge sawtooth carrier for Vin = 120 V. (1) Output voltage (Vxy) (2) Voltage across load (V<sub>Load</sub>).

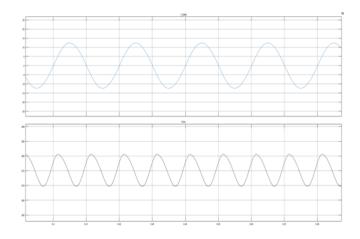


Figure 6(b): (3) Current across Load (I\_Load), (4) Voltage across DC-Link Capacitor (V\_inv)

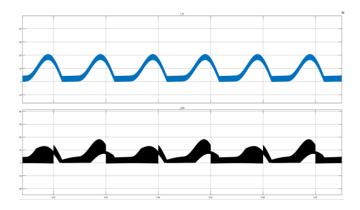


Figure 6(c) : (5) Current across Inductor ( $I_{in}$ ), (6) Current across Diode ( $D_x$ ) - ( $I_{in}$ )

#### V. CONCLUSION

Considering the unidirectional dc – ac operation, the operation of the SSIs in this paper was analyzed for single phase application, using an unconventional topology, in which a dual-diode common-cathode kit could be used instead of two separate diodes to mitigate the voltage spikes in the output voltage of different switches. Among the three different carrier signals the lead-edge sawtooth carrier signal achieves the lowest current value possible for one commutation per cycle of the input diodes, which is equal to half of the minimum input current. Also to maintain similar differential output switching frequency is doubled which helps to use similar filter requirements

#### VI. REFERENCES

- Fang Zheng Peng, "Z-Source Inverter", IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, VOL. 39, NO. 2, MARCH/APRIL 2003.
- [2] O. Ellabban and H. Abu-Rub, "Z-source inverter: Topology improvements review," IEEE Ind. Electron. Mag., vol. 10, no. 1, pp. 6– 24, Mar. 2016.
- [3] H. Ribeiro, A. Pinto, and B. Borges, "Single-stage dc-ac converter forphotovoltaic systems," in Proc. IEEE Energy Convers. Congr. Expo., Sep. 2010, pp. 604–610.
- [4] M. K. Nguyen, Y. C. Lim, and S. J. Park, "A comparison between single phase quasi-Z-source and quasi-switched boost inverters," IEEE Trans. Ind. Electron., vol. 62, no. 10, pp. 6336–6344, Oct. 2015.
- [5] H. Ribeiro, A. Pinto, and B. Borges, "Single-stage dc-ac converter for photovoltaic systems," in Proc. IEEE Energy Convers. Congr. Expo., Sep. 2010, pp. 604–610.
- [6] S. S. Lee and Y. E. Heng, "Improved single phase split- source inverter withhybrid quasi-sinusoidal and constant PWM," IEEE Trans. Ind. Electron., vol. 64, no. 3, pp. 2024–2031, Mar. 2017.
- [7] A. Abdelhakim, P. Mattavelli, and G. Spiazzi, "Three-phase split-sourceinverter (SSI): Analysis and modulation," IEEE Trans. Power Electron.,vol. 31, no. 11, pp. 7451–7461, Nov. 2016.
- [8] A. Abdelhakim, P. Mattavelli, and G. Spiazzi, "Three- phase three-levelflying capacitors split-source inverters: Analysis and modulation," IEEETrans. Ind. Electron., vol. 64, no. 6, pp. 4571–4580, Jun. 2017.
- [9] A. Abdelhakim, P.Mattavelli, and G. Spiazzi, "Three-level operation of thesplit-source inverter using the flying capacitors topology," in Proc. 8th Int.Power Electron. Motion Control Conf., May 2016, pp. 223–228.
- [10] A. Abdelhakim and P. Mattavelli, "Analysis of the three-level diodeclampedsplit-source inverter," in Proc. 42nd Annu. Conf. IEEE Ind.Electron. Soc., Nov. 2016, pp. 3259–3264.