Analysis of Techniques used in Error Detection and Correction Code for Multiple-Bit-Cell Upset

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***Abstract*— In the radiation environment, there may be a single bit upset (SBU) or multiple cell upsets (MCU) can occur during the transmission process. The different error detection and correction codes are widely used to protect the memory cells and to achieve the high level of reliability. The existing decimal matrix code technique is used to detect and correct the error and it utilizes more redundant bits for memory protection. In this paper the analysis of technique is performed to detect and correct the error and to maintain the high memory reliability with less redundant bits in the presence of multiple-bit-cell-upsets (MBCUS).**

Keywords—Error detection and correction codes, memory, multiple cell upsets (MCU), single bit upset (SBU).

I. INTRODUCTION

Memory reliability is the important role in radiation environment. In the reliable communication, error detection and correction is must. The information bits that are generated during the data communication processes are in the form of binary symbols. The circuit encoder in the transmitter accepts the message bits and adds the redundancy (extra) bits according to a prescribed rule and hence an encoder data at higher bit rate can be produced. The circuit decoder in the receiver exploits the redundancy to decide which message bits were actually transmitted. In the transmitter part, the redundant bits are added and removed by the receiver part. The combined goal of the encoder and decoder circuit is to minimize the effect of circuit error. In essence, the number of errors between the encoder circuit input (derived from the source) and the decoder circuit output (delivered to the user) is minimized. The encoders and decoders are mainly used in data transmission process. The original data is transmitted from encoder to decoder and there may be an error occurred in transmission process. Many types of error can be occurred, they are:

- Single-bit error
- Burst error

Single bit error means a 0 changed to 1 or a 1 to 0. This kind of bit changes in the data unit referred as single bit upsets. The term burst error expresses, if two or more bits in the data unit have changed from 1 to 0 or from 0 to 1. Multiple cells that are changed in the data unit named as multiple cell upsets (MCUs).

II. RELATED WORK

In CMOS technology, as the size of devices decreases, the soft errors in the memory cells increases. Especially in the space environment, where ionizing effects of atmospheric neutron, alpha particles and cosmic rays [1]. Single bit upsets and multiple cell upsets are the trending major issues which affect the memory reliability. The single bit upset can be defined when only one bit is flipped in the memory cell and multiple cell upset can be defined when multiple bits are flipped in the same memory cell [2].

In the Reed Muller code, decoding technique is used to improve the performance, power saving and to reduce area. In the memory cells, the soft errors are protected by using protection code. The error correction codes (ECCs) are widely used to protect the memory [3-5]. The ECCs techniques are Punctured difference set codes, Reed-Solomon codes and Bose-Chaudhuri-Hocquenghem codes and so on. The drawbacks of those codes are, they have more area, power consumption and delays. Also the circuit diagram is more complex [6-8].

Matrix-Based Codes for adjacent error correction method is developed to provide protection against errors in adjacent bits in memories. This technique improves memory reliability for clustered MCUs. By determining the locality of error, this technique provides the better protection level and reduced cost. Another way to protect memory is by using Built In Current Sensors (BICS). These sensors are placed in the columns of the memory block and it detects the unexpected current variation on the memory.

By this they can able to detect the occurrences of error. The disadvantage of this technique is that, it can correct multiple errors only when they are in adjacent manner [9]. In order to detect and to correct the error, the redundancy bits are used. In Decimal Matrix Code technique, the number of redundancy bits is 36 and obviously which are more than the original data. Hence, there is an increasing area and power utilization [10]. In parity matrix code technique required 26 redundant bits [11].

III. EXISTING METHODOLOGY

A. Decimal Matrix Code

The error detection and correction process are done in the decimal matrix code technique. In this technique, the encoder and decoder circuits are used to detect and correct the error in the memory cell. Here the information bit Din is taken as 32

bit and transmitted to the encoder. In encoder part, the divide-symbol idea is used, which means the 32 bit word, is divided into 8 symbols of 4bits and these symbols are arranged in matrix format. Here the 2D matrix is used to arrange the 8 symbol in the form of 2×4 and to calculate the horizontal redundant bits (H) and vertical redundant bits (V).

The encoder output is stored in the memory. During the transmission process from encoder to memory, the error may occur. This memory output is indicated as D' and again calculate the horizontal redundant bits (H') and vertical redundant bits (V'). In the memory part, error may be a single-bit upset (or) multiple cell upsets and this error can be corrected at decoder part which consists of:

(i) Syndrome calculator

(ii) Error locator

(iii) Error corrector

The operation of Syndrome calculator is that the redundant bits must be recomputed from the received information bits and compared to the original set of redundant bits. The difference is named as syndrome bits. If the syndrome bits are equal to zero, then there is no error occurred in this process. If the syndrome bits are equal to one, it represents that error is occurred and hence error location is to be found and to be corrected.

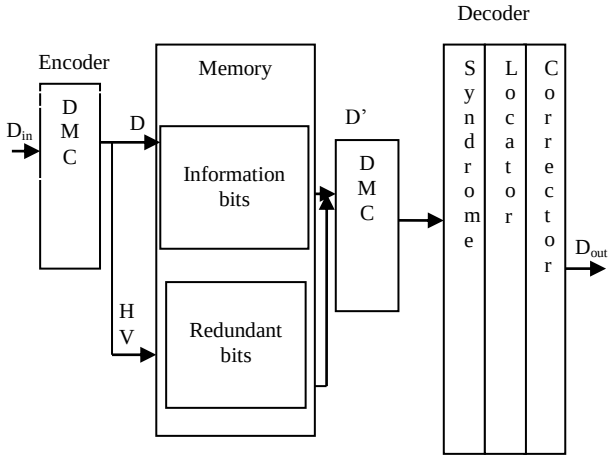


Fig.1. DMC Block

Depending on the memory output the error can be identified and solved at the decoder part. The memory output consists of two cases.

(i) Without error bit in memory, which means there is no error in the memory and the original bit is obtained at output.

(ii) With error bit in memory, which means error occurred in memory and corrected at the output side.

These are explained in following case.

Case 1: Error Corrector (Without Error Bit In Memory)

Let the horizontal redundant bits are H and H' which are calculated by using information bit D and D'. Here horizontal redundant bits are 20 and it is divided into 5bits. The normal XOR operation is performed to get syndrome value.

i.e., H = 00011 | 00000 | 01111 | 10000

H' = 00011 | 00000 | 01111 | 10000

Syn bit 1 Syn bit 2 Syn bit3 Syn bit 4

Here all the syndrome values are 0, there is no 1's. This implies the memory has no error.

Case 2: Error Corrector (With Error Bit In Memory)

The same process is repeated and to calculate the syndrome bit. If the syndrome value is 1means the error can occur in the memory and corrected by inverting the values of error bits.

In the DMC technique required more area and power compare to other technique. The number of used 4 input LUTs and IOBs are 109 and 96 respectively. The total supply power is 0.054W.

B. Parity Matrix Code

In order to overcome the drawbacks in the DMC, the Parity Matrix Code can be implemented. In this PMC technique, the number of redundancy bit can be reduced to 24 bit. So compared to DMC, the area and power consumption can be minimized. The PMC technique consists of encoder, memory and decoder. In encoder, the 32 bit input is separated into four bits of each 32 bits. Here the four bits are parity check which is multiplied into generator matrix G.

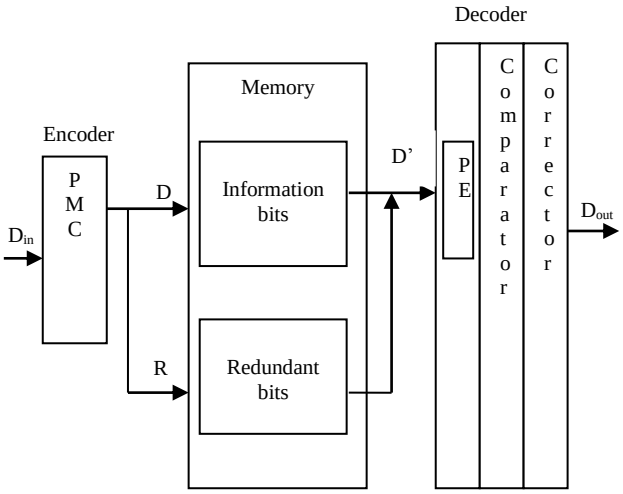


Fig.2. PMC Block

Here the parity bits and data bits are arranged in p1, p2, p3, d1, d2, d3, d4. The each parity bit is represented with a column vector containing a 1 in the row corresponding to each data bit included in the computation and a zero in all other rows. The data bits are arranged in diagonal matrix.

p1= p2= p3=

The generator matrix G is given as

$$G = \left(\begin{array}{ccc|cccc} 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 \end{array}\right) =$$

p1 p2 p3 d1 d2 d3 d4

The parity check bit and generator matrix (P×G) is multiplied to get the redundancy value. Which contain first three bits are redundant bits and remaining bits are parity check bits.

$$\text{PMCenc} = \underbrace{1111}_{\text{Parity check bits}} * \begin{pmatrix} 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 \end{pmatrix}$$

$$= \underbrace{111}_{\text{Redundant bits}}\ 1111$$

When MBCUs occurs during the transmission, in the decoder part, parity equation is used to calculate the redundant bit. The equation is given by,

PMCdec=
p1=d2+d3+d4;
p2=d1+d3+d4;
p3=d1+d2+d4;

p1=1+1+1=1
p2=1+1+1=1
p3=1+1+1=1
} =1111111

If the redundant bits are equal, then there is no error. Otherwise error is occurred and this error can be corrected by flipping the values of error bits. When comparing to DMC, the area and power consumption is minimized in the PMC technique. The number of used 4 input LUTs and IOBs are 96 and 96 respectively. The total supply power is 0.052W.

IV. PROPOSED WORK

In this section, the LRC technique is proposed for error detection and correction with efficient memory reliability and reduced redundant bits. The 32 bits are taken as input and they are organized in a table with row and columns. The detection and correction of an error can be performed by calculating the parity bit for each column in encoder and this parity bit is send along with original data. In decoder, the received bits are processed in same manner and compared with the redundant bits. The bit flip technique is used to correct the error. LRC of n bits can easily detect single and burst error with less redundant bits.

$$\begin{pmatrix} 0 \\ 1 \\ 1 \\ 1 \end{pmatrix} \quad \begin{pmatrix} 1 \\ 0 \\ 1 \\ 1 \end{pmatrix} \quad \begin{pmatrix} 1 \\ 1 \\ 0 \\ 1 \end{pmatrix}$$

These are shown in a block in the Fig.3 and its RTL schematic view is shown in Fig.4.

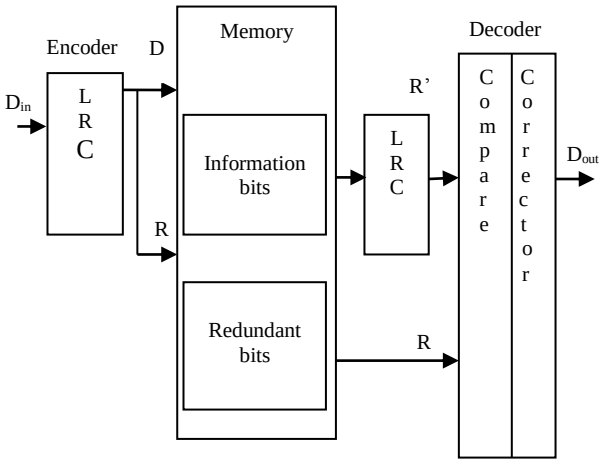


Fig.3. LRC Block

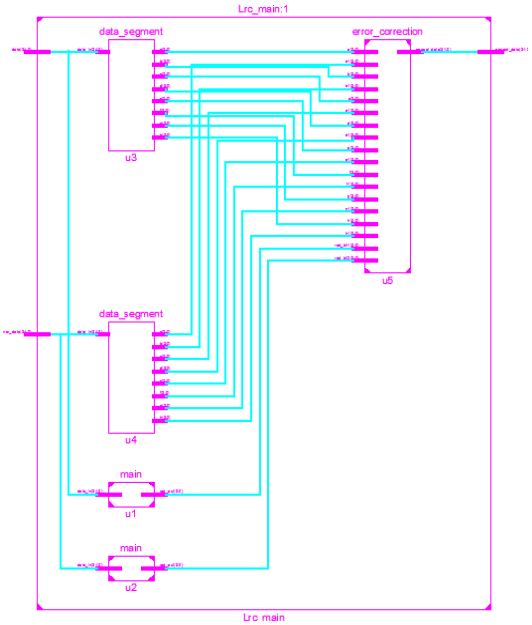


Fig.4. RTL schematic view of LRC

A. Result Analysis

In encoder part, the 32 information bit is segmented into 8 symbols of 4 bits in a table with row and columns. This

segmentation bits are represented by a, b, c, d, e, f, g and h. The XOR operation is performed to calculate the redundant bits. Here the number of redundant bits reduced to 4bits.

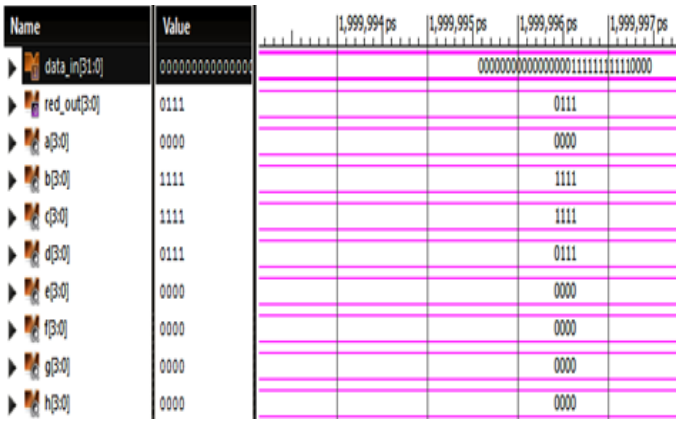


Fig.5. Segmented with calculation of redundant bits

The same information bit D is transmitted to the memory and MBCUs occurs during the transmission process. Again same process is taken to calculate the redundant bits. In decoder part, the both redundant bits are compared. If the redundant bits are equal, then there is no error in the memory. Otherwise error is occurred. The bit flipping technique is used to correct the errors.

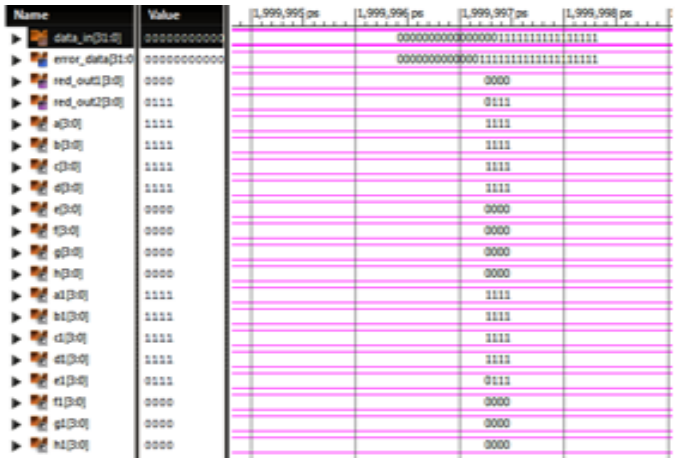


Fig.6. Error detection

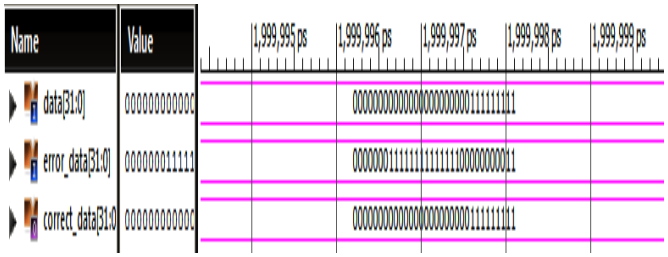
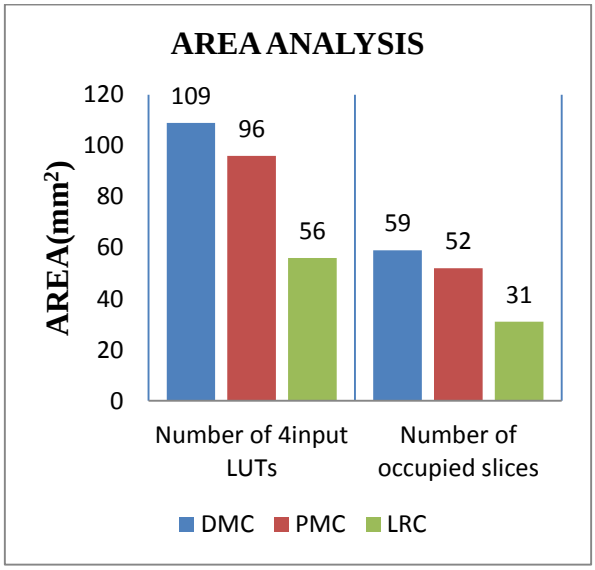
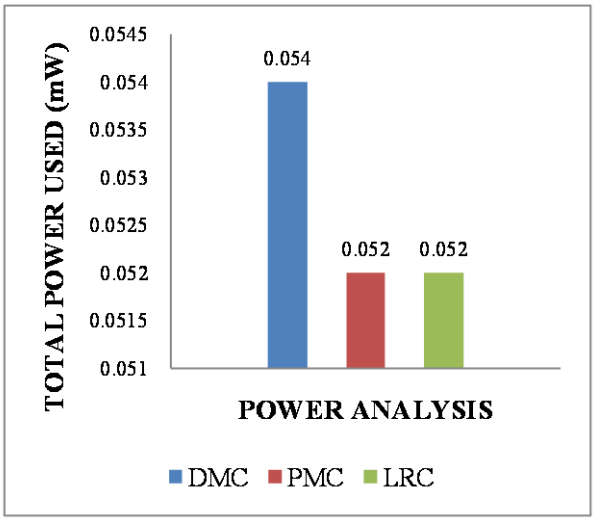


Fig.7. Error correction

When compared to existing method, the LRC technique requires less area and power with reduced redundant bits. The number of 4 input LUTs and IOBs are 56 and 96 respectively. The total supply power is 0.052W. The design can be implemented in VHDL and it's simulated by Xilinx ISE.

B. Analysis of Area and Power





V. CONCLUSION

The analysis of technique is made for detection and correction of the error in the memory with less redundant bits. The techniques analyzed are DMC, PMC and LRC. When compared to the existing methods, the LRC technique provides efficient utilization than other techniques. The memory cells are well protected and high memory reliability is achieved. It is used in memory and telecommunication application. The future work may be proceeded to detect and correct the error for 64 bits and 128 bits and further it may be enhanced to reduce the redundant bits with improved memory reliability.

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