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Analysis of Parallel Connected Three-Phase Inverter for Power Sharing using Droop Control Technique

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Abstract **- This project presents analysis of a two parallel connected three-phase voltage source inverter(VSIs) system each rated at 10 kVA (400 V line-line RMS, 50 Hz), intended to act as a main source in a micro-grid, supplying local loads in islanded modes. The system consists of a three-phase voltage-source inverter fed from a DC source giving 750V, an LCL output filter, and R–L loads (Load 1: 12 kW + 2 kVAR; Load 2: 8 kW + 2 kVAR) , through switchable circuit breakers, and it is designed for a rated three phase AC voltage and power level appropriate for low-voltage micro-grid applications. A droop-based control strategy employs P–f and Q–V droop characteristics to autonomously regulate frequency and terminal voltage magnitude of each inverter based on local power measurements such as active power and reactive power, which enables decentralized power sharing. The parallel connected three-phase VSIs along with droop control technique is implemented in MATLAB/Simulink under different loading and operating modes. Simulation results indicate that the specified inverter system can maintain output voltage around 400V and frequency vary from 49.75Hz to 50.25Hz which is within designed limits, and achieve satisfactory active and reactive power sharing for dynamic load changing. For operating of two parallel VSIs and both loads, the THD of output voltage is obtained as 2.42% and output current THD is around 2.60% which is within the limits of IEEE 519 standards.**

Keywords **- *Micro-grid, Voltage Source Inverters(VSIs), Parallel Operation, Droop Control Technique, Power Sharing, Total Harmonic Distortion.***

I. INTRODUCTION

Traditional electric utilities undergo evolutionary changes as a result of distributed generation (DG), which combines smaller generating systems based on renewable energy resources, such solar and wind power, with loads and energy storage systems. The idea of a micro-grid (MG) is becoming increasingly attractive as an efficient method of integrating renewable energy sources as compared to conventional generators. The MG is often made up of a number of dispersed, networked generators that serve as a fundamental building piece. Due to its flexibility and ability to operate in two fundamental modes—autonomous and grid-connected and hence micro-grids are becoming more and more popular. The majority of distributed generation (DG) systems, including micro-turbines, solar systems, and energy storage systems, need to be connected to the micro-grid via a power electronics (PE) interface in order to have greater operational and control flexibility. However, they also increase the system's susceptibility to network disruptions because of their minimal physical inertia[1].

With the growing integration of distributed generators (DG), the design of the electric grid is changing from a centralised to a decentralised structure. Demarcating a section of the network that can function as an island or in grid-connected mode is the current trend. A micro-grid is the name given to such a network. A micro-grid should be able to generate and store sufficient electrical energy to meet the demands of the islanded mode of operation. The DGs are intended to divide the load according to their ratings when operating in the island mode[2]. In order to increase the redundancy and dependability of power supply systems, the parallel architecture of voltage source inverters (VSIs) enables the connecting of multiple VSI to build a micro-grid, thereby lowering the cost of manufacturing and enabling system growth. Each DG operating in the "autonomous" mode is expected to fulfil the following criteria:1) The micro-grid's steady-state operation should not be impacted by any DG operation mode switching; 2) Each DG should independently control its own frequency and voltage based on local data from the DG itself. Accurate load sharing across several sources in this system requires a well-designed controller[3].

A variety of centralised control methods for micro-grids that rely on external communication links between the inverters have been documented in the literature in recent years. But these controllers create a financial and technological barrier, particularly for remote micro-grids[4]. It is widely agreed that conventional droop control can result in decentralised proportional power sharing[5]. The droop control method is ideal to control several parallel inverters since it eliminates the need for external communication between them. Several droop control systems and combinations exist to effectively share power for linear and nonlinear loads, as documented in literature. Traditional droop control involves active power-frequency (P-f) and reactive power-voltage (Q-V) controls[6].

The article is followed by the block diagram of parallel connected VSI with droop control technique explanation in Section II. Later in Section III the analysis of different types of controller with equations is presented. In Section IV the

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simulations result of the proposed topology is presented and results are obtained for each operating modes, and the followed by the Conclusion of the paper in Section V.

II. PROPOSED TOPOLOGY

A. Parallel Connected VSIs.

The work proposes a decentralized control scheme for two three-phase voltage source inverters, each supplied from an independent DC source and connected to common R–L loads through circuit breakers as shown in fig. 1. In this arrangement, either inverter can feed one or both loads, which provides flexibility in operation and allows the total demand to be shared between the units.

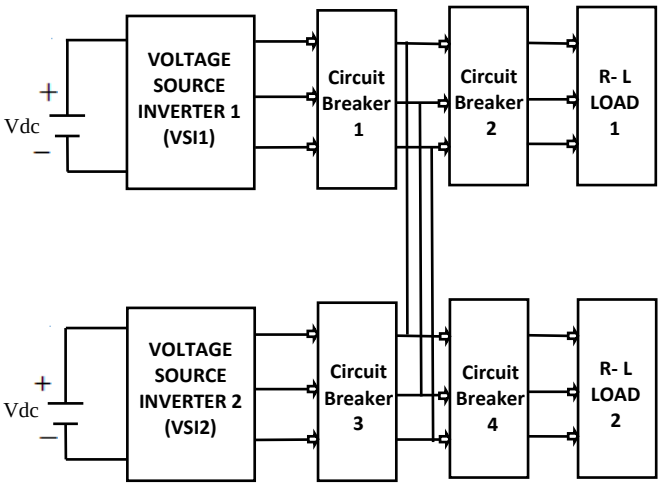

Fig. 1. Block Diagram of Parallel VSIs with R-L loads

Each inverter operates as a grid-forming source whose output voltage magnitude and frequency are adjusted according to its own measured active and reactive power. This behaviour is achieved using active-power–frequency and reactive-power–voltage droop characteristics, which imitate the natural droop of synchronous generators and allow the inverters to share load proportionally without any communication link. The references produced by the droop laws are followed by inner voltage and current controllers, implemented in a rotating reference frame and realized through PWM gating of the inverter switches, so that the two inverters remain synchronized while delivering the required power to the common AC bus and the connected R-L loads.

B. Block Diagram of Droop Controlled Three-Phase VSI.

The fig. 2, shows the Block Diagram of Droop Controlled Three-Phase VSI along with different controllers like voltage, current and droop controller.

The three-phase voltage source inverter transforms steady DC voltage into adjustable AC waveforms using six power switches (S1–S6) controlled by SPWM gating signals. A LCL filter follows the inverter to suppress high-frequency PWM harmonics. Droop control mimics traditional generator regulation through active-power droop (frequency decreases proportionally with power output) and reactive-power droop (voltage magnitude drops with reactive loading), enabling automatic load sharing among parallel inverters without communication.

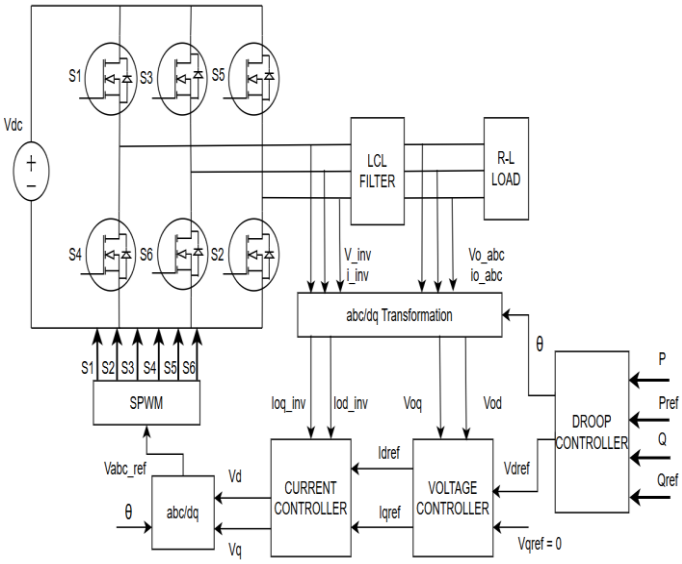

Fig. 2. Block Diagram of Droop Controlled Voltage Source Inverter(VSI)

Nested dq-frame PI regulators form the inner control structure: outer voltage loops track droop-generated amplitude commands to produce current references, while faster inner current loops with cross-coupling compensation ensure precise current following and LCL stability. Final SPWM modulation compares phase-displaced sinusoidal references against a high-frequency triangular carrier, where the modulation ratio (peak sine/carrier amplitude) directly sets AC output voltage while carrier frequency determines harmonic attenuation.

C. Droop control.

The droop control is to choose a frequency droop character curve similar to the traditional generator as the control method of the micro-source, that is, to obtain stable frequency and voltage through P-f droop control and Q-V droop control, respectively. The droop control method controls the active and reactive power outputs of each micro-source in the micro-grid are regulated independently, without requiring communication-based coordination among units, thereby enabling plug-and-play capability of micro-sources. This decentralized operation allows the micro-grid to reliably maintain power balance and frequency synchronization during islanded operation.

The fig. 3, shows the basic droop characteristics used for active and reactive power control. In fig. 3(a), P-f droop control explains that, frequency f is on the vertical axis and active power on the horizontal axis. At no-load, the inverter (or generator) runs at nominal frequency fo. As the active power output increases from 0 to Po and then to P, the operating point moves along the sloping line, so the frequency

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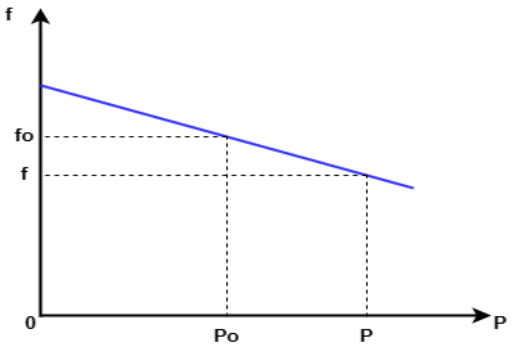
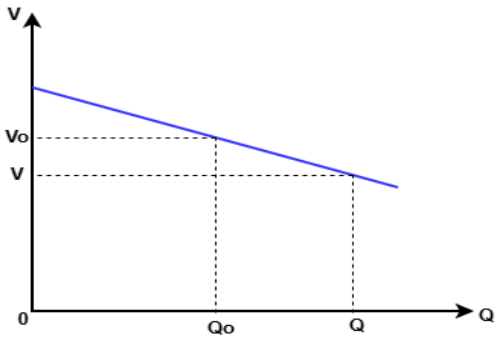
drops from fo down to f. This straight line is the P–f droop: more active power means a slightly lower frequency, which allows several units to share active power automatically.



(a) P-f droop control



(b) Q-V droop control.

Fig. 3. Droop Characteristics (a) P-f droop control, (b) Q-V droop control.

In fig. 3(b), Q-V droop control explains that, voltage magnitude V is on the vertical axis and reactive power Q on the horizontal axis. At zero reactive power, the terminal voltage is at its nominal value Vo. When the inverter supplies more reactive power (from 0 to Qo and then to Q), the operating point moves along the downward line and the voltage reduces from Vo to V. This is the Q-V droop: higher reactive power output causes a small voltage drop, which helps multiple units share reactive power without direct communication.

III. Analysis Of Different Types Of Controller

A. Equations of Droop Controller

The measured output voltage(V_{0abc}) and current (I_{inv}) from load is given to abc/dq transformation to obtain V_{od}, V_{oq}, I_{od} and I_{oq} respectively and later the instantaneous active power(P) and reactive power(Q) is calculated.

$$P = (V_{od} * I_{od}) - (V_{oq} * I_{oq}) \quad (1)$$

$$Q = (V_{oq} * I_{od}) - (V_{od} * I_{oq}) \quad (2)$$

These instantaneous power is then given to low pass filter to obtain average active and reactive power, later we obtain reference voltage(V_{ref}) and angle θ in form of ωt for further controller blocks as feedback from (16) and (18).

B. Equations of Voltage controller

The obtained V_{ref} is then transformed to V_{dref} and V_{qref}, which is compared with output voltage V_{od} and V_{oq} to obtain voltage error and then given to PI controller to eliminate steady state voltage error later added to cross coupling terms to obtain I_{dref} and I_{qref}.

$$I_{dref} = (V_{dref} - V_{od})\left(K_p + \frac{K_i}{s}\right) - \omega C_f V_{oq} + I_{od} \quad (3)$$

$$I_{qref} = (V_{qref} - V_{oq})\left(K_p + \frac{K_i}{s}\right) + \omega C_f V_{od} + I_{oq} \quad (4)$$

This I_{dref} and I_{qref} is given to Current Controller as input.

C. Equations of Current controller

The obtained I_{dref} and I_{qref} which is compared with output voltage I_{od} and I_{oq} to obtain current error and then given to PI controller to eliminate steady state current error later added to cross coupling terms to obtain V_d and V_q.

$$V_d = (I_{dref} - I_{od})\left(K_p + \frac{K_i}{s}\right) - \omega L_C I_{oq} + V_{od} \quad (5)$$

$$V_q = (I_{qref} - I_{oq})\left(K_p + \frac{K_i}{s}\right) + \omega L_C I_{od} + V_{oq} \quad (6)$$

These V_d and V_q is again given back to dq/abc transformation to obtain V_{ref_abc} which is then compared with triangular wave to obtain to gate pulses to six switches.

D. Design Of LCL Filter

Design of LCL filter is as follows:

$$Z_b = \frac{(V)^2}{P} \quad (7)$$

$$C_b = \frac{1}{\omega_0 \cdot Z_b} \quad (8)$$

$$I_{max} = \frac{P}{V} \quad (9)$$

Where, V is line voltage, P is active power, C_b is base capacitance, ω_0 is nominal angular velocity, Z_b is base impedance. If the rated current is allowed to fluctuate by 10% for the design parameters, the values in (10) and (11) are obtained.

$$\Delta I_{L\_max} = \%10 \cdot I_{max} \quad (10)$$

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$$L_1 = \frac{V_{DC}}{6 \cdot f_{sw} \cdot \Delta I_{L\_max}} \quad (11)$$

Where, L1 is value inverter side inductance, f_{sw} is switching frequency, V_{DC} is dc link voltage. The capacitor value is limited by the reduction of the power factor (less than 5%) in the rated capacity. The capacitance value, the attenuation factor, the resonance value, and the resonance frequency are given by (12) and (14).

Limitation $Q_C \leq 0.05\ to\ 0.1 P_{rated}$

$$C_f = \frac{0.1\, P_{rated}}{2\pi \cdot f \cdot 3 \cdot V_{ph}^2} \quad (12)$$

$k_a = 0.2(\%20)$

Where k_a is the attenuation factor.

$$L_2 = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f \cdot \omega_{sw}^2} \quad (13)$$

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 \cdot L_2 \cdot C_f}} \quad (14)$$

Where, C_f is filter capacitance, L_2 is grid side inductance, f_{res} is resonance frequency. To avoid resonance problems for the filter (due to low and high harmonic ratings), the resonance frequency should be selected as half the switching frequency and 10 times the of grid frequency. Switching frequency and grid frequency range is shown in below.

$$10 f_0 < f_{res} < 0.5 f_{sw}$$

In order to prevent resonance and reduce a part of the ripple at the switching frequency, a series resistor connection with the capacitor is required. This resistor must be up to one third of the filter capacitor impedance at the resonance frequency rated. Resistor value calculate is given in (15).

$$R_f = \frac{1}{3 \cdot \omega_{res} \cdot C_f} \quad (15)$$

E. Design of Droop Co-efficients

1. Choose allowable deviations:
   i. Decide the maximum steady-state frequency deviation Δf_{max} from nominal (for example ±0.05–0.25 Hz around 50 Hz).
   ii. Decide the maximum steady-state voltage deviation ΔV_{max} at the PCC (for example ±5–10% of nominal phase-to-neutral voltage).

2. Fix rated and minimum powers:
   i. Take each inverter's rated active power P and choose the minimum active power point P_{ref} where full droop range ends often from no-load to rated, i.e. 0 to Prated.
   ii. Similarly, take the rated reactive power Q and its minimum Q_{ref} for the Q –V droop characteristic.
   iii. The difference $\Delta P = P - P_{ref}$ and $\Delta Q = Q - Q_{ref}$ defines the active and reactive power range covered by droop.

3. Compute basic droop gains:
   i. Active-power / frequency droop

$$\omega_{ref} = \omega_0 - m_P (P - P_{ref}) \quad (16)$$

$$m_P = \frac{\Delta \omega_{max}}{\Delta P} \quad (17)$$

where $\Delta\omega_{max} = 2\pi \cdot \Delta f_{max}$
m_P is in rad/sec per watt.

   ii. Reactive-power / voltage droop

$$V_{ref} = V_0 - n_Q (Q - Q_{ref}) \quad (18)$$

$$n_Q = \frac{\Delta V_{max}}{\Delta Q} \quad (19)$$

n_Q is in volt per var.

These formulas give droop slopes so that when power changes from P_{ref} to P, frequency drops at most Δf_{max}; similarly for voltage and reactive power.

F. Design of Line Impedance

From the given Line voltage, power ratings of inverter and nominal frequency, line impedance can be calculated as below,

$$S = \sqrt{P^2 + Q^2} \quad (20)$$

where P is active power, Q is reactive power and S is apparent power of inverter.

$$V_{ph} = \frac{V_L}{\sqrt{3}} \quad (21)$$

where V_{ph} is a phase voltage and V_L is line voltage.

Per-phase Apparent power is given as,

$$S_{ph} = \frac{S}{3} \quad (22)$$

Line Impedance per phase is given as below,

$$Z_f = \frac{V_{ph}^2}{S_{ph}} \quad (23)$$

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To find base Resistance,

$$R = \frac{Z_f}{\sqrt{1+(\frac{X}{R})^2}} \quad (24)$$

Considering short circuit ratio(SCR) = 50,

$$R_{actual} = \frac{R}{SCR} \quad (25)$$

So, $X = R_{actual}$ (26)

and

$X = 2\pi.fo.L$

$$L = \frac{X}{2\pi\ fo} \quad (27)$$

Finally, the resistance(R_{actual}) and inductance(L) are used as source impedance.

IV. Simulation Results

The parameters used in the simulation is provided in table I:

Table I: Simulation Specification of the system

Parameters	Values
DC Voltage (Vdc)	750V
Inverter Output Frequency (fo)	50Hz
Inverter Output Voltage (Vn)	400V
Power (individual inverter) (Pinv)	10kW
Switching Frequency (fsw)	15kHz
Load Power P1, Q1	12kW, 2kVAR
Load Power P2, Q2	8kW, 2kVAR
Load side Inductance L1	1.67mH
Load side Inductance L2	0.887mH
Filter Capacitance Cf	33μF

The designed inverter can keep its three-phase output voltage and frequency close to the desired values when supplying the R–L load through the LCL filter and line impedance. The waveforms at the load are sinusoidal, and the LCL filter removes most of the switching ripple so the current is smooth and power quality is good.

When the load or power are changed suddenly, the droop controller slightly adjusts the inverter voltage and frequency, and the inner voltage and current controllers quickly bring the system to a new steady state. The active and reactive powers move to their new reference values without large overshoot or long oscillations, which means the inverter can share power and keep the micro-grid stable even when the line impedance or load changes.

The simulation of parallel connected inverters of same ratings and R-L loads of different values and by using circuit breakers, six cases of operation is implemented. The inverter1 operates from t=0s to t=4s and inverter2 operates from t=4s to t=8s and both inverter1 and inverter2 operates from t=8s to t=12s. Similarly Load1 is connected from t = 0s to t=12s and load2 is connected from t=2s to 4s and 6s to 8s and 10 to 12s.

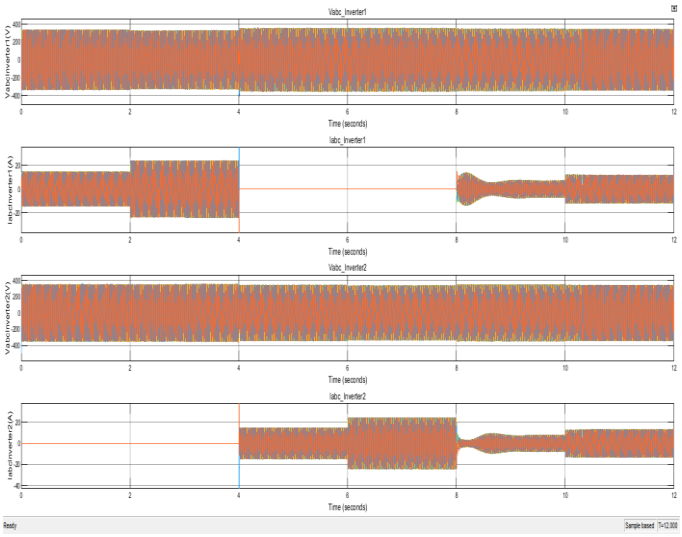

Fig. 4. Output voltage and current waveforms of both inverters

Fig. 4, shows the output voltage and current of each inverter in six different operating conditions where each condition is operated for 2 seconds over the range of 12 seconds.

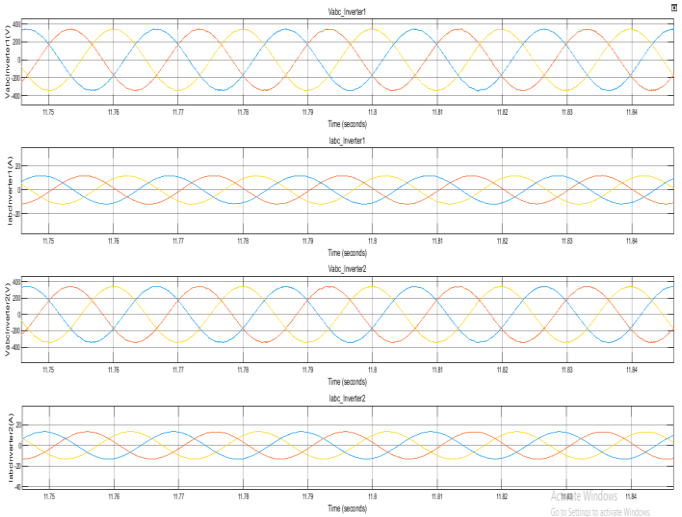

Fig. 5. Output voltage and current waveforms of both inverters in time t = 10 to 12s

The fig. 5, shows the output voltage and current waveforms during t = 10 to 12s, where both inverter and R-L loads are operating.

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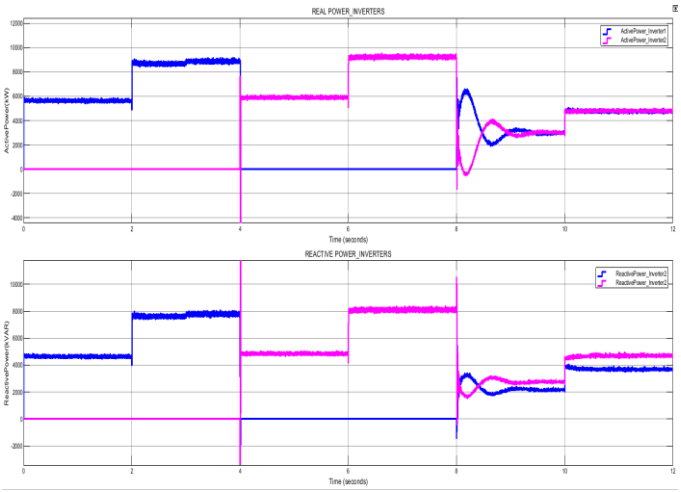

Fig. 6. Active power and reactive power of both inverter

Fig. 6, shows the active and reactive power of each inverter in six different operating conditions, and how power varies when load increases or decreases and also when single inverter is connected and or two inverters are connected.

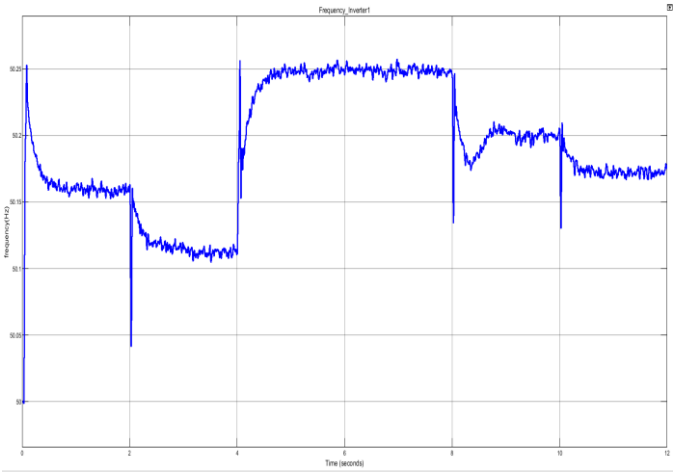

Fig. 7. Frequency Response of inverter1

In fig. 7, frequency of the inverter1 is provided in above graph in which when the inverter1 is disconnected or when load is varied, the frequency deviates from 50.05Hz to 50.25Hz.

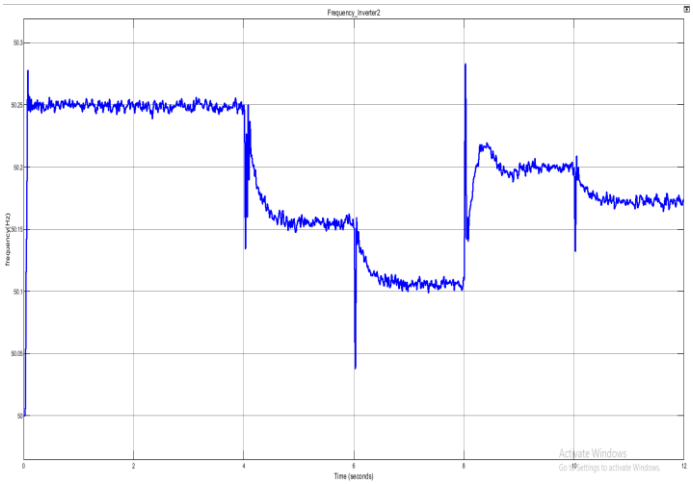

Fig. 8. Frequency Response of inverter2

In fig. 8, frequency of the inverter2 is provided in above graph in which when the inverter is disconnected or when load is varied, the frequency deviates from 50.05Hz to 50.25Hz.

From fig. 4 to 8, we can explain that when load increases, the power increases and frequency is dropped, and by droop control technique the frequency is stabilized within the limits, and inverter share active and reactive power proportionally.

From t >11s, both inverters and loads are operating, where voltage of inverters is 340V, current is around 12A, frequency is stabilized to 50.18Hz, and active power is balanced at 5kW and reactive power around 4kVAR.

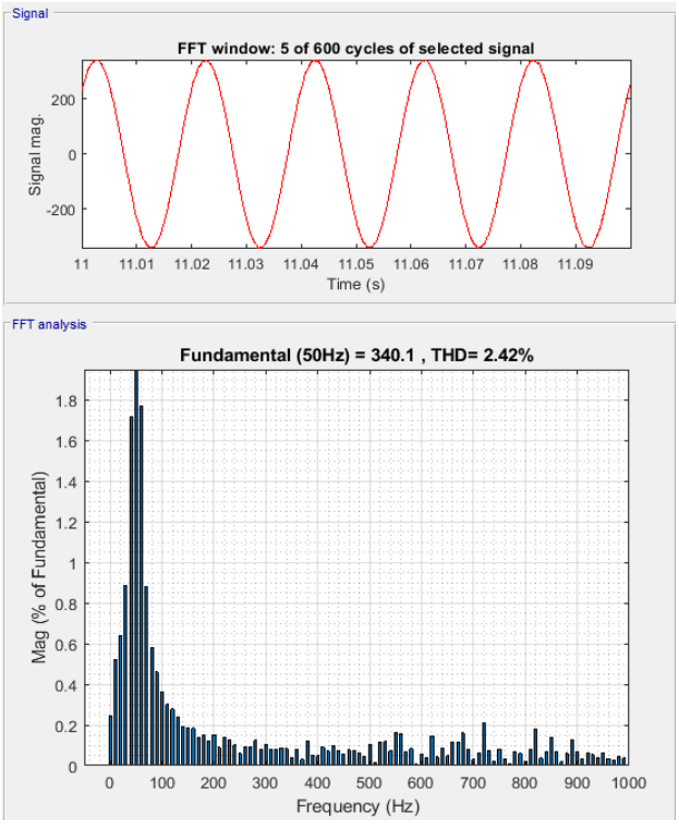

Fig. 9. Voltage THD values of inverter1

As shown in the fig. 9, the Total Harmonic Distortion (THD) of the output voltage of inverter1 is analyzed using FFT analysis. By using droop control technique and LCL filter, the total harmonic distortion is 2.42% which is within the acceptable limits of IEEE 519 Standards, for operating condition t > 11s where both inverter and loads are operating

As shown in the fig. 10, the Total Harmonic Distortion (THD) of the output current of inverter1 is analyzed using FFT analysis. By using droop control technique and LCL filter, the total harmonic distortion is 2.92% which is within the acceptable limits of IEEE 519 Standards, for operating condition t > 11s where both inverter and loads are operating.

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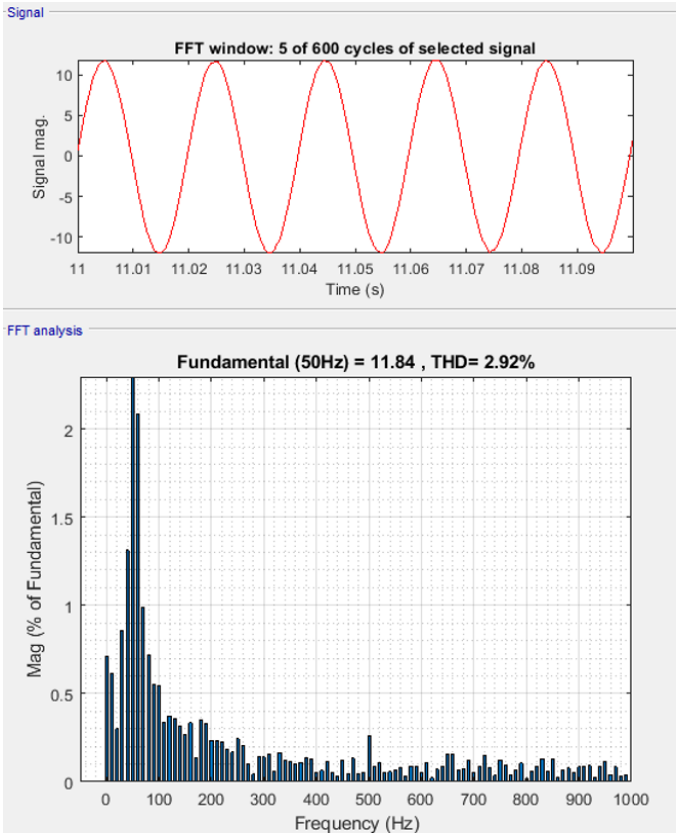

Fig. 10. Current THD values of inverter1

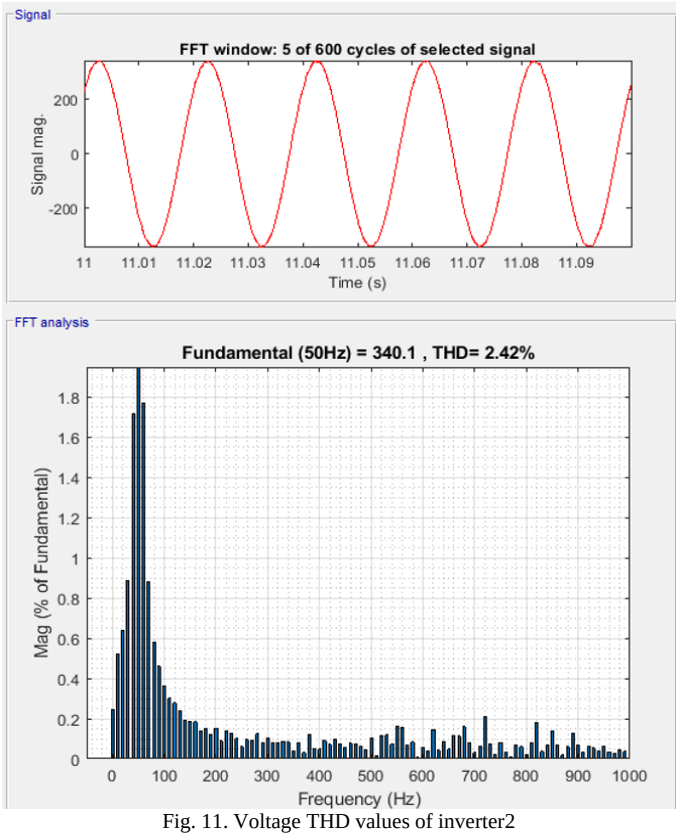

Fig. 11. Voltage THD values of inverter2

As shown in the fig. 11, the Total Harmonic Distortion (THD) of the output voltage of inverter2 is analyzed using FFT analysis. By using droop control technique and LCL filter, the total harmonic distortion is 2.42% which is within the acceptable limits of IEEE 519 Standards, for operating condition t > 11s where both inverter and loads are operating.

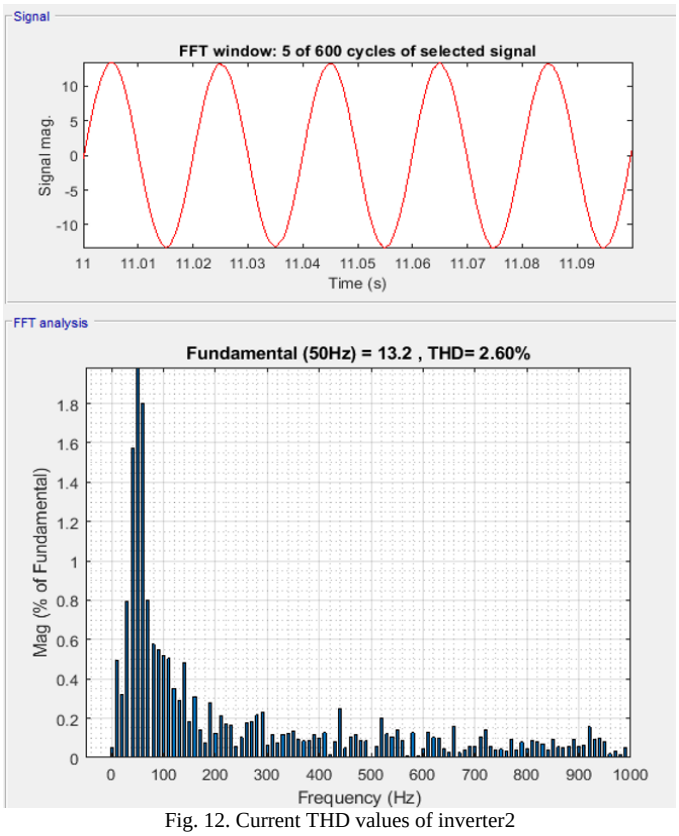

Fig. 12. Current THD values of inverter2

As shown in the fig. 12, the Total Harmonic Distortion (THD) of the output current of inverter2 is analyzed using FFT analysis. By using droop control technique and LCL filter, the total harmonic distortion is 2.60% which is within the acceptable limits of IEEE 519 Standards, for operating condition t > 11s where both inverter and loads are operating.

V. CONCLUSION

The proposed droop-controlled three-phase grid-forming inverter system was successfully designed and implemented with coordinated outer P–f and Q–V droop loops and inner dq-frame voltage and current controllers, enabling autonomous sharing of active and reactive power between two parallel VSIs supplying common R–L loads in islanded micro-grid mode. By proper selection of droop coefficients, LCL filter parameters, and controller gains, the inverters maintained stable bus voltage and frequency during load switching while dynamically adjusting power output to achieve near-proportional sharing without any communication link.

The Voltage of both inverters is around 400V, and Current is maintained around 12A. Harmonic performance analysis confirmed that the LCL filter and control strategy effectively attenuated switching ripple, resulting in a current THD of about 2.92% for inverter1 and 2.60% for inverter2 and a

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voltage THD of both inverters is about 2.42%, which lie within acceptable power quality limits for practical micro-grid applications as per IEEE 519 standards.

REFERENCES

[1] N. Pogaku, M. Prodanovic, and T. C. Green, “Modeling, Analysis and Testing of Autonomous Operation of an Inverter-Based Microgrid,” *IEEE Transactions on Power Electronics*, vol. 22, pp. 613-625, 2007.

[2] Yusuf Gupta, Neelima Parganiha, Akshay Kumar Rathore and Suryanarayana Doolla, “An Improved Reactive Power Sharing Method for an Islanded Microgrid,” *IEEE Transactions on Industry applications*, vol. 57, no-3, may/june 2021.

[3] Z. Kan, Z. Guo, C. Zhang, and X. Meng, “Research on droop control of inverter interface in autonomous microgrid,” in *Electronics and Application Conference and Exposition (PEAC)*, 2014 International, 2014, pp. 195-199.

[4] Q. C. Zhong and Y. Zeng, “Universal Droop Control of Inverters With Different Types of Output Impedance,” *IEEE Access*, vol. 4, pp. 702-712, 2016.

[5] M. C. Chandorkar, D. M. Divan, and R. Adapa, “Control of parallel connected inverters in standalone ac supply systems,” *IEEE Trans. Ind. Appl.*, vol. 29, no. 1, pp. 136–143, Jan. 1993.

[6] Allal. El Moubarek Bouzid, Pierre Sicard, Amine Yamane, Jean-Nicolas Paquin, “Simulation of Droop Control Strategy for Parallel Inverters in Autonomous AC Microgrids*,” 8th International Conference on Modelling, Identification and Control (ICMIC)*, 2016.

[7] Wei Zhang et al., "Droop Control Method to Achieve Maximum Power Output of Photovoltaic for Parallel Inverter System”, *CSEE Journal of Power and Energy Systems*, vol. 8, november 2022.

[8] M. Su et al., "Stability analysis and stabilization methods of DC micro-grid with multiple parallel-connected DC–DC converters loaded by CPLs,*" IEEE Transactions on Smart Grid*, pp. 132-142, 2016.

[9] Q. Hongxia et al., "Discussion on the technology of intelligent micro-grid and flexible distribution system," *Power System Protection and Control*, vol. 44, pp. 17-23, 2016.

[10] S. Chandran and P. Lenin, “A review on active & reactive power control strategy for a standalone hybrid renewable energy system based on droop control,” in *International Conference on Power, Signals, Control and Computations (EPSCICON)*, 2018, pp. 1-10: *IEEE*.

[11] Saurabh Kharjule , “Voltage Source Inverter”, *International Conference on Energy Systems and Applications (ICESA)*, vol. 12, pp. 842–850, 2015.

[12] Suleman Haider et al., “A dual control strategy for power sharing improvement in islanded mode of AC micro-grids”, Protection and Control of Modern Power Systems, vol. 3 , 2018.