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Analysis of Multilevel Inverter with Different Topologies

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***Abstract* — In this paper H-bridge topologies of a higher output voltage level in multilevel inverters with reduce number of switches is proposed. These topologies maintain the performance of a 15 level output from multilevel inverter and reduction in switching losses, installation area, converter cost and size. The converter has a simple strategy switching control. One topology consists of 16 switches and the other topology has 10 switches and 6 diodes. An output waveform is analyzed and the Total Harmonics Distortion (THD) results are compared to conventional method. The validity of the analysis has been proved by simulation.**

Main objective of multilevel inverter is to reduce the THD in the operating system. Normally it is achieved by increasing the number of the DC source and the switch. However, this method will increase the power losses. That is why the new topology will try to reduce the component without reducing the quality output of converter. Due to the stepped output waveform characteristic of a multilevel inverter, the Total Harmonic Distortion (THD) content is low compared to the conventional two-level inverters.

Index Terms— Multilevel inverter, Cascaded multilevel inverter, Sub-multilevel inverter, Full-bridge, H-bridge

I. INTRODUCTION

The converters have to be designed to obtain a quality output voltage or a current waveform with a minimum amount of ripple content. In high power and high voltage applications the conventional two level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of the power device ratings. Series and parallel combination of power switches in order to achieve the power handling voltages and currents. The conventional two level inverters produce THD levels around sixty percent even under normal operating conditions which are undesirable and cause more losses and other power quality problems too on the AC drives and utilities.

For high voltage applications, two or more power switches can be connected in series in order to provide the desired voltage rating. However, the characteristics of devices of the same type are not identical. For the same OFF state current, their OFF state voltages differ. Even during the turn OFF of the switches the variations in stored charges cause difference in the reverse voltage sharing. The switch with the least recovered charge faces the highest transient voltage. For higher current handling, the switches are connected in parallel, however because of uneven switch characteristics the load current is not shared equally. If a power switch carries more current than that of the others, then the power dissipation in it increases, thereby increasing the junction temperature and decreasing the internal resistance. This in turn increases its current sharing and may damage the devices permanently which is undesirable for critical applications.

In the conventional two level inverters the input DC is converted into the AC supply of desired frequency and voltage with the aid of semiconductor power switches. Depending on the configuration, four or six switches are used. A group of switches provide the positive half cycle at the output which is called as positive group switches and the other group which supplies the negative half cycle is called negative group. A detailed comparison is made between the conventional and multilevel inverter as shown in

S.No.	Conventional Inverter	Multilevel Inverter
1	Higher THD in output voltage	Low THD in output voltage
2	More switching stresses on devices	Reduced switching stresses on devices
3	Not applicable for high voltage applications	Applicable for high voltage applications
4	Higher voltage levels are not produced	Higher voltage levels are produced
5	Since dv/dt is high, the EMI from system is high	Since dv/dt is low, the EMI from system is low
6	Higher switching frequency is used hence switching losses is high	Lower switching frequency can be used and hence reduction in switching losses
7	Power bus structure, control schemes are simple	control scheme becomes complex as number of levels increases
8	Reliability is high	Reliability can be improved, rack swapping of levels is possible

Table 1.1.
Table 1 Comparison of conventional two level inverters and Multilevel inverter

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The multilevel inverters perform power conversion in multilevel voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility and higher voltage capability.

One of the most important problems in controlling a multilevel voltage source inverter is to obtain a variable amplitude and frequency sinusoidal output by employing simple control techniques. Indeed, in voltage source inverters, non-fundamental current harmonics cause power losses, electromagnetic interference and pulsating torques in AC motor drives. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy. In multilevel voltage source inverters, various Pulse Width Modulation control schemes have been developed.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are $2n+1$, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two former types. Fig.1 shows an 5 level cascaded H-bridge multilevel inverter. An n level cascaded H-bridge multilevel inverter needs $2(n-1)$ switching devices where n is the number of the output voltage level.

5-level Cascaded H-bridge multilevel inverter

The output voltage of this inverter has 5 levels like in the flying capacitor type and diode clamped type multilevel inverters. This inverter consists of two H-bridge inverters that are cascaded. For a 5-level cascaded H-bridge multilevel inverter 8 switching devices are need. The switching states are as shown in table. The different voltage levels can be obtained at the output terminals are 2Vdc , Vdc , 0, -Vdc , -2 Vdc . If the DC voltage sources in both the inverter circuits connected in series are not equal to each other, then also levels can be obtained at the output terminals. The number of levels in the output voltage can be increased by adding an identical inverter in series. The n number of output phase voltage levels in a cascaded inverter with s separate dc sources and 2s+ 1possible levels.

V0	Sa1	Sa2	Sa3	Sa4	Sb5	Sb6	Sb7	Sb8
2Vdc	1	1	0	0	1	1	0	0
Vdc	1	1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
-Vdc	0	0	1	1	1	0	0	1
-2Vdc	0	0	1	1	0	0	1	1

Table 2:- Switching states Cascaded H-Bridge Inverter

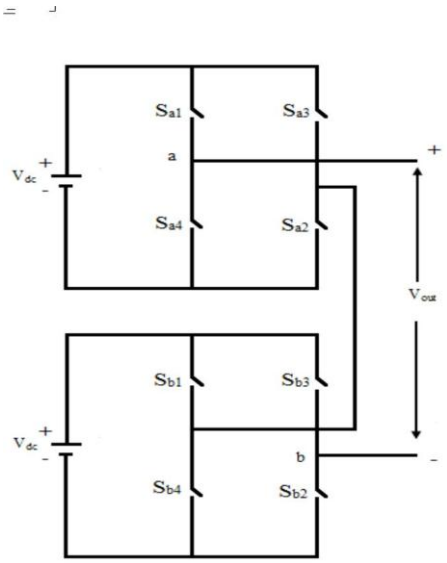

Fig 1:- Five level cascaded multilevel inverter

III. TOTAL HARMONIC DISTORTION (THD)

When a signal passes through a non-ideal, non-linear device, additional content is added at the harmonics of the original frequencies. THD is a measurement of the extent of that distortion.

When the main performance criterion is the ″purity″ of the original sine wave (in other words, the contribution of the original frequency with respect to its harmonics), the measurement is most commonly defined as the ratio of the RMS amplitude of a set of higher harmonic frequencies to the RMS amplitude of the first harmonic, or fundamental, frequency.

In Multilevel inverter THD analysis is done for both voltage and current as shown in (6.1),(6.2)

$$THD = \left(\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2)}}{V_1} \right) * 100$$

THD for voltage

$$THD_i = \sqrt{\sum_{h=2}^{H} \left(\frac{I_h}{I_1} \right)^2} = \frac{\sqrt{I_2^2 + I_3^2 + \ldots + I_{40}^2}}{I_1}$$

THD for current

Where V_n is the RMS voltage of the nth harmonic and n is the frequency of other than fundamental.

The comparison of THD levels for three different topologies shown in results (Refer Fig.17).

III. PULSE GENERATOR

Pulse Generator block is present in Fundamental Blocks/Power Electronics in Simulink Library.

Fig. 2:- Pulse Generator block

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The Pulse Generator block generates square wave pulses at regular intervals. The block waveform parameters, Amplitude, Pulse Width, Period, and Phase delay, determine the shape of the output waveform. The following Fig.3 shows how each parameter affects the waveform.

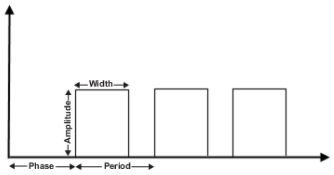

Fig. 3:- Square wave Pulse Generation

The Pulse Generator can emit scalar, vector, or matrix signals of any real data type. To cause the block to emit a scalar signal, use scalars to specify the waveform parameters. To cause the block to emit a vector or matrix signal, use vectors or matrices, respectively, to specify the waveform parameters. Each element of the waveform parameters affects the corresponding element of the output signal. For example, the first element of a vector amplitude parameter determines the amplitude of the first element of a vector output pulse. All the waveform parameters must have the same dimensions after scalar expansion. The data type of the output is the same as the data type of the Amplitude parameter.

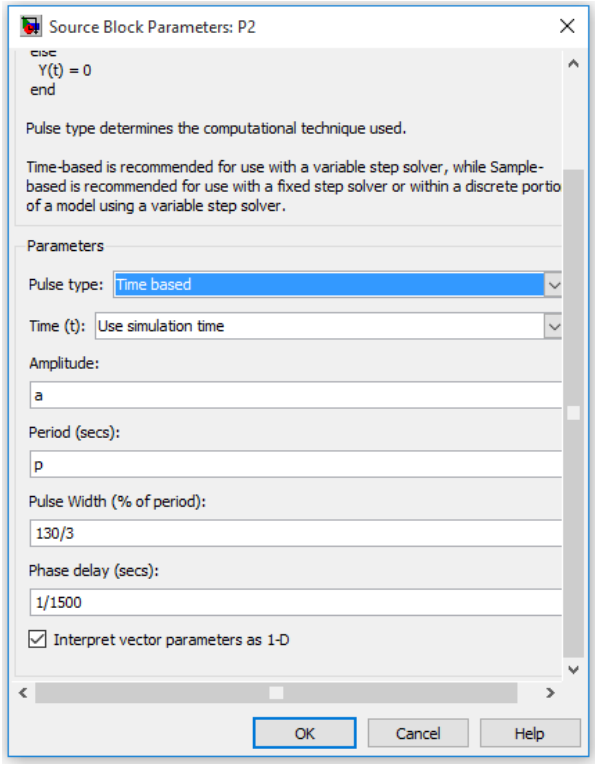

Fig. 4:- Pulse Generator Parameters

Modes of pulse generation

This block output can be generated in time-based or sample-based modes, determined by the Pulse type parameter.

Time-Based Mode

In time-based mode, Simulink® computes the block output only at times when the output actually changes. This approach results in fewer computations for the block output over the simulation time period. Activate this mode by setting the Pulse type parameter to Time based.

The block does not support a time-based configuration that results in a constant output signal. Simulink returns an error if the parameters Pulse Width and Period satisfy either of these conditions:

$$\text{Period} * \frac{Pulse\ Width}{100} = 0$$

$$\text{Period} * \frac{Pulse\ Width}{100} = \text{Period}$$

Depending on the pulse waveform characteristics, the intervals between changes in the block output can vary. For this reason, a time-based Pulse Generator block has a variable sample time. The sample time color of such blocks is brown.

Simulink cannot use a fixed-step solver to compute the output of a time-based pulse generator. If you specify a fixed-step solver for models that contain time-based pulse generators, Simulink computes a fixed sample time for the time-based pulse generators. Then the time-based pulse generators simulate as sample based.

If you use a fixed-step solver and the **Pulse type** is Time based, choose the step size such that the period, phase delay, and pulse width (in seconds) are integer multiples of the solver step size. For example, suppose that the period is 4 seconds, the pulse width is 75% (that is, 3 s), and the phase delay is 1 s. In this case, the computed sample time is 1 s. Therefore, choose a fixed-step size of 1 or a number that divides 1 exactly (e.g., 0.25). You can guarantee this by setting the fixed-step solver step size to auto on the **Solver** pane of the Configuration Parameters dialog box.

Sample-Based Mode

In sample-based mode, the block computes its outputs at fixed intervals that you specify. Activate this mode by setting the Pulse type parameter to Sample based.

An important difference between the time-based and sample-based modes is that in time-based mode, the block output is based on simulation time, and in sample-based mode, the block output depends only on the simulation start, regardless of elapsed simulation time.

This block supports reset semantics in sample-based mode. For example, if a Pulse Generator is in a resettable subsystem that hits a reset trigger, the block output resets to its initial condition.

Data Type Support

The Pulse Generator block outputs real signals of any numeric data type that Simulink supports, including fixed-point data types. The data type of the output signal is the same as that of the Amplitude parameter.

Difference between Time-Based and Sample-Based Pulse Generation Modes

This example shows the difference in the behavior of the Pulse Generator block in time-based and sample-based modes.

Consider a model with two Pulse Generator blocks. In one block, the **Pulse type** parameter is set to Time based. In the other block, it is set to Sample based. Both blocks are

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set up to output a Boolean pulse of 10 seconds: 5 seconds on followed by 5 seconds off. The simulation runs for 15 seconds from a start time of 3 seconds to a stop time of 18 seconds, specified in the Model Configuration Parameters dialog box. The figure shows the block diagram for this model and the simulation output in the Scope block.

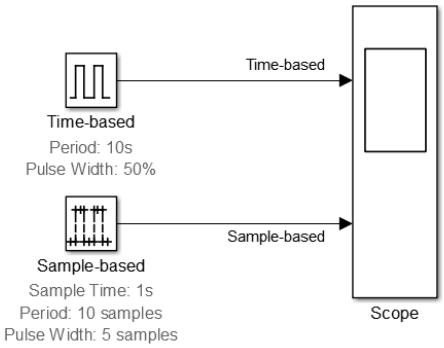

Fig.5:- Circuit for comparison of two modes

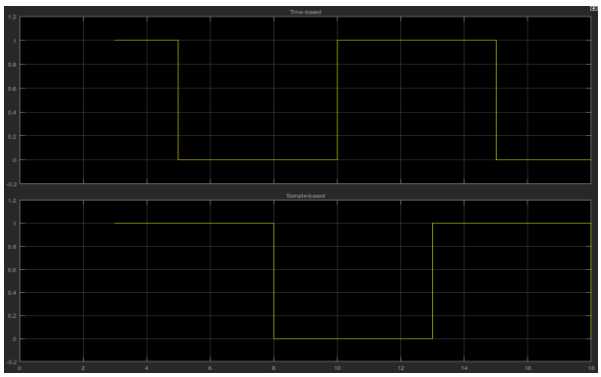

Fig. 6:- Pulses generated under two modes

IV. MATLAB/SIMULINK MODELS

The simulation is being done for the topologies with 28, 16 and 10 IGBT switches respectively. Simulations are done by using PWM technique, harmonics spectrum analysis also done through using FFT window in MATLAB/Simulink.

Single-Phase Inverter

An Inverter is a circuit which converts a DC power input into an AC power output at a desired output voltage and frequency. This conversion is achieved by controlled turn-on and turn-off devices like IGBT's. Ideally, the output voltage of an Inverter should be strictly sinusoidal. However the outputs are usually rich in harmonics and are almost always non-sinusoidal.

The DC power input to the inverter may be a battery, a fuel cell, solar cell or any other DC source. Most industrial applications use a rectifier which takes AC supply from the mains and converts it into DC to feed it to the inverter

The following Single-phase Inverter circuit was modeled in MATLAB/Simulink and is explained as follows.

Modeling the 15 level MLI

The Power Circuit of the Single-Phase Inverter consists of 4 bidirectional IGBT's arranged in bridge-form. The input to each H-bridge is a Vref (240/7=34.28) Volts DC supply from a battery. The IGBT/Diodes are triggered in various distinct cycles.

In the first cycle, from 0 to 180 degrees, IGBT/Diode 2 and 3 are triggered by applying signal to their gates. Thus they conduct during this period and output is obtained across the load.

In the next cycle, from 180 to 360 degrees, IGBT/Diode1 and 4 are triggered and they conduct during this period. Hence the output of V_{ref} (240/7=34.28) Volts is obtained across the load in the opposite direction. Thus a DC supply voltage is converted to AC voltage across the load and Inverter action is obtained.

This holds good for only one level. The remaining levels are obtained by switching the IGBTs as shown in table. Thus 15 level output is obtained as shown below.

Here figures shows the output waveforms of the 15-level with 28 switches, 16 switches and 10 switches which is being produced by PWM technique. The total harmonic distortion of each topology is analyzed by using FFT spectrum analysis. The MATLAB models, waveforms and THD analysis are of each topology are shown below figures.

Modeling with 28 switches

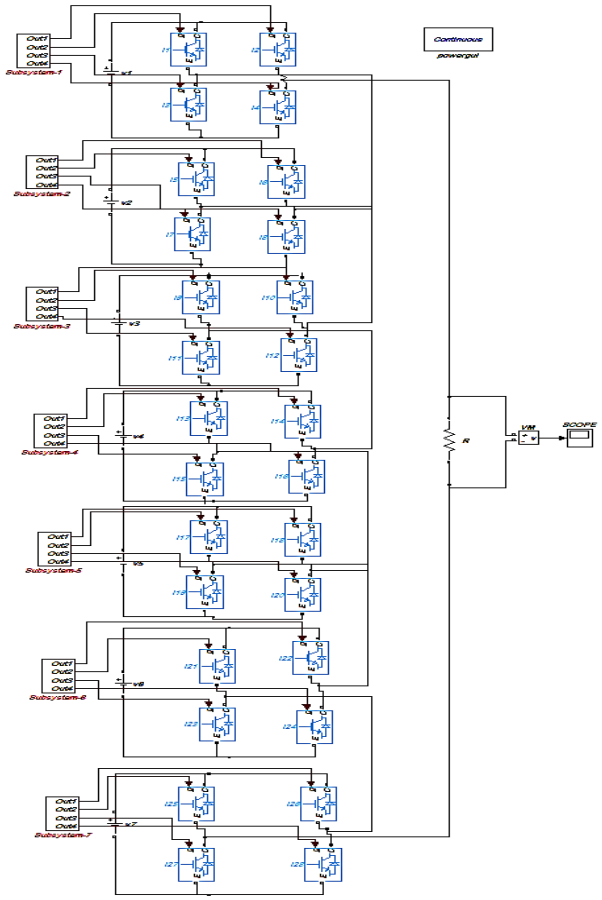

Fig. 7:- Circuit for 28 switches.

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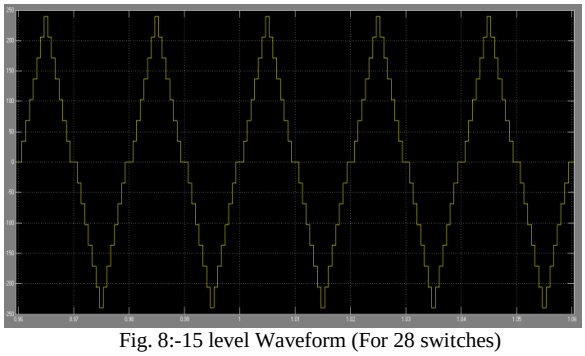

Fig. 8:-15 level Waveform (For 28 switches)

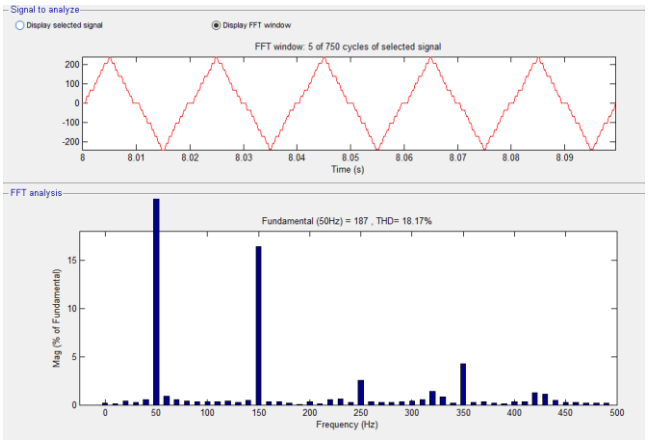

Fig. 9:-THD analysis (For 28 switches)

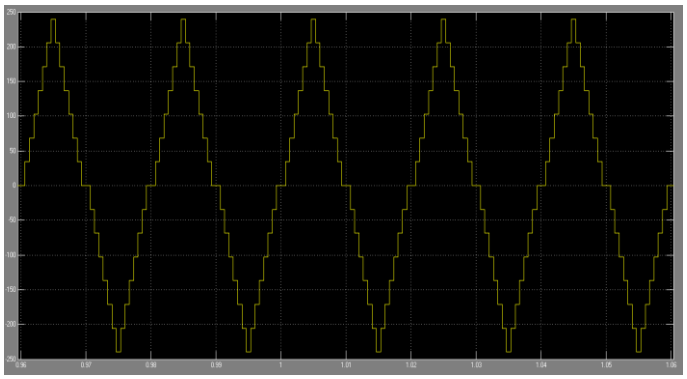

Fig. 10:-15 level Waveform (For 16 switches)

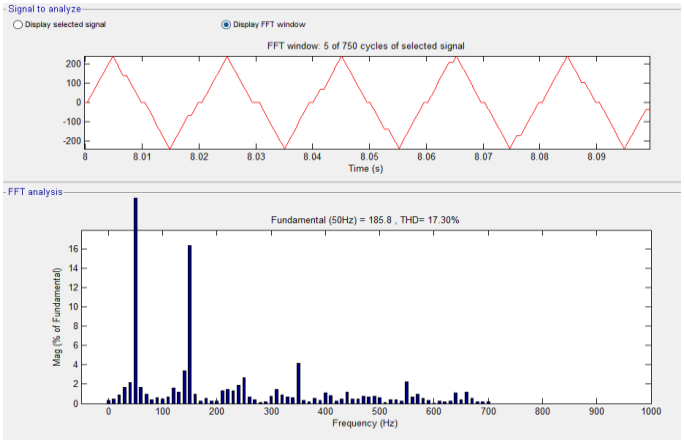

Fig 11:- THD analysis (For 16 switches)

Modeling with 16 switches

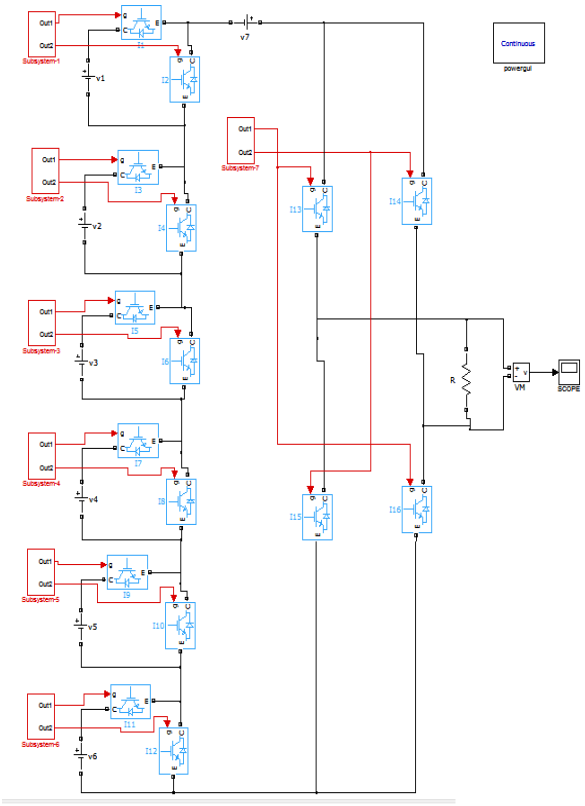

Fig. 10:- Circuit with 16 switches.

Modeling with 10 switches

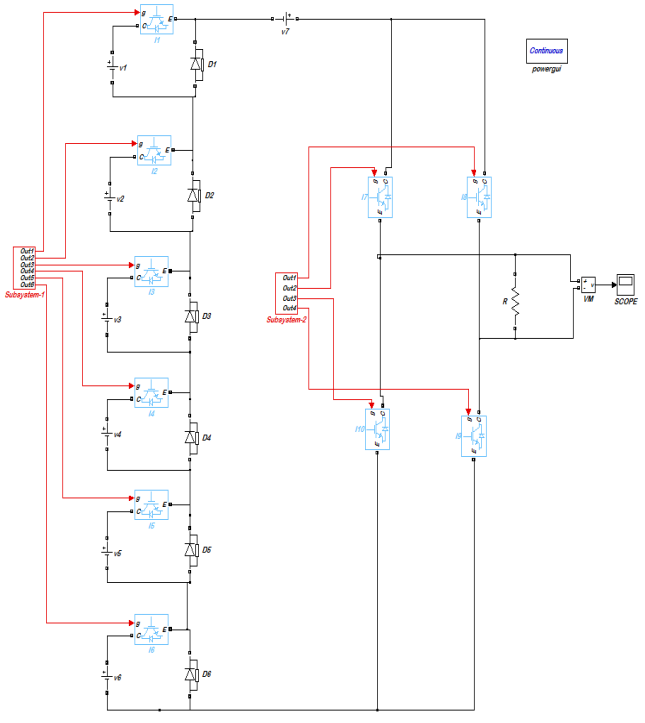

Fig. 12:- Circuit with 10 switches

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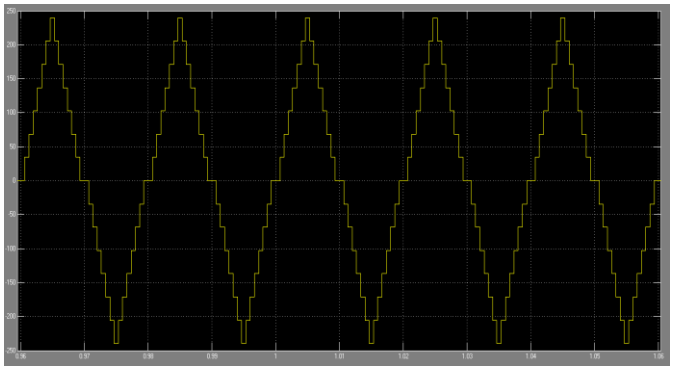

Fig. 13:-15 level waveform (For 10 switches)

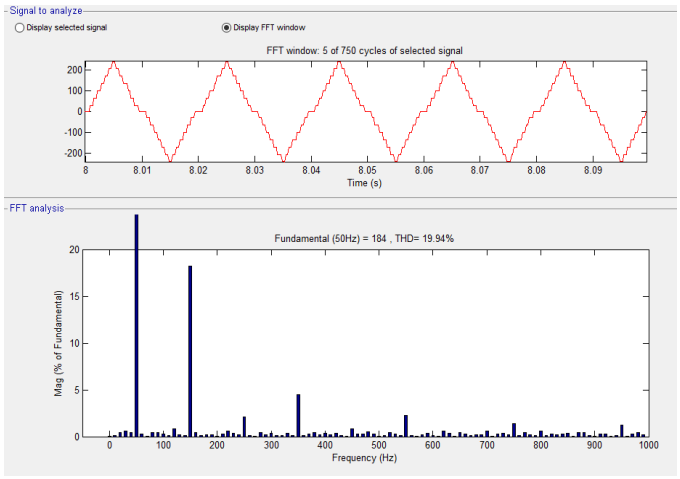

Fig. 14:- THD analysis (For 16 switches)

Comparison of 3 topologies

The outputs of the three topologies are same, but the cost, voltages stress of the switches differ.

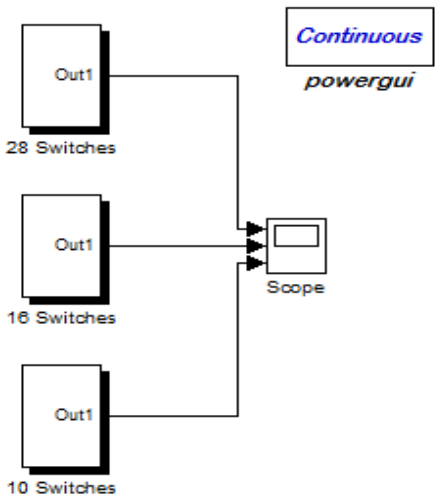

Fig. 15:- Circuit for comparison

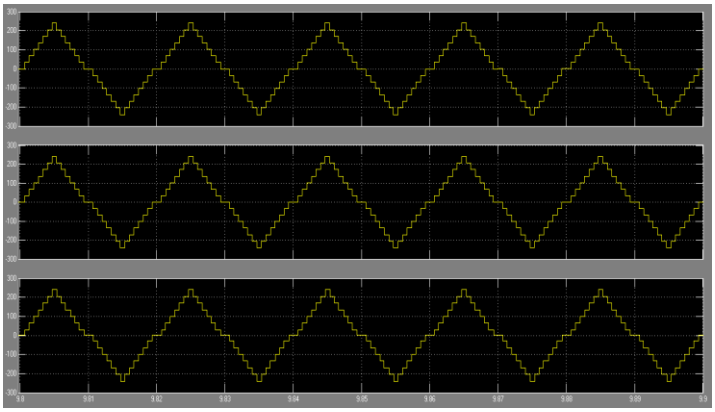

Fig. 16:- Comparison of Waveform

The following chart shows three topologies (with 28, 16, 10 switches) and comparison is drawn between them based on THD(%), Number of diodes and Number of Switches (IGBTs).

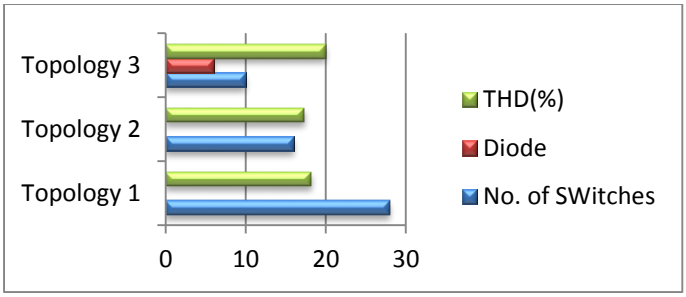

Fig. 17:- THD Chart for 3 topologies

Comparison of different MLIs

The following table shows the comparison between three types of multilevel inverters i.e., between Diode clamped MLI, Capacitor clamped MLI and Cascaded MLI. In Cascaded MLI three different topologies are compared. The comparison is made between number of switches, diodes and capacitor.

MLI Type→	Diode Clamped MLI	Capacitor Clamped MLI	Cascaded MLI		
No. of ↓			Topology 1	Topology 2	Topology 3
Switches	28	28	28	16	10
Diodes	182	-	-	-	6
Capacitor	14	30	-	-	-

Table 3: Comparison of 3 types of MLI

V. CONCLUSION

It is concluded that, Multilevel inverter is more advantageous than the conventional inverter with advantages such as reduced stress on switches, low THD and more reliability among others. In Multilevel inverter, Cascaded H-bridge inverter has more advantages over diode-clamped and flying capacitor inverter such as requirement of least number

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of components, soft switching techniques which reduces switching losses and device stresses among others.

In cascaded MLI, three topologies with different number of switches are simulated among which the topology with 10 switches is more advantageous because it has less number of switches which reduces cost and complexity of the circuit when compared to circuits with 16 and 28 switches. But the topology with 10 switches has slightly increased THD percentage.

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